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2005

On the design of turbo codes with convolutional interleavers

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On the Design of Turbo Codes with Convolutional Interleavers

A thesis submitted in fulfilment of the
requirements for the award of the degree

Doctor of Philosophy

from

THE UNIVERSITY OF WOLLONGONG

by

Sina Vafi
Master of Engineering

SCHOOL OF ELECTRICAL, COMPUTER
AND TELECOMMUNICATIONS ENGINEERING
2005

*To my beloved Parents
and Sisters, Tina and Nikan*

Abstract

Random interleavers are amongst the most effective interleavers for turbo codes. However, due to their random permutations, a compact representation of the code specification is a major obstacle. Thus, to date, much research has been conducted on the design of deterministic interleavers having performances close to random interleavers. These interleavers are mainly constructed as block interleavers, which allows the code to be analyzed as a block code.

In contrast to block interleavers, there are non-block interleavers. These utilize a reduced number of memories in their structures and have self-synchronization with their deinterleavers; this simplifies their design. Because of their non-block structures, turbo codes constructed by these interleavers must usually be analyzed in terms of the continuous performance. Previous research confirms that the codes' continuous performance is similar to their block performance, but at the expense of increased complexity of the code analysis and decoding. In order to analyze a turbo code constructed with non-block interleavers as a block code, it is necessary to consider the applied interleavers as block interleavers. This is accomplished by the insertion of stuff bits at the end of each input data block, returning the interleaver memories to zero state.

This thesis is related to the application of convolutional interleavers which are the most popular non-block interleavers for turbo codes. It introduces convolutional interleavers as good deterministic interleavers that can perform similar or even better than previous deterministic and random interleavers. The thesis presents two different structures of block-wise convolutional interleavers, created on the basis of distribution of stuff bits in the interleaved data. On the basis of convolutional interleaver

properties, a simple algorithm is introduced to analyze code performance at different signal to noise ratios. The code analysis is confirmed with simulation results, which allow selection of the most suitable interleaver.

Different models of the selected convolutional interleavers are verified. These models are constructed based on changing the period and space values, which are introduced as the constituent parameters of convolutional interleavers. The performance of interleavers with different periods and a space value 1 are investigated. For a similar number of stuff bits, these interleavers are compared with interleavers constructed with shorter periods and highest fixed space values than 1. Convolutional interleavers with variable space values operating as generalized convolutional interleavers are also presented and their performance is compared with interleavers using the fixed space value.

Turbo codes constituted with the mentioned interleavers are analyzed using different input bitstreams. Based on the analysis, suitable modifications are proposed for each model of interleaver so as to improve the turbo code performance through a reduced number of stuff bits. The performance of the modified convolutional interleavers is compared with good deterministic and random block interleavers. The results demonstrate that with an acceptable number of stuff bits contributed to each interleaved data, convolutional interleavers provide similar or improved performance when compared to block interleavers.

Finally, the application of designed convolutional interleavers in Unequal Error Protection (UEP) turbo codes is presented. Based on the code specifications and interleaver properties, three different techniques for UEP are suggested to improve protection of priority data, while reducing the overall number of stuff bits inserted into the interleaver memories.

Statement of Originality

This is to certify that the work described in this thesis is entirely my own, except where due reference is made in the text.

No work in this thesis has been submitted for a degree to any other university or institution.

Signed

Sina Vafi

December, 2005

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List of Abbreviations

3G	3rd Generation
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
Bi-SOVA	Bidirectional SOVA
BRC	Block-Random Chaotic
BSC	Binary Symmetric Channel
DAB	Digital Audio Broadcasting
DRP	Dithered Relative Prime
DVB	Digital Video Broadcasting
EEP	Equal Error Protection
FEC	Forward Error Correction
FSP	Finite State Permuter
LAN	Local Area Network
LLR	Log-Likelihood Ratio
MAP	Maximum A-Posteriori
ML	Maximum Likelihood
OFDM	Orthogonal Frequency Division Multiplexing
RSC	Recursive Systematic Convolutional
SNR	Signal to Noise Ratio
SOVA	Soft Output Viterbi Algorithm
UEP	Unequal Error Protection
XOR	Exclusive OR