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January 2015

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Abstract

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Keywords

modulation, balancing, control, strategy, single, phase, five, level, anpc, converter, novel, technique

Publication Details

H. R. Teymour, D. Sutanto, K. M. Muttaqi & P. Ciufo, "A novel modulation technique and a new balancing control strategy for a single-phase five-level ANPC converter," IEEE Transactions on Industry Applications, vol. 51, (2) pp. 1215-1227, 2015.

This journal article is available at Research Online: https://ro.uow.edu.au/eispapers/3872

A Novel Modulation Technique and a New Balancing Control Strategy for a Single-phase Five-level ANPC Converter

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***Abstract*—This paper proposes a novel modulation technique and a new balancing control strategy for a single-phase five-level flying capacitor (FC) based active-neutral-point-clamped (ANPC) converter. The proposed modulator can control the FC voltage to follow the requested reference value and simultaneously generate the required ac output voltage regardless of the values of the dc capacitor voltages of the converter. By implementing this method, smaller values of dc-link and flying capacitors can be used even in applications that could experience ripple or transient in the capacitors voltage. In a single-phase five-level ANPC converter applications, where the capacitors can experience pulsation power and dc-link balancing issues, such as grid connected PV system, the selection of the reference voltage value for the FC can play an important role to balance the average values of the dc-link capacitors voltage. The proposed new control strategy uses a new reference voltage for the FC to be applied by the new modulator to have an average balanced dc-link voltages as well as an ac output voltage with good power quality. Simulation studies and experimental results demonstrate the effectiveness of the proposed modulation technique and control strategy even with relatively small dc capacitors to produce high quality output voltage and current waveforms while maintaining an average balanced dc-link voltages.**

***Index Terms*—Active-neutral-point-clamped (ANPC) converter, flying capacitor, multilevel converters, photovoltaic (PV) power system, pulse width modulation, voltage balancing.**

I. Introduction

In recent years, multi-level converters have been under research and development for several industrial applications [1]–[3]. One of the new topologies of multilevel converters is a five-level active neutral point clamped (5L-ANPC) converter which was introduced by ABB to combine the flexibility of the multi-level floating capacitor converters with the robustness of NPC converters [2]. Recently, the proposed topology was commercialized for industrial motor drive applications and has been proposed for a 6 MVA wind power application [1], [3]. Fig. 1 shows a circuit of a single phase FC-based 5L-ANPC converter which can be used in low voltage applications.

The redundancy in the switching states of the FC-based ANPC converter allows the voltage across FC to be regulated.

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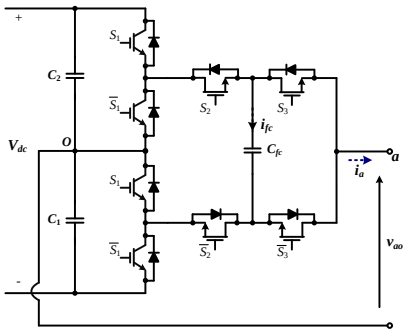


Fig. 1. Single-phase five-level ANPC converter

To generate the switching pulses, a variety of strategies have been presented to generate the output voltage with reduced harmonics and simultaneously regulate the FC voltage of the converter such as carrier-based PWM [4], modified triangular carrier-based PWM [5], optimized pulse pattern [6] and selective harmonic elimination PWM (SHE-PWM) [7], [8]. In these methods, to generate switching pulses, the dc-link capacitor voltages are considered to be balanced or the calculation is carried out based on balanced condition.

Space vector PWM is used to generate switching pulses of three-phase five-level converters in [9], [10], [11] and [12]. Proper switching vectors between available redundancies are selected to control the FC voltages and to achieve balanced dc-link capacitor voltages. In [13] and [14], an optimum zero-sequence voltage is added to obtain balanced dc-link voltages. These methods are normally suitable for three-phase applications.

Although different techniques have been reported to control and generate switching pulses in the FC-based 5L-ANPC converter, most of these are mainly suitable for a three-phase application and virtually in all of these approaches, the dc-link capacitor voltages are considered balanced or controlled to be balanced. But in some applications or under transient conditions, the dc-link capacitor voltages can experience voltage variation and also have a risk to become unbalanced. In single-phase applications, where the dc-link capacitors can experience pulsation power and consequently ripple in their voltages, the ability to reduce the effect of voltage ripples on the dynamic behaviour of the system is crucial. The ability to work under continuous ripple condition is considered to be desirable for the modulator. Furthermore, the dc-link capacitor voltage balancing is another problem encountered in single

TABLE I
SWITCHING STATES OF THE FIVE-LEVEL ANPC CONVERTER

Switching states	S_1	S_2	S_3	Phase voltage V_{ao}	V_{ao} Symetrical	FC Current i_{fc}
V_1	0	0	0	$-V_{C1}$	$-V_{dc}/2$	0
V_2	0	0	1	$V_{fc}-V_{C1}$	$-V_{dc}/4$	$-i_a$
V_3	0	1	0	$-V_{fc}$	$-V_{dc}/4$	i_a
V_4	0	1	1	0	0	0
V_5	1	0	0	0	0	0
V_6	1	0	1	V_{fc}	$V_{dc}/4$	$-i_a$
V_7	1	1	0	$V_{C2}-V_{fc}$	$V_{dc}/4$	i_a
V_8	1	1	1	V_{C2}	$V_{dc}/2$	0

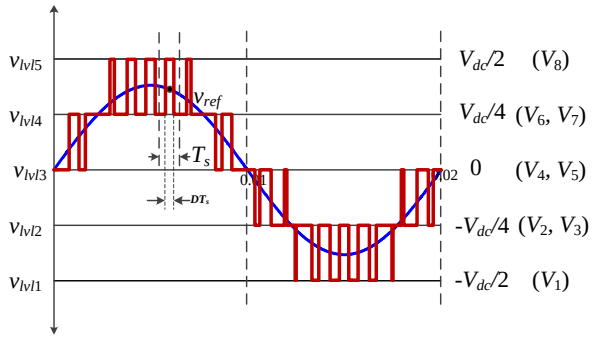


Fig. 2. Inverter PWM output voltage with redundancy in switching states to generate a sinusoidal output voltage

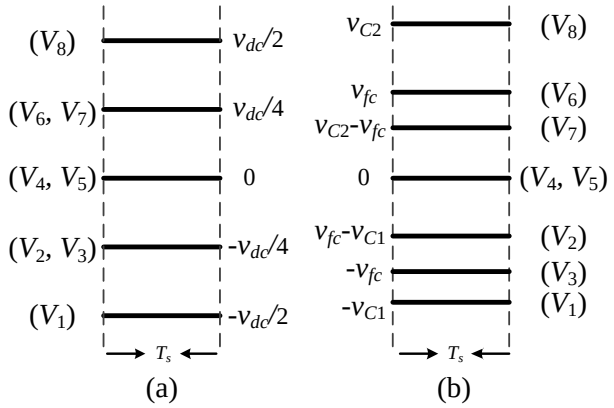


Fig. 3. Switching states and corresponding output voltage levels during a short time-step for (a) symmetrical voltage conditions, (b) unsymmetrical voltage conditions

phase applications, which cannot be solved using a three phase technique such as adding zero-sequence voltage [13]. Applying unsymmetrical switching pattern in each half cycle can overcome unbalancing problems, however it will reduce the quality of the converter output. Also, in most single-phase applications, a dc-link voltage divergence problem can occur if the FC voltage is controlled to be a fixed value (a quarter of the dc-link voltage) as will be demonstrated in this paper.

To overcome these problems, this paper presents a new modulator which can produce the requested output voltage even when there is unbalance and ripple in the dc-link capacitors. The proposed modulation technique adds the ability to control the FC voltage to follow the requested reference voltage without need to be to be always equal to a quarter of the dc-link voltage. In addition, by applying the proposed modulation technique, a new reference generation technique for FC voltage is introduced in this paper to overcome the dc-link voltage divergence problem, even though the capacitors may have ripple in their voltages, without reducing the quality of the converter output.

This paper is organized in the following way. In Section II, the operation principles of FC-based ANPC converter are presented. The FC-based ANPC converter control strategy to control the FC voltage and generate the requested output voltage using a new modulation technique is discussed in Section III. In Section IV, the issues related to a single-phase grid-connected 5L-ANPC converter is discussed. The performance evaluation of the proposed system using simulation is investigated under different operating conditions in Section V. Section VI presents the results from experimental work and finally, conclusions are summarized in SectionVI.

II. FLYING CAPACITOR BASED ANPC CONVERTER OPERATIONAL PRINCIPLES

The phase-leg of the five-level FC based ANPC converter is shown in Fig. 1. The dc-link consists of two capacitors each of which is rated at half of the dc-link voltage. This topology requires a flying capacitor per phase, the voltage of which should normally be one quarter of the dc-link voltage to generate uniform step levels at the output phase voltage as shown in Fig. 2. The outer switches (S_1, $\bar{S}_1$) operate at a lower switching frequency and should be able to withstand twice the voltage of S_2 and S_3 switches. In low-voltage power applications, insulated gate bipolar transistors (IGBTs) could be utilized for the outer switches and lower blocking voltage MOSFETs with higher switching capability can be used for (S_2, $\bar{S}_2$) and (S_3, $\bar{S}_3$) switches as illustrated in Fig. 1. The operation of the switch pairs (S_1, $\bar{S}_1$), (S_2, $\bar{S}_2$) and (S_3, $\bar{S}_3$) are complementary.

The five-level FC-based ANPC converter consists of eight switching states which generate the different voltage levels at the output based on the capacitors voltages as shown in Table I. If the voltages across the dc-link capacitors are balanced and the voltage across FC is $V_{dc}/4$, five possible levels of the output voltage V_{ao} will be generated based on the different switching states as shown in Table I. In this case, some of the switching states are redundant in generating certain output voltage level. For example, V_6 and V_7 are redundant switching states to generate $V_{dc}/4$. Similarly (V_2, V_3) and (V_4, V_5) are redundant states to generate $-V_{dc}/4$ and 0 respectively. Although, the redundant switching states (V_2 and V_3), (V_6 and V_7) generate the same output voltage level, their affect on the FC voltage is opposite to each other due to the change in the direction of FC current. The ability to generate the same output voltage level with the opposite effect on FC voltage gives an opportunity to regulate the voltage across it. The rate of change of the voltage across FC can be expressed as:

$$\frac{d}{dt}v_{fc} = \frac{i_a}{C_{fc}}(S_2 - S_3) \tag{1}$$

where S_2 and S_3 are equal to '0' when the switch is OFF and equal to '1' when the switch is ON.

In some applications, because of the limitations of the size of the dc-link capacitors, the dc-link could experience voltage variations. For example, in single-phase grid-connected applications, the dc-link power can have second harmonic ripple that will cause second harmonic ripple across the dc-link capacitor voltage. Also, dc-link voltage variations could be caused by applications where an ac rectifier is used to provide the dc-link voltage for the converters.

Generally, the dc-link voltage can have voltage variations in steady-state, dynamic and transient conditions. In these conditions, capacitor voltages will not be symmetrical. (In this paper, a symmetrical condition is defined as $V_{C1} = V_{C2} = 2V_{Cf}$) This will result in V_{ao} having more than five different output voltage levels as illustrated in Table I. Further, the difference between the voltage levels are not equal. In this case, the switching states (V_2, V_3) and (V_6, V_7) would not produce the same voltage level and the effect of these different voltage levels must be considered in the switching time calculations for the generation of the required output voltage. The resulting different voltage levels are illustrated in Fig. 3(a) and (b) for balanced and unbalanced conditions respectively for a specific time-step. In a balanced condition, the reference for FC voltage is usually set to be $V_{dc}/4$. However in an unbalanced condition, the reference for the FC voltage needs to be investigated. It can play an important role to balance the average values of the dc-link capacitor voltages as well as to control the output voltage harmonics. Different control techniques and strategies can be used to determine the reference value of FC voltage depending on the applications. For example, the FC reference voltage can be a fixed value regardless of the dc-link voltage variations or can be $(V_{C1} + V_{C2})/4$ or a value that can satisfy the application requirements.

III. Proposed Modulation Technique with FC Voltage Controller for Five-Level FC based ANPC Converter

In this paper, a novel modulation technique is proposed to determine the appropriate switching states to be selected to generate the requested output voltage as well as controlling the FC voltage to the requested FC voltage during a sampling time both for balanced and unbalanced conditions. Adding FC reference voltage accompany with output reference voltage as input of the modulator which is able to follow them in variable and unbalanced dc-link voltage condition, will improve controlling ability of the five-level ANPC inverter system to be applied in variety of applications.

A. Basic Concept of the Averaging Technique

Generally, the average value of the output voltage, v_{o_s}, in each sample time T_s, can be expressed as in (2), which forms the basis of the modulation technique.

$$v_{o_s} = \frac{1}{T_s}\int_0^{T_s} v_{ao}(t)dt \tag{2}$$

In (2), $v_{ao}(t)$ is the output switching voltage. Fig. 4 shows the reference requested waveform (v_{ref}) lies between two voltage levels v_{lvlx} and v_{lvly} and the resulting output voltage tracks the reference waveform based on (1). For illustration purposes,

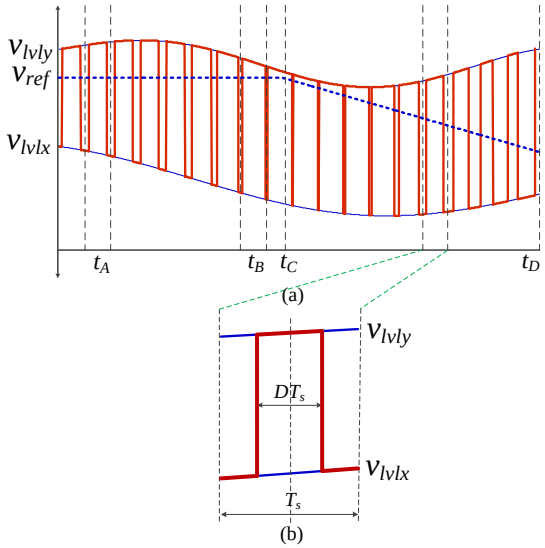


Fig. 4. Applying variable nearest voltages to generate PWM voltage to track the reference voltage

the reference requested waveform (v_{ref}) shown in Fig. 4 is assumed to be constant until t_C and then decreases linearly until t_D.

If the capacitor sizes are large enough, even though there is a voltage fluctuation across the capacitors, the changes in the capacitors voltage during a sample time are assumed to be so small that they can be neglected. Applying this assumption, the variations in the voltage levels v_{lvlx} and v_{lvly} shown in Fig. 4(b) are neglected and assumed to be v_{lvlx_s} and v_{lvly_s} during T_s. Therefore, (2) can be simplified to (3).

$$\begin{aligned} v_{ref_s} &= v_{o_s} = \frac{1}{T_s}\int_0^{T_s} v_{ao}(t)dt \\ v_{o_s} &= (1-D_s)v_{lvlx_s} + D_s v_{lvly_s} \end{aligned} \tag{3}$$

Generally, in order to generate v_{ref_s} from two different voltage levels v_{lvlx_s} and v_{lvly_s} in a specific duration time, the duty-cycle (D_s) can be determined from (3) as shown in (4).

$$D_s = \frac{v_{ref_s} - v_{lvlx_s}}{v_{lvly_s} - v_{lvlx_s}} \tag{4}$$

Fig. 4 illustrates the changes in the duty-cycle for different operating conditions. For example to generate the required output voltage during the time periods t_A and t_B, the duty-cycle is varied depending on the chosen voltage levels, v_{lvlx} and v_{lvly}, even though in this case, v_{ref} is a constant value.

B. Proposed Modulation Technique with FC Voltage Control

From Section III-A, the averaging method can be implemented to obtain the requested output voltage in a Five-level ANPC inverter. In Section II, the operational principles of a five-level FC based ANPC converter have been discussed for different voltage values across the three capacitors. In the symmetrical condition, the five different voltage levels can be utilized to generate the requested output voltage where some of them have redundancy in the switching state selection. For example when the output reference voltage is between $V_{dc}/4$ and $V_{dc}/2$, the switching states V_6 and V_8 or V_7 and V_8 can

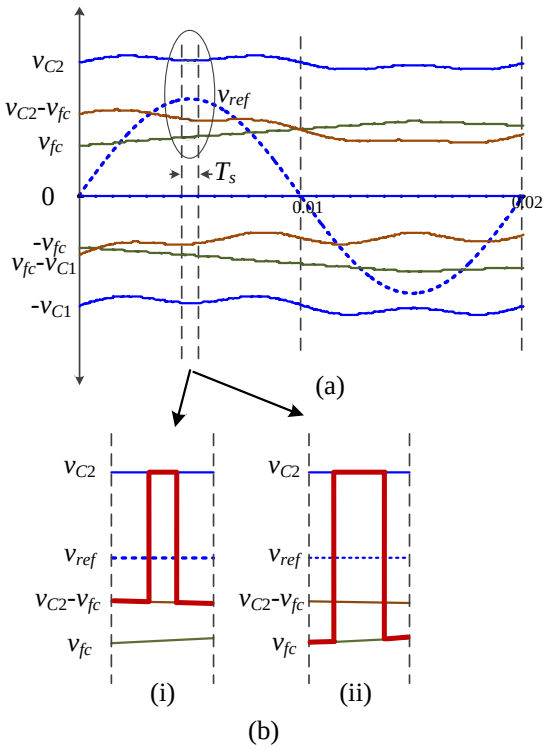


Fig. 5. (a) Applicable voltage levels to implement requested output voltage during a period under varying dc capacitor voltages (b) effect of selection of different voltage level on duty cycle during a special time-step to have same reference output voltage

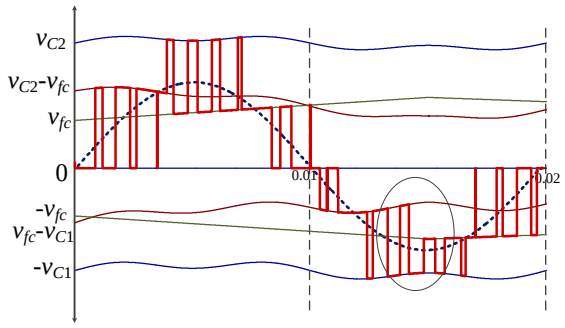
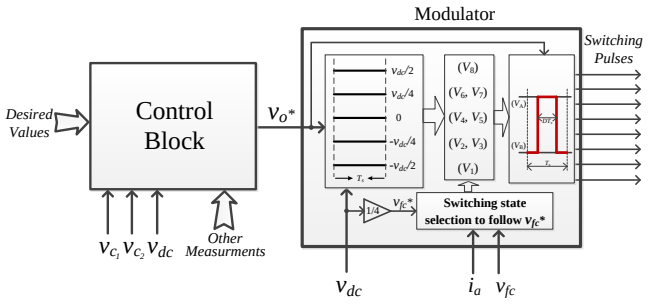


Fig. 6. Modulator selection of the appropriate voltage level under varying dc capacitor voltages to generate a sinusoidal output voltage



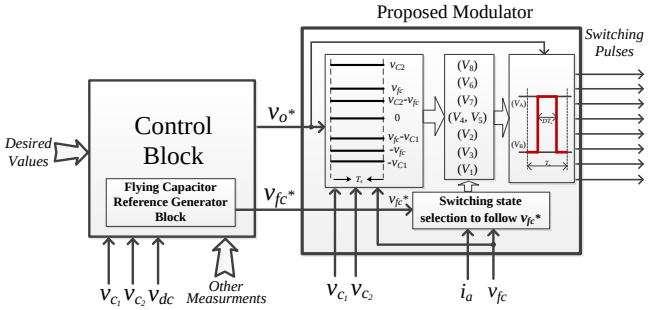


Fig. 7. (a) Control system diagram using conventional modulation technique, (b) system control diagram using proposed modulation technique

be utilized. To select which of these is to be used (V_6 or V_7), the main objective is to reduce the difference between the reference and the actual FC voltage. Based on (1), to regulate the FC voltage, the polarity of the output current must be considered in selecting the switching states V_6 or V_7. When the polarity of the output current is positive, the selection of V_6 will cause the FC to be discharged and hence the voltage will be reduced while the selection of V_7 will cause the FC to be charged and hence the FC voltage will be increased.

Traditionally, the modulator only requires the output reference voltage as an input and the FC voltage is assumed to be regulated to $V_{dc}/4$ and during switching selection in the modulator, the dc-link capacitors are assumed to be balanced. However, in general, the value of the reference FC voltage has to be taken into account as described in Section II for balanced and unbalanced dc-link voltages. Therefore the modulator should have an additional input in the form of the reference FC voltage. This approach provides an improvement to the ability of the modulator and more flexibility for the control system.

Fig. 5(a) shows an operating condition where the capacitor voltages are fluctuating and unbalanced. During the time step, T_s, shown in Fig. 5(a), seven different voltage levels are available to generate the required output voltage. Based on the averaging technique, the two nearest appropriate voltage levels need to be utilized to generate the requested output voltage. In this case, the voltage level V_{C2} is one of the appropriate nearest voltage levels. Even though the voltage level $(V_{C2} - V_{fc})$ is also one of the nearest voltage levels, it may not be the appropriate voltage level to select. A rule to determine the selection of the appropriate voltage level can be based on the effect it has on the FC voltage. For example, during a certain time step, if the actual FC voltage is less than the reference voltage, then the FC must be charged by selecting the appropriate switching state using (1). In (1), if the output current (i_a) is positive, the selection of the voltage level $(V_{C2} - V_{fc})$ will cause FC to be charged and if it is negative, the selection of voltage level (V_{fc}) will cause FC to be charged. Therefore, depending on the sign of (i_a), either the voltage level $(V_{C2} - V_{fc})$ or the voltage level (V_{fc}) need to be selected. The effect of the selection to generate the required output voltage will cause the duty cycle to be varied as shown in Fig. 5(b). Fig. 6 shows the modulator selection of the appropriate voltage level under varying dc capacitor voltages to generate a sinusoidal output voltage for a particular reference FC voltage and output current.

C. Modulator and Control Block Implementation

Fig. 7 shows the control system diagram consisting of the control block and the modulator. Two systems are compared, one with the conventional modulator, and the other with the proposed modulator. As shown in Fig. 7(b), the proposed modulator can consider unsymmetrical condition in the capacitor voltages to generate the requested output voltage. In this case, the FC voltage can be decoupled from the output voltage and then the modulator can accept a new input reference value for FC voltage. Using FC reference voltage as an input of modulator adds an additional freedom to control the system, whereas, in the conventional methods, the control block, can only produce and change the requested output voltage of the converter and the FC voltage is regulated to $V_{dc}/4$. This new feature in the proposed modulator is used to achieve balanced dc-link capacitor voltages of the converter in a single-phase application and will be further discussed in the next Section.

IV. Single-Phase Grid Connected Five-Level ANPC Photovoltaic System

A single-phase grid-connected PV system using a five-level ANPC inverter has the advantage of having high quality output voltages by using an optimal number of low voltage switches. One of the important issues in single phase application is the dc-link capacitor voltage ripple and balancing. In a three-phase three-wire application, the dc-link capacitor voltage balancing can be achieved by controlling the zero-sequence voltage of the inverter. But in the single-phase structure, because of effect on the output voltage, this technique is not applicable and in this case, the control of the flying capacitor voltage can play an important role in solving the problem.

A. Power and voltage ripple in the capacitors

Fig. 8 shows a single-phase grid-connected PV system using a five-level ANPC inverter. To analyze the system behaviour under steady-state conditions, it is assumed that the inverter operates with unity power factor with low current THD. Under these conditions, the grid voltage and the inverter current are given by (5) and (6) respectively:

$$v_s = V_m \sin(\omega t) \tag{5}$$

$$i_s = I_m \sin(\omega t) \tag{6}$$

The power transmitted to the ac grid voltage is:

$$\begin{aligned} p_s &= v_s i_s = V_m I_m \sin^2(\omega t) \\ &= \frac{V_m I_m}{2} - \frac{V_m I_m}{2}\cos(2\omega t) \end{aligned} \tag{7}$$

and then inverter ac side power is:

$$\begin{aligned} p_{out} &= v_{out} i_s = (v_s + L_s di_s/dt) i_s \\ &= \frac{V_m I_m}{2} - Pr_m \cos(2\omega t + \phi) \end{aligned} \tag{8}$$

where

$$\phi = \arctan(L_s \omega I_m / V_m); Pr_m = \frac{I_m}{2}\sqrt{V_m^2 + (L_s \omega I_m)^2}$$

Based on (7) and (8), the power transmitted to the grid and power transferred from the ac side of the inverter have the same dc value but different ac value. To investigate the operation requirements of the modulator and the control system, the dissipation of the inverter is assumed to be neglected and the PV modules and the maximum power point tracker (MPPT) circuit are assumed to transfer dc power to the dc side of the inverter, where the value is dependent on the PV modules and the sun irradiation. Therefore, when the system is in a stable condition, the output power from the PV modules with MPPT circuit, P_{PV}, shown in Fig. 8 must be equal to the dc part of p_{out} which is $V_m I_m/2$. If the inverter dissipation is neglected, the difference between p_{out} and P_{PV} must cause the three capacitors of the inverter C_1, C_2 and C_f to experience power ripple. The power ripple in a capacitor will produce voltage ripple across the capacitors as given in (10).

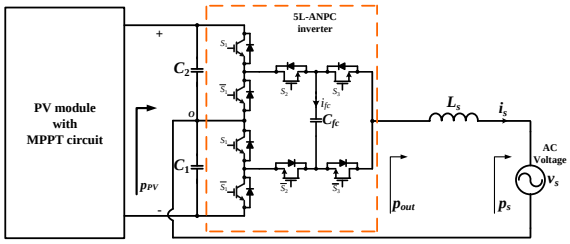


Fig. 8. A single-phase grid-connected PV system using Five-level ANPC converter

$$\frac{dW_{C_i}}{dt} = \frac{d}{dt}\left(\frac{1}{2}C_i v_{C_i}^2\right) = p_{C_i} \tag{9}$$

$$dv_{C_i} = p_{C_i}\frac{dt}{C_i v_{C_i}} \tag{10}$$

This voltage ripple in the dc voltage of the capacitors in the conventional modulator will cause harmonics in the inverter output voltage. Furthermore, it can cause unexpected behavior on the control system action. One solution to reduce the ripple magnitude of the capacitor voltages is to increase the size of the capacitors. This will result in increased cost, size and weight of the system. Further it cannot solve completely the issues related to voltage ripple and also any transient on the capacitor voltages can produce unexpected transient on the output voltage and the system behaviour.

Also, in the grid-connected, single-phase five-level ANPC system, power ripple will not be shared between the capacitors simultaneously. As shown in Table I when the output voltage is positive, C_2 is transferring power to the output and when the output voltage is negative, C_1 is transferring the power, however, during the whole period, both capacitors are involved in receiving power from the PV circuit. Therefore, not only the dc-link capacitors have voltage ripple problems because of their power ripple, but also they have different timing in their ripples which can produce instantaneous unbalancing of dc-link voltages. To reduce the effect of the dc voltage ripple on the output waveform, the proposed modulation technique in Section III can be used.

However, two issues still need to be considered; first is the phenomena of the possible divergence of the dc-link capacitor voltages. Second is the selection of the FC voltage reference and its effect on the system.

B. Investigation On Instability and Inherent Stability in the dc-link Voltages in Single-phase Three-level and Five-level ANPC Inverters Using Power Transmission Concept

The unbalance in the dc-link capacitor voltage can be caused by issues such as the tolerance in the capacitor values, leakage currents, unequal switching losses, unsymmetrical switching, any transients in the system, unsymmetrical ac side current or improper control strategy.

The divergence of the dc-link voltage can be one of the major problems in a multi-level inverter. As discussed before, in three-phase applications several techniques are introduced in literature to have balancing in the dc-link capacitors. A common method to solve the balancing issues in the three-phase application is adding the zero-sequence voltage to the output voltages of the three-phase inverter which will not affect their line voltages. But this cannot be applied in single-phase applications. Thus, the divergence of the dc-link voltages can be one of the major problems in single-phase five-level ANPC inverters. It can also similarly be a problem for a single-phase three-level inverters.

To explain the phenomena and explain power transmission concept more easily, a grid-connected three-level NPC inverter is first discussed. Then based on the concept explained in the three-level inverter, the idea can be expanded to five-level FC based inverters.

In the three-level NPC inverter, two capacitors C_1 and C_2 in Fig. 9 are involved in the power transmission activity. The average power transmitted from the dc-side P_{dc} to the ac-side is the sum of P_1 and P_2. The power P_1 is related to the power transmitted to the ac-side through the capacitor C_1 which occurs during one half-cycle of the inverter output voltage and P_2 is related to the other half-cycle of the inverter output voltage when the power is transmitted through C_2. In the normal steady-state operation, regardless of the capacitors voltage, P_1 and P_2 must be equal to have two symmetrical half-cycle currents. Therefore, under any balanced or unbalanced dc-link voltage or transient conditions, the modulator must produce a symmetrical output voltage to ensure sinusoidal current in the ac side. However, traditional modulators will normally assume balanced dc-link capacitor voltages to produce the symmetrical output voltage. If the capacitor voltages are unbalanced, an unsymmetrical output voltage will be produced, depending upon to the values of the unbalanced capacitor voltages. This behaviour will produce distortion in the ac side current, however this can help to produce inherent dc-link balancing ability, because when the capacitor with the higher voltage transfers higher power to the output, the capacitor voltage will automatically decrease more than that of the capacitor with the lower voltage.

But if the modulator is designed to produce a symmetrical output voltage in an unbalanced dc-link voltage condition (V_{C1} not equal to V_{C2}), P_1 and P_2 will be equal and hence I_{C1} and I_{C2} will be different. If the input current from the dc-side is considered to be constant during the period, the capacitor with the higher voltage will now have lower average output current compared to the capacitor with the lower voltage. This will lead to the divergence of the two capacitor voltages, with the voltage of the higher voltage capacitor increasing higher and higher and the voltage of the lower voltage capacitor decreasing lower and lower.

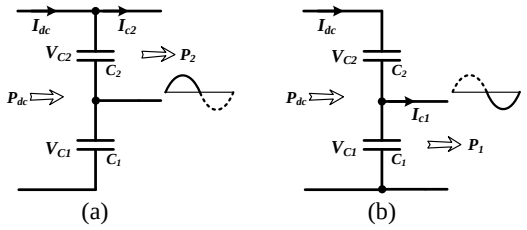


Fig. 9. Power transmission interaction of dc-link capacitors during two half-cycles of the output voltage period for a three-level inverter or a five-level inverter with constant FC voltage

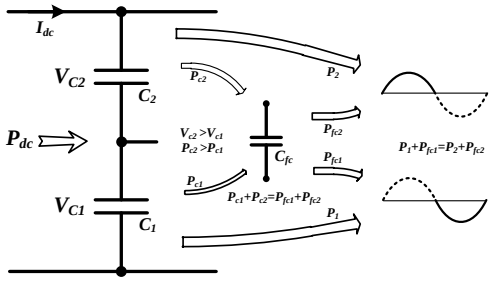


Fig. 10. Power transmission interaction of dc capacitors during two half-cycles of the output voltage period for a five-level inverter to control dc-link balancing and having symmetrical output voltage

This phenomena can also occur in a single-phase five-level ANPC inverter when the FC voltage is controlled to be a constant value and acts only as an intermediary for the power transfer from the dc-link capacitors to the ac side of the inverter.

Fig. 10 shows the power flows of a single-phase five-level ANPC inverter where V_{C2} is greater than V_{C1}. To produce a symmetrical output voltage, $P_2 + P_{fc2}$ must be equal to P_1+P_{fc1}. Since the FC voltage is controlled to have a constant value, during the positive cycle of the output voltage, P_{fc2} is equal to P_{c2} and during next half-cycle, P_{fc1} is equal to P_{c1}. Therefore, $P_2 + P_{c2}$ (from capacitor C_2) must be equal to $P_1 + P_{c1}$ (from capacitor C_1). Hence, similar to the single-phase three-level inverter, there will be divergence in the two capacitor voltage values.

However, in single-phase or three-phase applications of a five-level ANPC inverter, it is possible to take advantage of the flying capacitor to control the balancing of the dc-link capacitors, if the FC voltage does not have to be controlled to a constant value and the FC is allowed to be charged or discharged as required during a cycle of the output voltage. To control the voltage balance in the dc-link capacitors, the capacitor C_2 should transfer higher power ($P_2 + P_{c2}$) than that from the capacitor C_1 ($P_1 + P_{c1}$) to reduce the voltage unbalance in the dc-link capacitors. This can be achieved by not controlling the FC voltage to a constant value. P_{c2} can be controlled to be higher from P_{fc2} causing the FC voltage to rise. The excess power stored in the FC can be used in the next half-cycle to help C_1 to generate the output power (P_1+P_{fc1}), which causes the FC voltage to reduce to its original value at the end of the cycle. In this way, the capacitor C_2 will transfer higher power than capacitor C_1 leading to the desired voltage balance in the dc-link capacitors.

This can be implemented by the new modulator which can

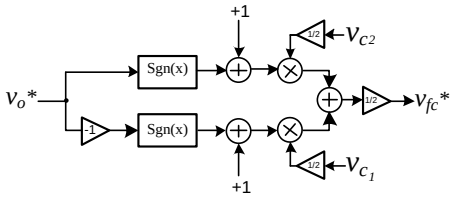


Fig. 11. Flying capacitor reference generator diagram

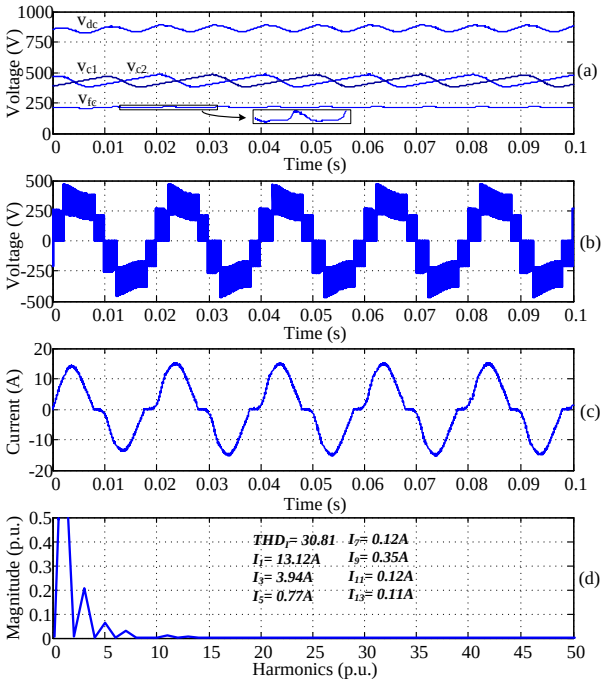


Fig. 12. Results of applying conventional modulation technique with dc-link capacitors equal to 300 μF: (a) dc-link voltage, dc-link capacitors voltages and FC voltage (b) inverter output voltage (c) inverter output and ac grid current (d) magnitude of current harmonics (pu).

control the output voltage to be symmetrical regardless of the values of capacitor voltages. In this paper, we propose that the FC reference voltage of the new modulator has to be selected to follow $V_{C2}/2$ during the positive cycle of the output reference voltage and then to follow $V_{C1}/2$ during the negative cycle of the output reference voltage. In the balanced dc-link voltage condition when V_{C1} is equal to V_{C2} then the defined reference voltage for FC will be equal to $V_{dc}/4$. Based on this technique, Fig. 11 shows the control diagram to generate the FC reference voltage. It is used in the "Flying Capacitor Reference Generator Block" presented in Fig. 7(b).

V. Performance Evaluation and Simulation Results

A simulation has been carried out using MATLAB/Simulink to verify the effectiveness of the proposed modulator and control technique for the five-level ANPC inverter application for a single-phase grid-connected PV system. The simulation is based on Fig. 8 and it is assumed that the PV modules and the MPPT circuit transfer a constant power to the dc-side of the inverter regardless of the variation on the dc-link voltages of the inverter, assumed to be between 700 V to 1000 V. The value of transferred power from the MPPT circuit is dependent

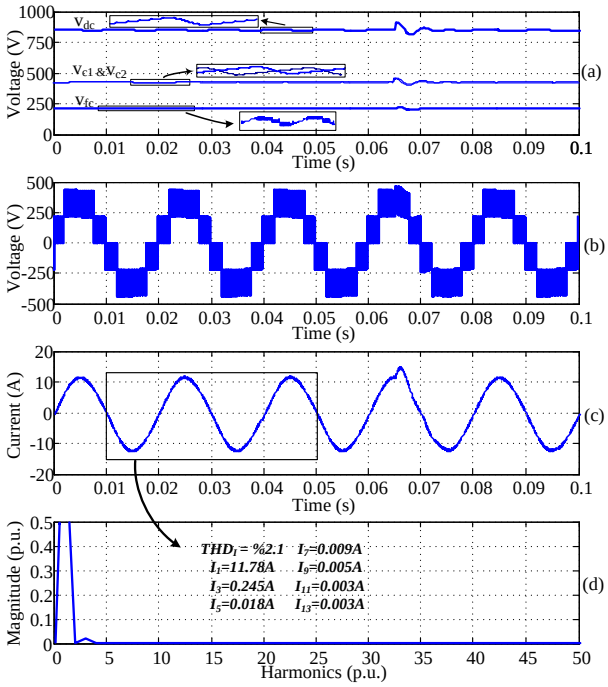


Fig. 13. Results of applying conventional modulation technique with dc-link capacitors equal to 3 mF: (a) dc-link voltage, dc-link capacitors voltages and FC voltage (b) inverter output voltage (c) inverter output and ac grid current (d) magnitude of current harmonics (pu).

on the power available from the PV and can vary for different solar irradiation. During the 100 ms simulation, it is considered to be constant and equal to 2 kW. In Fig. 8, the ac grid voltage (V_s) is 240 V and the series inductor L_s is 4.8 mH. The control system which will be discussed further at the end of this section, is designed to transfer the PV power to the ac grid with unity power factor. The simulations have been carried out for both the conventional and the proposed modulator with different values of dc-link capacitors. To investigate the effectiveness of the proposed modulator and control strategy on balancing of the dc-link capacitor voltages, the simulations are carried out using a constant value of FC reference voltage as $V_{dc}/4$ and using the proposed technique of setting the reference FC voltage as $V_{C2}/2$ during the positive cycle of the output reference voltage and as $V_{C1}/2$ during the negative cycle of the output reference voltage. The flying capacitor value is 500 μF. The sample time (T_s) is 50 μs representing a 20 kHz output switching frequency.

Fig. 12 shows the simulation results of the system using the conventional multi-carrier modulation technique to generate the inverter switching signals. The conventional modulator applies the average of the dc voltage to generate a per-unit reference waveform to be applied for the conventional modulation technique. To investigate the effect of the value of the capacitor, initially the dc-link capacitor values are set as 300 μF to examine the quality of the output voltage and inverter current using a small dc-link capacitors. The FC reference voltage in the simulation is set equal to one-quarter of the dc-link voltage. Fig. 12(a) shows the dc-link voltage V_{dc}, the dc-link capacitor voltages V_{C1} and V_{C2} and the flying capacitor voltage V_{fc}. Fig. 12(a) shows that the voltage of V_{dc} varies by around 100 V and the variation of

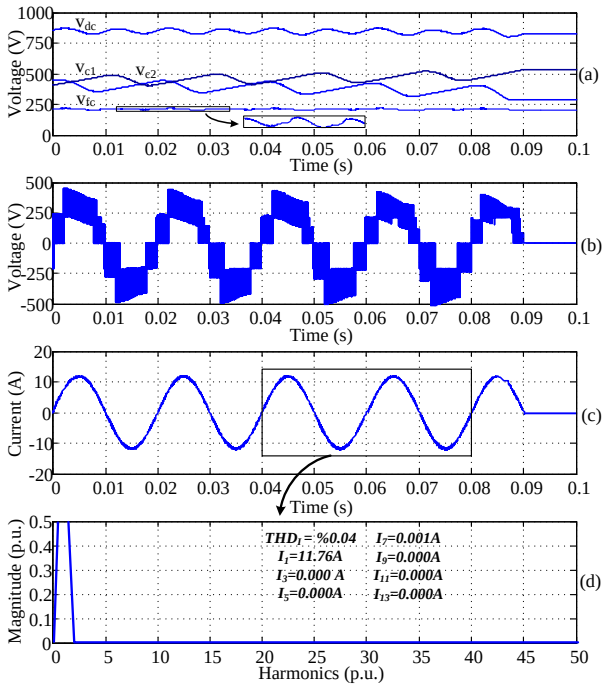


Fig. 14. Results of applying proposed modulation technique with dc-link capacitors equal to 300 μF and FC reference voltage equal to $V_{dc}/4$: (a) dc-link voltage, dc-link capacitors voltages and FC voltage (b) inverter output voltage (c) inverter output and ac grid current (d) magnitude of current harmonics (pu).

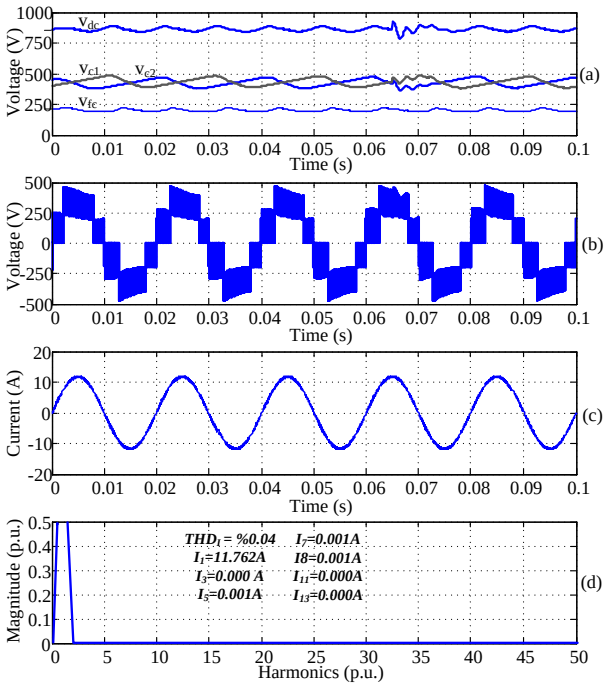


Fig. 15. Results of applying proposed modulation technique with dc-link capacitors equal to 300 μF and FC reference voltage equal to half of engaged dc-link capacitor in each output half-cycle: (a) dc-link voltage, dc-link capacitors voltages and FC voltage (b) inverter output voltage (c) inverter output and ac grid current (d) magnitude of current harmonics (pu).

each dc-link capacitor voltage is around 150 V, which is a significant variation. Fig. 12(b) shows the five-level output of the inverter voltage waveform where each output level follows the variation in the dc capacitor voltages accompanied by the high frequency switching pulses. Fig. 12(c) shows the inverter output current which contains harmonics due to the ripple in the dc capacitor voltages shown in Fig. 12(a). The spectrum of the inverter current harmonics is shown in Fig. 12(d), showing that most of the harmonics of the inverter current are 3rd, 5th and 7th and the total harmonic distortion (THD) is 30.81%, which is quite significant.

The traditional solution to reduce the dc voltage ripple problem is to increase the size of dc-link capacitors. This will result in the improvement of the output current quality. To test this, the dc-link capacitor values are both now increased to 10 times their original value (3000 μF). Fig. 13 illustrates the results of the simulation using the same modulation technique and FC reference voltage as in the previous simulation. Fig. 13(a) shows the dc-link voltage V_{dc}, the dc-link capacitor voltages V_{C1} and V_{C2} and the flying capacitor voltage V_{fc}. Fig. 13(a) shows that the variations in all voltages are reduced. To demonstrate that there is still ripple in the capacitor voltages, a small section of each graph is zoomed to show this. Fig. 13(b) shows the five-level inverter output voltage waveform showing that the reduced variation in the capacitor voltages are reflected in the reduced variation in each output level. Fig. 13(c) shows the inverter current with improved waveform quality and reduced harmonic content as shown in Fig. 13(d) where the THD is now only about 2.1% and third harmonic current magnitude is about 2.07% and the other harmonic currents are negligible in value. However, any transient in the dc-link capacitor voltages, as shown in Fig. 13(a) at t = 65 ms can cause the inverter current in Fig. 13(c) to be distorted and therefore have higher harmonic content.

To demonstrate the effectiveness of the proposed modulator to reduce the effect of the dc voltage ripple on the output current waveform, the dc-link capacitors are returned back to the lower value of 300 μF and the FC reference voltage is set to be equal to one-quarter of the dc voltage. Fig. 14(a) shows the dc voltage V_{dc}, the dc-link capacitor voltages V_{C1} and V_{C2} and the flying capacitor voltage V_{fc}. Fig. 14(a) shows that V_{dc} still varies by around 100 V as before. Fig. 14(b) shows the five-level output of the inverter voltage waveform where each output level follows the variation in the dc capacitor voltages accompanied by the high frequency switching pulses as previously, however the inverter output voltage has been modified in its switching time as discussed in Section III-A. This will result in a less distorted inverter output current as shown in Fig. 14(c), and much reduced harmonic content and THD as shown in Fig. 14(d) where the THD of inverter current is now only 0.04%. However, Fig. 14(a) also shows that the average voltage of Vc_1 is increasing while the average voltage of Vc_2 is decreasing which indicates that the system has dc-link voltage divergence problem as was expected based on section IV. When the divergence reaches an unacceptable level, after 90 ms, the control system turns the inverter off.

To demonstrate the effectiveness of the proposed method of varying the reference FC voltage in the the modulator to solve the problem of capacitor voltage divergence in the previous simulation, the dc-link capacitors remain at their low value 300 μF and the FC reference voltage of the new modulator has to be selected to follow $V_{C2}/2$ during the positive cycle of

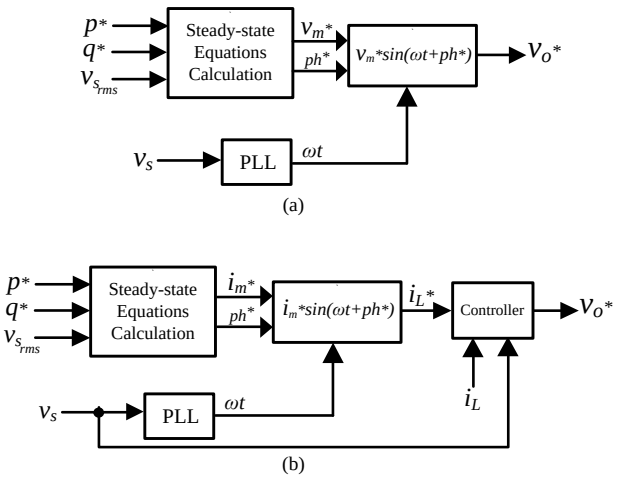


Fig. 16. Control techniques to generate reference voltage: (a) simple steady-state technique (b) current control based technique

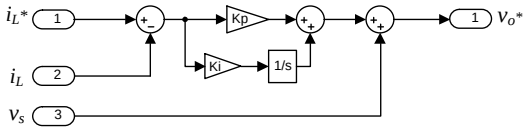


Fig. 17. PI controller and decoupling source voltage

the output reference voltage and then to follow $V_{C1}/2$ during the negative cycle of the output reference voltage as given in Section IV-B. Fig. 15(a) shows the dc voltage V_{dc}, dc-link capacitors voltages Vc_1 and Vc_2 and the flying capacitor voltage V_{fc}. Fig. 15(a) shows that V_{dc} still varies by 100 V as before, however the divergence problem has now been solved, while achieving a clean current waveform as shown in Fig. 15(c). Fig. 15(d) shows that the THD is very good and is around 0.04%. Further, a transient in the dc-link capacitor voltages as shown in Fig. 15(a) at t = 65 ms does not cause the inverter current in Fig. 15(c) to be distorted.

Several algorithms can be used for the "Control Block" presented in Fig. 7(b) that can be designed to improve performance in the transient response or to make the system to be less sensitive to the component values or to be less sensitive to harmonics and noise, or to be less sensitive to the measurement

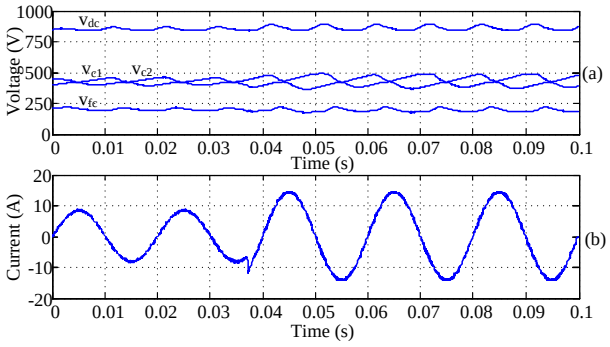


Fig. 18. Results of applying proposed modulation technique with proposed FC reference voltage with having step power in the PV and transmission power to the grid at t= 37ms: (a) dc-link voltage, dc-link capacitors voltage and FC voltage (b) inverter output and grid current

accuracy. This is a big topic by itself and it is beyond the scope of this paper.

However, as a brief description, the control blocks used in the study are shown in Fig. 16(a) and 16(b) which have been applied to control the single-phase grid connected system.

Fig. 16(a) used a simple technique to determine the inverter output reference voltage by using steady-state system equation calculations in (11).

$$P = (V_o V_s / X_L) sin(Ph); Q = V_s(V_I cos(Ph) - V_s)/X_L \quad (11)$$

where P and Q are the active and reactive power transmitted to the grid, V_o and V_s are the inverter and grid voltage, and ph is phase between the inverter voltage and grid voltage.

This voltage reference generation method was applied for both modulator and the results are shown in the previous four simulations.

The current control technique, which is less sensitive to the grid harmonics, is used in Fig. 16(b) to control the inverter current. The inverter output reference voltage is produced by the controller box shown in Fig. 16(b). It used PI and decoupling control techniques which are shown in Fig. 17. The current control technique is applied for the conventional and the proposed modulation techniques. However, when it is applied in the conventional modulation, by increasing gain of the current controller and improving the quality of the output current, divergence problem will occur as discussed in section IV. By reducing the speed of current controller to have average balancing in the dc-link capacitor voltages, the result will be similar to the results using Fig. 16(a) controller.

The current control technique is applied to the new modulator using the the control diagram to generate FC reference voltage shown in Fig. 11 and using kp = 45 and ki=120000. The technique works properly and the results are very similar to the simulation shown in Fig. 15.

Fig. 18 shows the transient behaviour of the system using the current control technique with proposed modulator and applying presented balancing control strategy. In the simulation, the PV generation is changed from 1.4 kW to 2.4 kW at $t = 37ms$ resulting in the change in the reference current magnitude. As shown in Fig. 18, the inverter current follows the requested current properly and quickly, while the ripple of dc-link capacitors (shown in Fig 18(a)) is increased after the step change.

VI. Experimental Results

Experimental tests have been conducted based on the configurations presented in Fig. 19(a) and (b) to test the new modulation technique and balancing control strategy. Fig. 19(a) shows a stand-alone Five-level FC based inverter connected to an inductor and a resistive load connected in series and Fig. 19(b) shows a grid connected five-level FC based inverter.

A prototype system based on the configurations in Fig. 19(a) and (b) is implemented in the laboratory as shown in Fig. 20 in order to to examine the ability of the proposed modulation technique and the balancing control strategy for a five-level FC based inverter. The system includes an inverter board and its measurement circuit, an ac measurement board, a dc measurement board and a control board as shown in Fig. 20. The measurement boards and the control board are designed

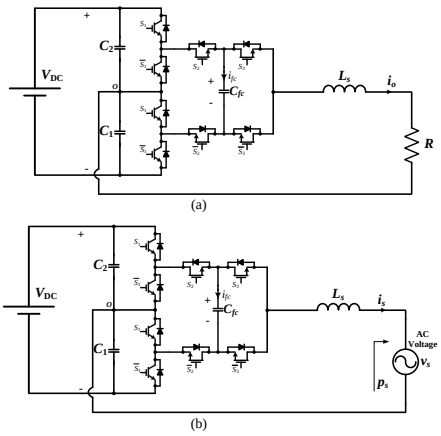


Fig. 19. Experimental system configurations (a) using resistive load (b) grid-connected system

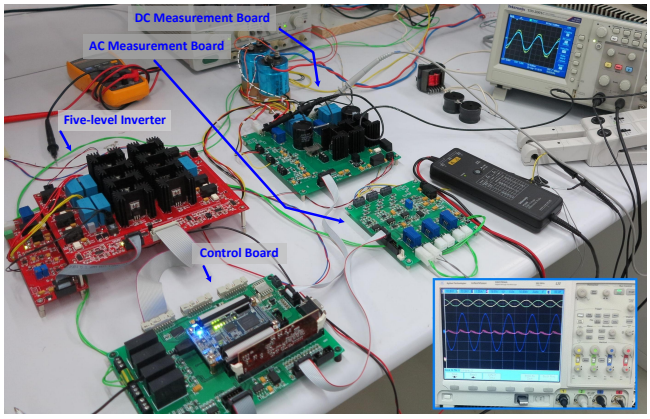


Fig. 20. Experimental setup

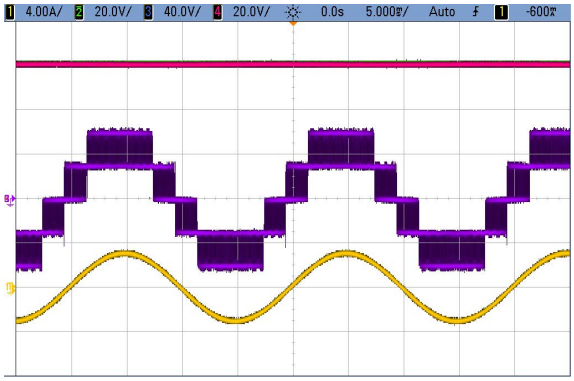


Fig. 21. Experimental result using high value of dc-link capacitors with R = 16 Ω load based on configuration in Fig. 19(a): dc-link capacitors voltages, inverter output voltage, inverter current

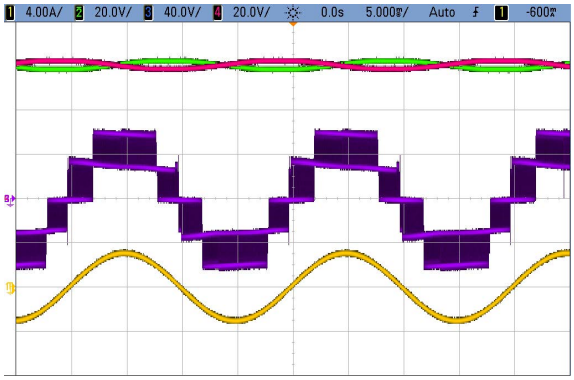


Fig. 22. Experimental result using low value of dc-link capacitors with R = 16 Ω load based on configuration in Fig. 19(a): dc-link capacitors voltages, inverter output voltage, inverter current

for a three-phase application, however in this research, they are used and programmed for a single-phase application. The control board uses a combination of the Texas Instruments TMS320F28335 control card and the Altera Cyclone IV EP4CE22F17C6N FPGA card to provide powerful real-time mathematical calculations and control functions.

Initially, the tests were conducted based on the configuration presented in Fig. 19(a) by using a 120 V dc source voltage, a 2.1 mH inductor and a 470 μF flying capacitor. Figures 21 and 22 show the inverter output voltage and current waveforms using a 16 Ω resistor and using two different values for the dc-link capacitors, one with 11200 μF and the other with 1200 μF respectively, to generate 34 V_{rms} output voltage. The results show that the dc ripple voltage will be increased by reducing the dc-link capacitors and it can be observed that, by using the proposed modulation technique, the output voltage and subsequently its current is not affected. Figure 23 shows the test results to generate a similar output voltage when 1200 μF dc-link capacitors and a lower value resistor (R = 8.8 Ω) are used. The results show that the dc-link voltage ripple increases by reducing the resistance or increasing the inverter current. Even with such an increase in the dc-link voltage ripple, the quality of the inverter current is not affected as shown in 23.

It is important to note that the balancing control strategy presented in this paper is used in the experimental work. As described in Section IV-B, a good quality output with a constant dc voltage across the flying capacitor will cause divergence in the dc-link voltages in a single-phase application. Figure 24 shows the inverter output voltage and current waveforms using the proposed modulation technique when the FC voltage is held constant and equal to $V_{dc}/4$. The results show that the inverter has a dc-link divergence problem, however because of the use of the proposed modulation technique, the inverter current is not affected by this problem while the voltages of the capacitors remain in an acceptable range. Unequal dc-link voltages will be compensated by using different pulse widths in the inverter output voltage. Figure 25 shows the capacitor voltages and the inverter output voltage and current waveforms using the proposed balancing control technique. The results show that the divergence problem in the dc-link capacitors is solved by using the proposed balancing control strategy and any initial unbalance or different leakage in the dc-link capacitors will be compensated by using the proposed balancing control strategy. It should be noted that, although the system has average balancing in the dc-link voltages, because of the ripple in the dc-link capacitor voltages, most of time, the system is working under instantaneous unbalancing condition. Figures 24 and 25 also verify that while there is transient in the dc-link capacitor voltages, proper output voltage will be generated by using the proposed modulator.

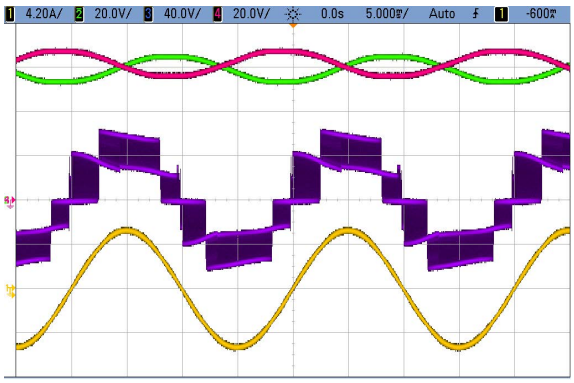


Fig. 23. Experimental result using low value of dc-link capacitors with R = 8.8 Ω load based on configuration in Fig. 19(a): dc-link capacitors voltages, inverter output voltage, inverter current

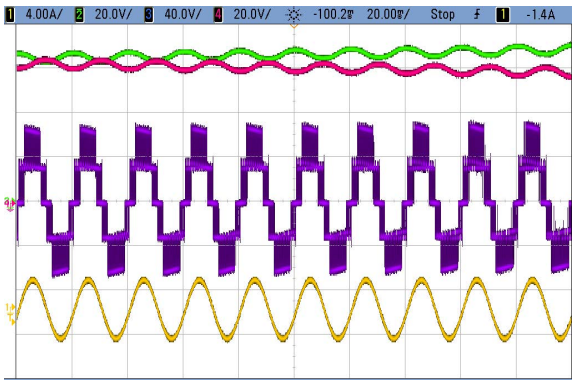


Fig. 24. Experimental result based on configuration in Fig. 19(a) using new modulation technique without having balancing control strategy (fixed reference value for FC voltage): dc-link capacitors voltages, inverter output voltage, inverter current

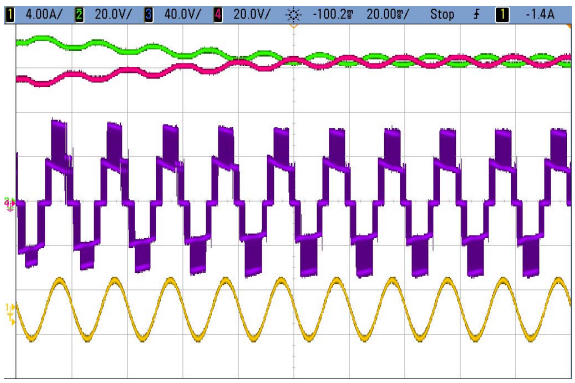


Fig. 25. Experimental result based on configuration in Fig. 19(a) using new modulation technique with having balancing control strategy: dc-link capacitors voltages, inverter output voltage, inverter current

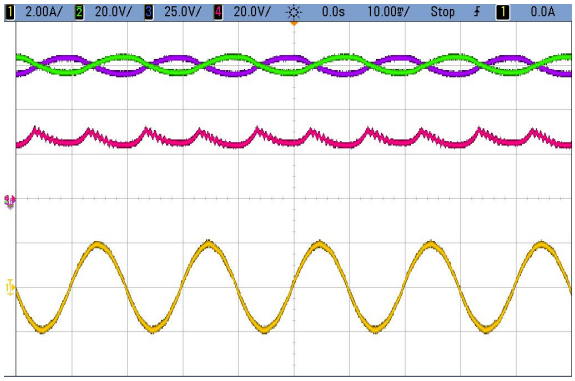


Fig. 26. Experimental result based on configuration in Fig. 19(b) using new modulation technique with having balancing control strategy: dc-link capacitors voltages, flying capacitor voltage, inverter current

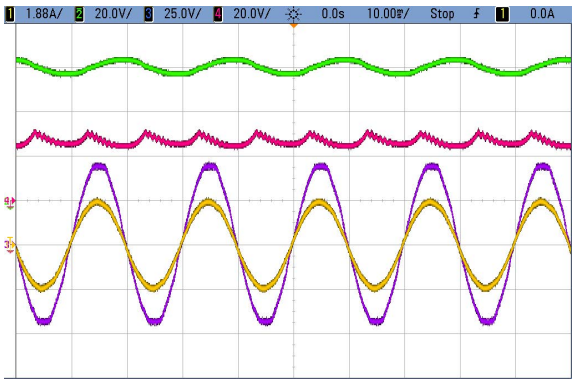


Fig. 27. Experimental result based on configuration in Fig. 19(b) using new modulation technique with having balancing control strategy: one dc-link capacitor voltage, flying capacitor voltage, ac source voltage, inverter current

Another test is conducted using the configuration presented in Fig. 19(b), similar to the system presented in the simulation section. In this test, a single dc supply is used as a source of energy to be transferred to the grid. For this configuration, the control board firmware and system connection are configured to produce a sinusoidal ac inverter current with unity power factor to transfer power from the dc source to the grid. The ac voltage source shown in Fig. 19(b) is the output of a transformer with ratio (240:35), the input of which is connected to the 240 V single-phase grid voltage.

As described in Section IV-A, in each half-cycle, one capacitor is involved in transferring power from the dc source to the ac side of the inverter, which will cause the dc-link capacitors to have ripple in their voltages, as shown in Fig. 26. The inverter current, the dc-link capacitor voltages and the FC voltage waveforms are shown Fig. 26. Fig. 26 shows that the implementation of the balancing control strategy can produce the average balancing in the capacitor voltages. The FC voltage tries to follow the desired dc-link capacitor voltage in each half-cycle to achieve the dc-link average voltage balancing.

Figure 27 shows the lower dc-link capacitor voltage V_{C1}, the grid voltage(V_s) and the inverter current waveforms. Fig. 27 shows that the inverter produces a good quality current waveform, which is in-phase with the grid voltage even though the grid voltage has relatively poor power quality shown by the flattish peaks of the voltage waveform.

VII. Conclusions

A novel modulation and control strategy for a five-level FC based ANPC converter has been presented. A theoretical framework of a novel extended modulation technique for unsymmetrical and symmetrical voltage conditions of a five-level ANPC converter has been proposed. The application of the proposed modulation and control strategy, for a single-phase grid-connected PV system using a five-level FC based ANPC converter to produce ac output voltages with good power quality under both symmetrical and unsymmetrical conditions, has been investigated. Issues related to the balancing of dc-link voltages and its associated problems are discussed and a new control strategy has been introduced to solve the dc-link voltage divergence problem. The proposed strategy is applicable for other applications of the five-level FC-based ANPC converter. The effectiveness of the proposed modulation technique and control strategy was demonstrated by the simulation and experimental results in the laboratory, demonstrating the ability of the system to operate properly using smaller size dc-link capacitors to produce ac output voltage and current waveforms with good power quality while maintaining dc-link average voltage balancing.

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