



UNIVERSITY
OF WOLLONGONG
AUSTRALIA

University of Wollongong
Research Online

Faculty of Engineering and Information Sciences -
Papers: Part A

Faculty of Engineering and Information Sciences

2015

Voltage sag compensation of point of common coupling for low voltage ride-through enhancement of inverter interfaced DG using bridge type FCL

Seyed Behzad Naderi
University of Tasmania

Michael Negnevitsky
University of Tasmania, michael.negnevitsky@utas.edu.au

Amin Jalilian
University of Tabriz,, Jaliliyan-amin90@ms.tabrizu.ac.ir

Mehrdad Tarafdar Hagh
University of Tabriz, mehrdadh@uow.edu.au

Kashem M. Muttaqi
University of Wollongong, kashem@uow.edu.au

Publication Details

S. B. Behzad Naderi, M. Negnevitsky, A. Jalilian, M. Tarafdar. Hagh & K. M. Muttaqi, "Voltage sag compensation of point of common coupling for low voltage ride-through enhancement of inverter interfaced DG using bridge type FCL," in Power Engineering Conference (AUPEC), 2015 Australasian Universities, 2015, pp. 1-6.

Research Online is the open access institutional repository for the University of Wollongong. For further information contact the UOW Library:
research-pubs@uow.edu.au

Voltage sag compensation of point of common coupling for low voltage ride-through enhancement of inverter interfaced DG using bridge type FCL

Abstract

Fully converter wind turbines and solar power utilise an inverter to connect to grid. The inverters are vulnerable to voltage sag in their terminal due to its damaging effect on semiconductor self-Turnoff switches. In this paper, a bridge-Type fault current limiter (B-FCL) is proposed for low voltage ride-Through (LVRT) of the inverters during different types of fault with simple control system. The proposed B-FCL is capable to compensate the voltage sag in point of common coupling (PCC) and makes a safe condition not only for the inverter but also for any equipment which has been connected to the PCC in the power system. The B-FCL does not affect the normal operation of the inverter. Whenever the fault happens, a limiting resistor enters to the line current pass and decreases the fault current. As a result, the voltage sag on the PCC is mitigated due to limiting the fault current. The proposed B-FCL improves LVRT capability of the inverter, which does not require to changing its control method to ride through the low voltage. Furthermore, the DC input voltage of the inverter will not increase due to consuming the excessive active power by the limiting resistance of the B-FCL. PSCAD/EMTDC software is utilised to show the appropriate performance of the B-FCL during the symmetrical and asymmetrical grid faults through simulation results.

Keywords

coupling, low, point, compensation, sag, voltage, ride, fcl, type, enhancement, inverter, interfaced, common, dg, bridge

Disciplines

Engineering | Science and Technology Studies

Publication Details

S. B. Behzad Naderi, M. Negnevitsky, A. Jalilian, M. Tarafdar. Hagh & K. M. Muttaqi, "Voltage sag compensation of point of common coupling for low voltage ride-through enhancement of inverter interfaced DG using bridge type FCL," in Power Engineering Conference (AUPEC), 2015 Australasian Universities, 2015, pp. 1-6.

Voltage Sag Compensation of Point of Common Coupling for Low Voltage Ride-Through Enhancement of Inverter Interfaced DG Using Bridge Type FCL

S. B. Naderi¹, M. Negnevitsky¹, A. Jalilian², M. Tarafdar Hagh², K. M. Muttaqi³

¹School of Engineering and ICT, University of Tasmania, Australia

²Faculty of Electrical and Computer Engineering, University of Tabriz, Iran

³School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, Australia
Naderi.Seyedbehzad@utas.edu.au

Abstract—Fully converter wind turbines and solar power utilise an inverter to connect to grid. The inverters are vulnerable to voltage sag in their terminal due to its damaging effect on semiconductor self-turnoff switches. In this paper, a bridge-type fault current limiter (B-FCL) is proposed for low voltage ride-through (LVRT) of the inverters during different types of fault with simple control system. The proposed B-FCL is capable to compensate the voltage sag in point of common coupling (PCC) and makes a safe condition not only for the inverter but also for any equipment which has been connected to the PCC in the power system. The B-FCL does not affect the normal operation of the inverter. Whenever the fault happens, a limiting resistor enters to the line current pass and decreases the fault current. As a result, the voltage sag on the PCC is mitigated due to limiting the fault current. The proposed B-FCL improves LVRT capability of the inverter, which does not require to changing its control method to ride through the low voltage. Furthermore, the DC input voltage of the inverter will not increase due to consuming the excessive active power by the limiting resistance of the B-FCL. PSCAD/EMTDC software is utilised to show the appropriate performance of the B-FCL during the symmetrical and asymmetrical grid faults through simulation results.

Index Terms—Inverter; bridge type fault current limiter (B-FCL); symmetrical and asymmetrical faults; low voltage ride-through (LVRT); point of common coupling (PCC) voltage.

I. INTRODUCTION

Nowadays, researcher pays as much possible as attention to the renewable energy mainly due to increasing power demand and air pollution issues [1]. Therefore, the future generation may mostly depend on the renewable energy resources. Solar power, wind power, hydropower, etc. are all attractive source of distributed generators (DGs) [2, 3]. In most cases, to connect the renewable generation to the power system, utilising an inverter to interact with the utility is essential. For example, the voltage source inverters are widely used for solar power and fully converter based wind power [4]. One of the most significant problem of inverter interfaced DGs is low voltage ride-through capability during fault. Semiconductor switches, which are used in the inverter, are vulnerable to the high values of fault current. As a result, there is a probability of disconnection of the inverter by operation of

protection system during voltage sag [5]. Disconnection of inverter interfaced DGs from the power system in the high penetration level of renewable power generation can cause to lose transient stability of power system [6, 7].

Considering the grid codes, China's newly enacted national standard GB/T 19964-2012 recommends 150(ms) continuous operation when the PCC voltage falls to zero [8]. Grid codes of different countries in Europe for wind turbines have been discussed in [9]. Out of the Europe's grid codes, the most challenging one is Nordic grid code, which requires the wind turbine to operate for 250(ms) during zero voltage in high voltage connection point. This requirement for low voltage ride-through makes that the inverter should have high low voltage ride-through capability to remain connected for 250(ms) during zero voltage in point of common coupling (PCC). The LVRT capability of generating units is mandatory in harmonised Europe network code and is one of the most important requirements for newly approved EU grid code [9, 10].

To ride through the low voltage of the inverter, many strategies have been proposed. Using indirect current control method, which is focused on controlling the delivered active power during the fault, has been studied in [11]. The drawbacks of the mentioned strategy are linked to the DC voltage stability and power quality. Application of energy storage systems is discussed in [12]. Dynamic voltage restorer is employed to compensate the voltage dip in the power networks which uses the large energy storage components [13]. Some methods for low voltage ride-through are based on the control methods including the model current predictive control [14], current control method [15], robust control [16] and voltage dip detection and phase locked [17].

The most common reason to cause the voltage sag in the power system is linked to the high current levels [18, 19]. The high current levels occur by either faults or starting large induction motors [20, 21]. The grid faults, when happen, make significant voltage sag in the power system, which force all power generation units to feed the fault location. As aforementioned, the inverter interfaced wind turbine and solar power are interesting in nowadays power system, so, if there is

not any low voltage ride-through method, they are also included in feeding the fault location. Using fault current limiters (FCLs) is one of the most effective solutions to limit the fault current. Many different types of FCLs have been proposed in the literature, which can be divided as follows: resistive or inductive type, solid-state type, saturated core type and superconductive or non-superconductive type [22].

This paper proposes a bridge type fault current limiter (B-FCL) which includes a limiting resistance to limit the fault current level. The proposed structure is placed in the PCC to not only reduce the faulty line current level but also to decrease the voltage sag in the PCC. In this way, the inverter interfaced renewable energy resources can ride through the low voltage without any control issues during the fault. In fact, the inverter continues its normal operation during the fault and generates as much active power as possible without any interruption. Therefore, after fault removal, the power system does not sense any reduction in active power generation, which helps power system dynamic stability especially in a high penetration level of the renewable energy resources.

II. OPERATION PRINCIPLES OF THE PROPOSED B-FCL

The proposed structure of the B-FCL is shown in Fig. 1. The B-FCL includes a bridge part and a limiting resistance (R_{FCL}). The bridge part composes a diode rectifier bridge, a small non-superconductor DC reactor (L_{dc}), a semiconductor switch (such as *IGBT*, *IGCT* etc.) and a freewheeling diode (D_5).

During the normal operation of the inverter interfaced distributed generation, the self-turnoff switch is ON. As a result, the line current (I_{line}) passes through “ D_1 , L_{dc} , self-turnoff switch, D_4 ” during the positive alternative and “ D_3 , L_{dc} , self-turnoff switch, D_2 ” during the negative alternatives. So, the L_{dc} is charged to peak of the I_{line} and behaves as a short circuit. Using semiconductor devices (diodes and self-turnoff switch) and small value of the non-superconducting L_{dc} , cause a negligible voltage drop on the B-FCL. Therefore, if the voltage drops on the L_{dc} , the diodes of rectifier bridge and the self-turnoff switch are neglected, the proposed B-FCL does not have any effect on the normal operation of the power system. However, it should be noted that due to the fast operation of the self-turnoff switch (such as *IGBT*, *IGCT* etc.), the small value for the L_{dc} is sufficient to prevent sever di/dt at the beginning of the fault occurrence. Therefore, the voltage drop and power losses will be negligible.

Fig. 2 shows the control circuit of the proposed B-FCL. When the fault occurs, the I_{line} increases. The DC current of the B-FCL increments as well. When the DC current of the B-FCL reaches to the maximum permissible current (I_m) during the fault, the self-turnoff switch will be turned off. Therefore, the single-phase rectifier bridge retreats from the line. In this condition, the PCC voltage drops on the R_{FCL} and the I_{line} will pass through the R_{FCL} which limits the fault current value as (1). At this moment, the freewheeling diode is turned on to provide a free route for the DC reactor current when the self-turnoff is OFF.

$$I_{fault} = \frac{V_{PCC}}{Z_{sh}} \quad (1)$$

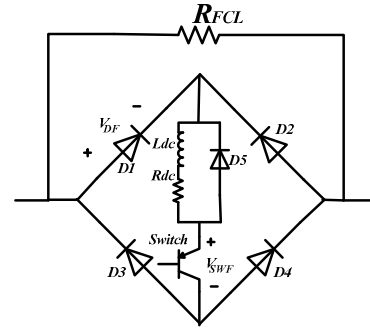


Figure 1. The proposed B-FCL topology

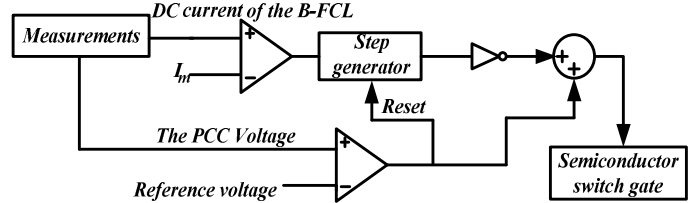


Figure 2. Control circuit of the proposed B-FCL

As it is obvious, after fault removal, the proposed B-FCL should be able to bypass the R_{FCL} from the line. When the fault is removed, it is assumed that the self-turnoff switch is still OFF. As a result, the R_{FCL} will be connected in series with the line just after fault removal. However, it is clear that after fault clearance, the PCC voltage will be back to its normal operation. Therefore, comparison of the PCC voltage with its normal value can be a detection pulse after the fault. The pulse turns the self-turnoff switch on and the R_{FCL} will be bypassed.

III. POWER LOSS CALCULATION

The power loss calculation is considered during the normal operation of the power system. As mentioned before, the self-turnoff switch is ON. Therefore, the power losses include the single phase rectifier bridge, the self-turnoff switch and non-superconducting L_{dc} . In addition, it should be noted that the proposed B-FCL is connected in series with the individual phases of three phase system. So total power losses should include all of the proposed B-FCLs.

The total power loss of the B-FCLs can be expressed as follows:

$$3P_{loss} = 3(R_{dc}I_{dc}^2 + 4V_{FD}I_{av} + V_{FS}I_{dc}) \quad (2)$$

where P_{loss} , I_{av} and I_{dc} and are the power loss of the B-FCL, average of the current in each diode of the rectifier bridge and the DC current of the B-FCL, respectively. Also, voltage drop on the diodes of the rectifier bridge and the self-turnoff switch is shown by V_{FD} and V_{FS} , respectively.

Typically, for high power applications, the voltage drop on the semiconductor devices are between 1(V) to 4(V) [23]. Furthermore, due to using the small value for the L_{dc} , its inherent resistance is also very small. As a result, the total power losses of the proposed B-FCLs can be very small percentage of the total generated active power of the DC source.

IV. SIMULATION RESULTS: INCLUDING THE SYMMETRICAL AND ASYMMETRICAL FAULTS

The simulated power system including the proposed B-FCL is shown in Fig. 3. The DC source is connected to the grid through the voltage source inverter with sinusoidal pulse width modulation, a step-up transformer and the transmission line. It should be mentioned that the control strategy of the inverter during the fault, voltage source strategy, is as same as during the normal operation of the inverter. The proposed B-FCL is placed in the PCC. The parameters of the simulation is presented in Table I.

Two types of faults, three phase fault (LLG) as symmetrical type, line to line and to ground fault (LLG) and single phase to ground fault (LG) as asymmetrical type will be applied at 1(s) in the PCC. The fault duration is 150(ms) in all cases.

A. Symmetrical Fault

In this section, the LLLG fault is applied in the PCC. Fig. 4 shows the AC line current without any low voltage ride-through method. The line current increases up to around 1.5(kA) which can be vulnerable to the inverter's self-turnoff switches. The DC side current of the inverter is presented in Fig. 5. Without any low voltage ride-through strategy, not only the DC side current of the inverter increases but also there are large oscillations on it. Also, the PCC voltage is illustrated in Fig. 6. The voltage in the PCC drops to zero for 150(ms) which affects any possible connected equipment to the PCC.

By employing the proposed B-FCL to ride through the low voltage of the inverter, both the line currents and DC side current of the inverter are limited effectively. Due to the symmetrical fault condition, Fig. 7 shows only the line current of A phase including the DC current of the B-FCL and the R_{FCL} current. As it is obvious, after the self-turnoff switch operation, the rectifier bridge retreats from the line and the R_{FCL} enters and limits the fault current. The DC side current of the inverter is shown in Fig. 8 which is both limited and smoothed in comparison with Fig. 5.

As aforementioned, to ride through the low voltage, the B-FCL inserts the large R_{FCL} to the faulty line. This operation principle mitigates voltage sag in the PCC by limiting the fault current. Fig. 9(a) in comparison with Fig. 6 clarifies that the zero voltage sag has been mitigated during the fault. Also to pay more attention on the voltage sag compensation capability of the proposed B-FCL, Fig. 9(b) presents the voltage drop on the B-FCL. Before and after the fault, the proposed structure does not have any effect on the normal operation of the power system and its voltage drop is almost zero. In the fault interval, the voltage drop on the B-FCL can compensate the PCC voltage in the fault condition.

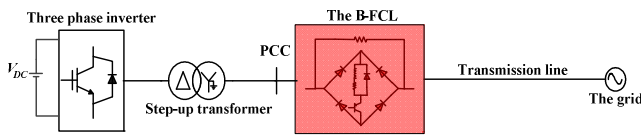


Figure 3. The simulated power system including the proposed B-FCL

TABLE I. SIMULATED POWER SYSTEM PARAMETERS

DC source	Rated Power: 4(MW), DC voltage: 5(kV), Capacitor: 1000(μ F)
Voltage source inverter	Carrier frequency: 1080(Hz), Output frequency: 60(Hz), Voltage drop on IGBT: 2(V)
Step-up transformer	Voltage ratio: 4(kV)/33(kV), Base operation frequency: 60(Hz), 3 phase transformer MVA: 5(MVA), Reactance: 0.1(p.u.)
The proposed B-FCL	Voltage drop on IGBT and diodes: 2(V), R_{sh} : 50ohm, Non-superconducting DC reactor: 10(mH), The inherent resistance of the DC reactor: 0.01(ohm), Maximum permissible current: 600(A)
The grid and transmission line	The grid voltage: 33(L-L, kV), The grid impedance: 50(mH), Transmission line impedance: 6(mH)

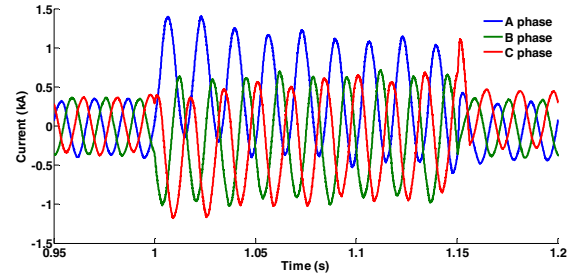


Figure 4. The AC output currents of the inverter during LLLG fault

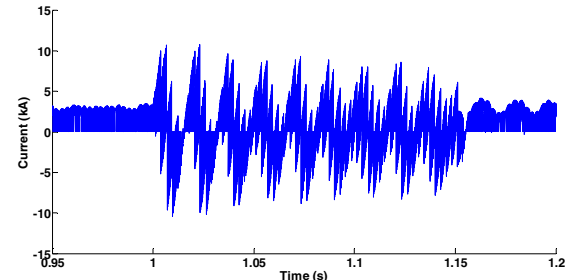


Figure 5. The DC side current of the inverter during LLLG fault

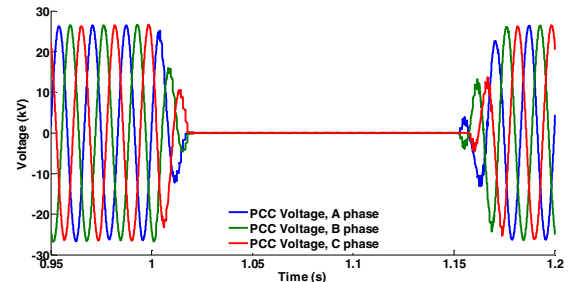


Figure 6. The PCC voltage during LLLG fault

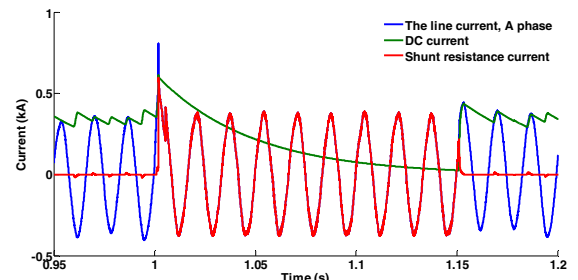


Figure 7. A phase line current with the B-FCL operation during LLLG fault

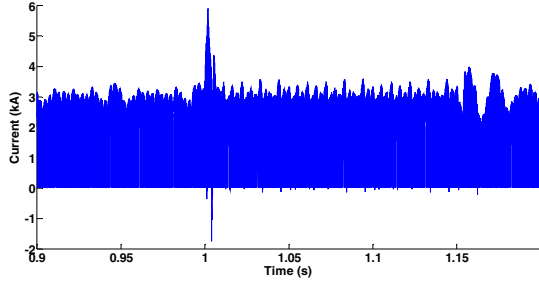


Figure 8. The DC current of the inverter with the B-FCL operation

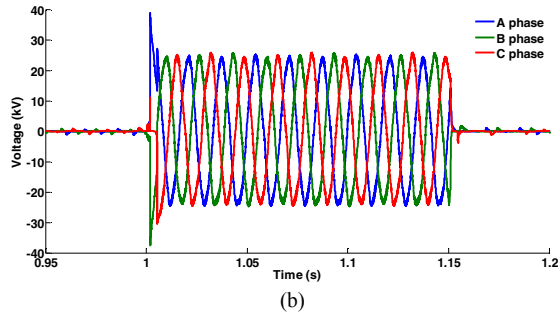
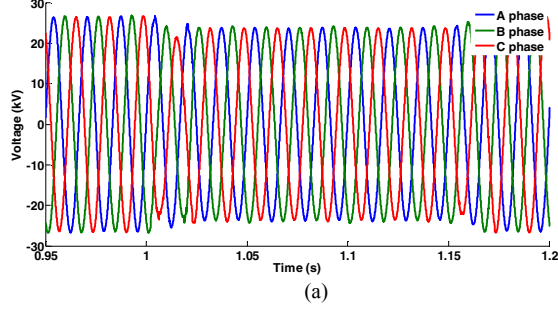


Figure 9. During LLLG fault with the B-FCL operation (a) The PCC voltage (b) The voltage drop on the B-FCL

B. Asymmetrical Fault

1) Single phase to ground: LG fault

The LG fault impact is evaluated in this section. The fault is applied in C phase in the PCC for 150(ms). In this situation, the B-FCL, which is placed in C phase, only operates. As well as the previous section, first, the fault condition is considered without any low voltage ride-through method. After that, the results will be compared to the B-FCL function on the low voltage ride-through improvement during the LG fault.

The AC currents are illustrated in Fig. 10 without the B-FCL operation. As it is clear, the peak of fault current reaches up to about 2(kA). Fig. 11 shows the PCC voltage during the LG fault. The C phase voltage sag is zero and affects the healthy lines as well.

When the proposed B-FCL is utilised to improve the low voltage ride-through capability, the fault current in C phase is restricted in a best manner. Fig. 12 shows the all three phase current including the R_{FCL} current and the DC current of the B-FCL. The B-FCL in C phase just operates and the other ones do not have any effect on the normal operation of the healthy phases, A and B phases. Furthermore in Fig. 13, the PCC voltages are recovered and the B-FCL makes the safe and reliable situation in the PCC. The voltage drop on the B-FCL for the LG fault is shown in Fig. 14. As it is expected, the

voltage drop on the B-FCL occurs in C phase which is the faulty line. So the healthy lines, A and B phase, do not sense the fault condition

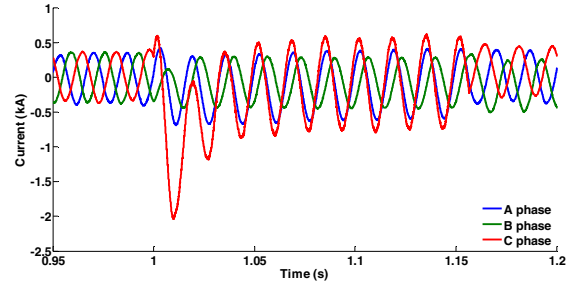


Figure 10. The AC output current of the inverter during LG fault

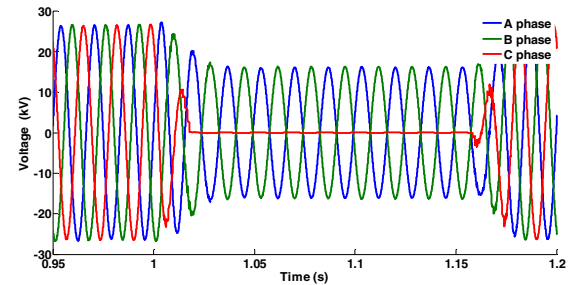


Figure 11. The PCC voltage during LG fault

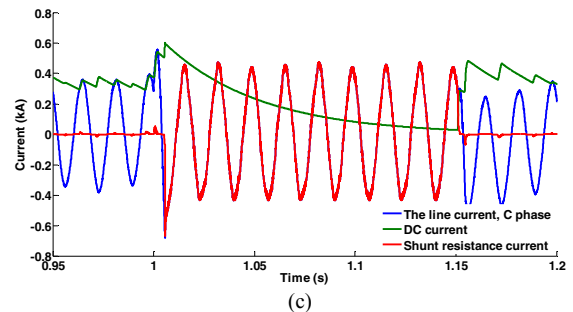
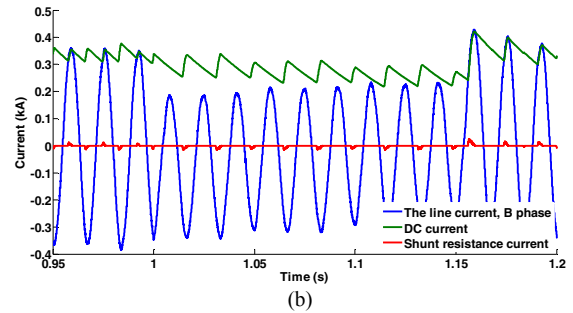
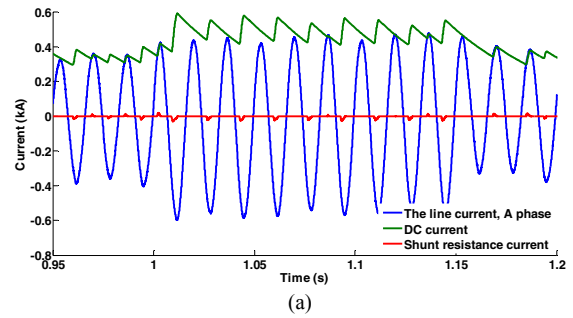


Figure 12. The AC output currents of the inverter with the B-FCL operation during LG fault

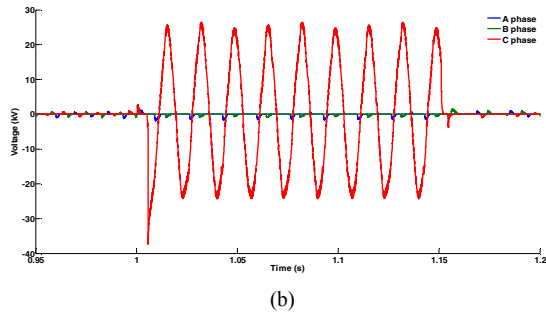
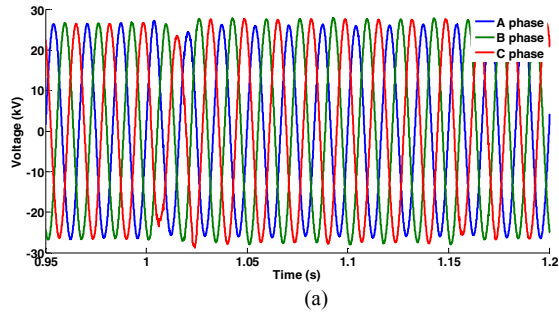


Figure 13. During LG fault with the B-FCL operation (a) The PCC voltage (b) The voltage drop on the B-FCL

2) Line to line and to ground: LLG fault

In this section, the low voltage ride-through capability of the proposed B-FCL during the LLG fault in B and C phases is considered. First, without the proposed B-FCL, the AC output currents and the PCC voltage are shown in Fig. 14 and Fig. 15, respectively. The maximum peak current is more than $3(kA)$ and the voltage sag happens in all three phases.

Utilising the B-FCL improves the inverter operation and decrease the fault current level in the faulty phases (B and C). Therefore, during the LLG fault, the inverter can remain connected to the power system.

As shown in Fig. 16, the B-FCLs, which are located in the faulty phases, operate and insert the R_{sh} . As it is clear, the line currents in B and C phases are limited successfully. The proposed structure in the healthy phase, A phase, does not function and continues its normal operation.

The PCC voltage and the voltage drop on the proposed structure are shown in Fig. 17(a) and Fig. 17(b), respectively. Considering Fig. 17(b), it is clear that the proposed structure can mitigate the voltage sag in the PCC and aids the inverter to ride through the fault without any disconnection from the grid.

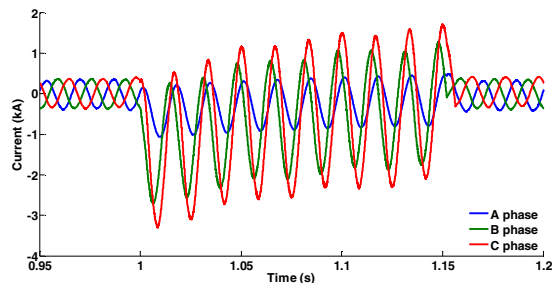


Figure 14. The AC output currents of the inverter during LLG fault

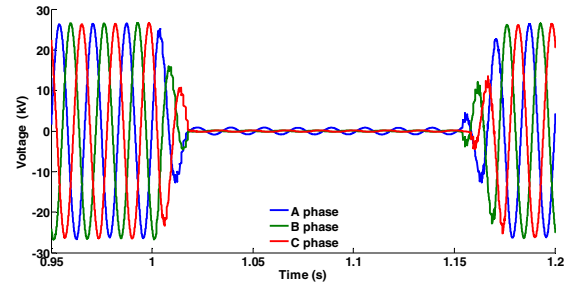


Figure 15. The PCC voltage during LLG fault

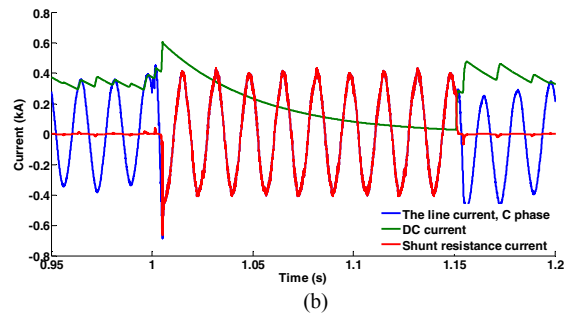
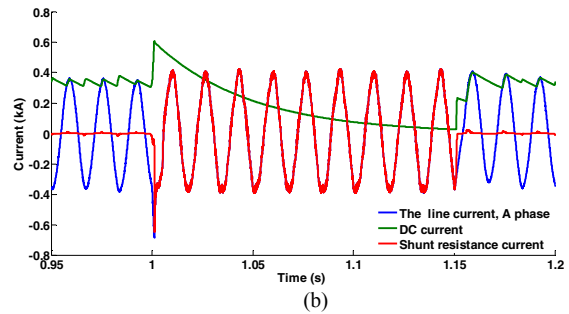
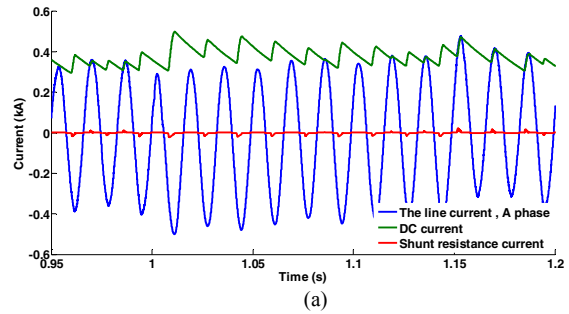


Figure 16. The AC output currents of the inverter during the B-FCL operation

V. CONCLUSION

This paper proposed the bridge type fault current limiter (B-FCL) to improve the low voltage ride through capability of the inverter interfaced distribution generation. The single phase B-FCL is placed in each individual phases. During the normal operation of the grid, the proposed structure does not affect the power system. When the fault occurs, the limiting resistance enters to the faulty line and suppresses the fault current level. The effectiveness of the proposed B-FCL has been assessed through all grid fault types including the three-phase fault, line to line and to ground fault and the single-phase fault. The B-FCL can mitigate the voltage sag in the point of common coupling during the fault and as a result, not only the inverter can stay connected to the utility but also the

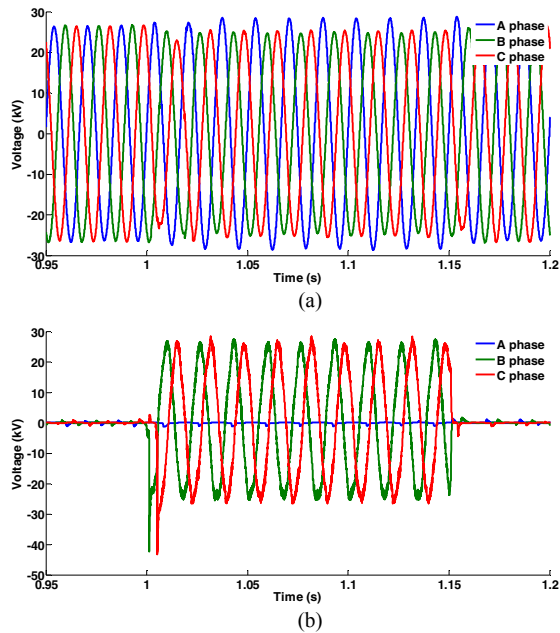


Figure 17. During LLG fault with the B-FCL operation (a) The PCC voltage (b) The voltage drop on the B-FCL

connected equipment to the PCC is not affected. Furthermore, with the proposed approach, the inverter does not require to change its operational condition in the fault condition and can continue to deliver as much active power as possible without any interruption. Simulation results have been provided by PSCAD/EMTDC software.

VI. REFERENCES

- [1] M. Y. Khamaira, A. Abu-Siada, and S. Islam, "DFIG-based WECS fault ride through complying with Australian grid codes," in *Power Engineering Conference (AUPEC), 2014 Australasian Universities*, 2014, pp. 1-5.
- [2] G. Rashid and M. H. Ali, "A Modified Bridge-Type Fault Current Limiter for Fault Ride-Through Capacity Enhancement of Fixed Speed Wind Generator," *Energy Conversion, IEEE Transactions on*, vol. 29, pp. 527-534, 2014.
- [3] A. Jalilian, M. Tarafdar Hagh, M. Abapour, and K. M. Muttaqi, "DC link fault current limiter-based fault ride-through scheme for inverter-based distributed generation," *IET Renew. Power Generation*, vol. In Press, 2015.
- [4] H. Tian, F. Gao, C. Ma, G. He, and G. Li, "A review of low voltage ride-through techniques for photovoltaic generation systems," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 1566-1572.
- [5] W. Shuzheng, Y. Xiaojun, and Z. Jianfeng, "A novel low voltage ride through strategy of two-stage grid-connected photovoltaic inverter," in *Future Energy Electronics Conference (IFEEEC), 2013 1st International*, 2013, pp. 400-405.
- [6] K. Kawabe and K. Tanaka, "Impact of Dynamic Behavior of Photovoltaic Power Generation Systems on Short-Term Voltage Stability," *Power Systems, IEEE Transactions on*, vol. PP, pp. 1-9, 2015.
- [7] H. H. Yengejeh, F. Shahnia, and S. M. Islam, "Contributions of single-phase rooftop PVs on short circuits faults in residential feeders," in *Power Engineering Conference (AUPEC), 2014 Australasian Universities*, 2014, pp. 1-6.
- [8] H. Guanghui, W. Deshun, Y. Bin, K. Ailiang, L. Huan, Z. Xinlong, *et al.*, "Development of low voltage ride through testing device for the grid-connected photovoltaic power station in high-altitude area," in *Electricity Distribution (CICED), 2014 China International Conference on*, 2014, pp. 21-25.
- [9] N. G. Code, "Nordic collection of rules," ed, 2007.
- [10] "ENTSO-E Network Code for Requirements for Grid Connection Applicable to all Generators," p. 85, 2013.
- [11] A. Camacho, M. Castilla, J. Miret, A. Borrell, and L. Garcia de Vicuna, "Active and Reactive Power Strategies With Peak Current Limitation for Distributed Generation Inverters During Unbalanced Grid Faults," *Industrial Electronics, IEEE Transactions on*, vol. 62, pp. 1515-1525, 2015.
- [12] C. Abbey and G. Joos, "Supercapacitor Energy Storage for Wind Energy Applications," *Industry Applications, IEEE Transactions on*, vol. 43, pp. 769-776, 2007.
- [13] D. Ramirez, S. Martinez, C. A. Platero, F. Blazquez, and R. M. de Castro, "Low-Voltage Ride-Through Capability for Wind Generators Based on Dynamic Voltage Restorers," *Energy Conversion, IEEE Transactions on*, vol. 26, pp. 195-203, 2011.
- [14] V. Yaramasu, W. Bin, S. Alepuz, and S. Kouro, "Predictive Control for Low-Voltage Ride-Through Enhancement of Three-Level-Boost and NPC-Converter-Based PMSG Wind Turbine," *Industrial Electronics, IEEE Transactions on*, vol. 61, pp. 6832-6843, 2014.
- [15] J. Miret, A. Camacho, M. Castilla, L. G. de Vicuna, and J. Matas, "Control scheme with voltage support capability for distributed generation inverters under voltage sags," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 5252-5262, 2013.
- [16] T. Hao, G. Feng, M. Cong, H. Guoqing, and L. Guanghui, "Robust control of two-stage photovoltaic inverter for unbalanced low voltage ride-through operation," in *Electronics and Application Conference and Exposition (PEAC), 2014 International*, 2014, pp. 560-565.
- [17] M. Karimi-Ghartemani and M. R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *Power Systems, IEEE Transactions on*, vol. 19, pp. 1263-1270, 2004.
- [18] S. B. Naderi, M. Jafari, and M. T. Hagh, "Impact of Bridge type Fault Current Limiter on Power System Transient Stability," in *7th International Conference on Electrical and Electronics Engineering, Bursa, Turkey*, 2011, pp. 148-152.
- [19] M. Pannu, Y. Valent, and U. Garbi, "Pre-saturated core Fault Current Limiter," in *Power Engineering Conference (AUPEC), 2013 Australasian Universities*, 2013, pp. 1-7.
- [20] M. T. Hagh, S. B. Naderi, and M. Jafari, "Application of Non-superconducting Fault Current Limiter to improve transient stability," in *Power and Energy (PECon), 2010 IEEE International Conference on*, 2010, pp. 646-650.
- [21] S. Leng, R. U. Haque, N. Perera, J. Salmon, and A. Knight, "Soft start and voltage control of grid connected induction motors using floating capacitor H-bridge converters," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 1309-1316.
- [22] S. B. Naderi, M. Jafari, and M. T. Hagh, "Controllable resistive type fault current limiter (CR-FCL) with frequency and pulse duty-cycle," *International Journal of Electrical Power & Energy Systems*, vol. 61, pp. 11-19, 2014.
- [23] ABB, "High-power semiconductors," p. 71, 2015.