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# Improving fault ride-through of three phase voltage source inverter during symmetrical fault using DC link fault current limiter

Mehrdad Tarafdar Hagh
*University of Tabriz*, haque1347@yahoo.com

Amin Jalilian
*University of Tabriz*, Jaliliyan-amin90@ms.tabrizu.ac.ir

Seyed Behzad Naderi
*University of Tasmania*

Michael Negnevitsky
*University of Tasmania*, michael.negnevitsky@utas.edu.au

Kashem M. Muttaqi
*University of Wollongong*, kashem@uow.edu.au

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**Abstract**
The majority of distributed generation (DG) units utilize three phase voltage source inverter (VSI) to exchange electric power with the utility grid. The VSI employs semiconductor devices (SDs) with limited current withstand capabilities which are very vulnerable during grid faults. However, to ensure a secure and reliable operation of power systems at high penetration level of the DGs, most of the new grid codes worldwide require that the VSIs must have fault ride-Through (FRT) capability. This paper presents a DC link fault current limiter (DLFCL) based VSI FRT scheme to improve its FRT capability. In the proposed scheme, the DLFCL is connected in series with the DC side of the VSI to limit the output current during symmetrical grid fault. The DLFCL does not have considerable effect on the VSI performance during the normal operation, whereas it limits the output current in all phases to the safe area operation of the SDs of the inverter. The effectiveness of the proposed scheme is validated through the simulation studies in PSCAD/EMTDC software.

**Keywords**
inverter, source, voltage, phase, three, ride, fault, improving, link, limiter, dc, current, symmetrical, during

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# Improving Fault Ride-Through of Three Phase Voltage Source Inverter During Symmetrical Fault Using DC Link Fault Current Limiter

*M. Tarafdar Hagh[1], A. Jalilian[1], S. B. Naderi [2], M. Negnevitsky [2], K. M. Muttaqi[3]*
*[1]Faculty of Electrical and Computer Engineering, University of Tabriz, Iran*
*[2] School of Engineering and ICT, University of Tasmania, Australia*
*[3]School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, Australia*
*mehrdadh@uow.edu.au*

***Abstract*— The majority of distributed generation (DG) units utilize three phase voltage source inverter (VSI) to exchange electric power with the utility grid. The VSI employs semiconductor devices (SDs) with limited current withstand capabilities which are very vulnerable during grid faults. However, to ensure a secure and reliable operation of power systems at high penetration level of the DGs, most of the new grid codes worldwide require that the VSIs must have fault ride-through (FRT) capability. This paper presents a DC link fault current limiter (DLFCL) based VSI FRT scheme to improve its FRT capability. In the proposed scheme, the DLFCL is connected in series with the DC side of the VSI to limit the output current during symmetrical grid fault. The DLFCL does not have considerable effect on the VSI performance during the normal operation, whereas it limits the output current in all phases to the safe area operation of the SDs of the inverter. The effectiveness of the proposed scheme is validated through the simulation studies in PSCAD/EMTDC software.**

***Index Terms*-- Voltage-sourced inverter; symmetrical fault; fault ride-through; DC link; fault current limiter.**

## I. INTRODUCTION

Increased power demand and the depletion of energy resources have resulted in more attention being paid to renewable energy. Over the years, power electronic converters have found wide application in numerous grid interfaced systems including distributed power generations like fuel cell [1], solar energy [2], adjustable speed drives [3] and active power filters [4]. Most of these systems employ three phase voltage source inverter (VSI) whose functionality is to exchange variable power with the utility grid.

The VSIs employ semiconductor devices (SDs) with limited over current withstand capability that usually is within the range of 1-2 times of nominal current [5]. The VSI is inherently very sensitive to the grid faults. Thus, the fault condition can either trip out the VSI or damage its SDs [6].

Two main control strategies are proposed in the literature to control the VSIs: Current Control Strategy (CCS) and Voltage Control Strategy (VCS) [7]. The advantage of the CCS is that, the output current of VSI can be effectively restricted to an acceptable level during the fault condition; consequently, the inverter can ride-through networks faults. However, the CCS has several drawbacks, like reduction of main controller robustness and need of both voltage and current sensors. On the other hand, while the VCS has good performance during the normal operation, but high level of fault current which is its main drawback. By increasing the penetration level (PL) and islanding operation of distributed generation units (DGs) in the power systems, using the VCS to control the VSIs is more acceptable than the use of CCS [8]. Furthermore, at high PL of the VSIs in the power system, their disconnection from the utility during the faults is not acceptable. In addition, according to [9], the impact of VSIs on the network operation with 40% PL is not negligible.

Despite the IEEE standard 1547 which recommends that the DGs should be disconnected from the network when the fault occurs in the utility grid, in some new grid codes, the DGs are forced to stay connected to the grid and ride-through the network faults [10]. In relation to the above discussion, different studies are conducted on current limitation strategies of the VSIs during the network faults.

Reference [4] has presented simulation and experimental results of a resistor based short circuit fault protection scheme for series active power filters. Some control approaches for inverter-interfaced distributed energy resources are proposed in [11] and [12] to limit inverter fault current and improve their fault ride-through (FRT) capability. In [13], an inverter fault current limitation strategy has been introduced in a micro-grid at high PL of the VSIs. However, in [13], simulation and experimental results have not been presented to approve its proposed technique. In [14], the authors investigated fault behavior of the VSIs against various network faults and presented analytical and experimental results.

An active and reactive power control strategy has been proposed in [15], for DG inverters, to improve their FRT capability and enable them to support grid voltage during unbalanced faults.

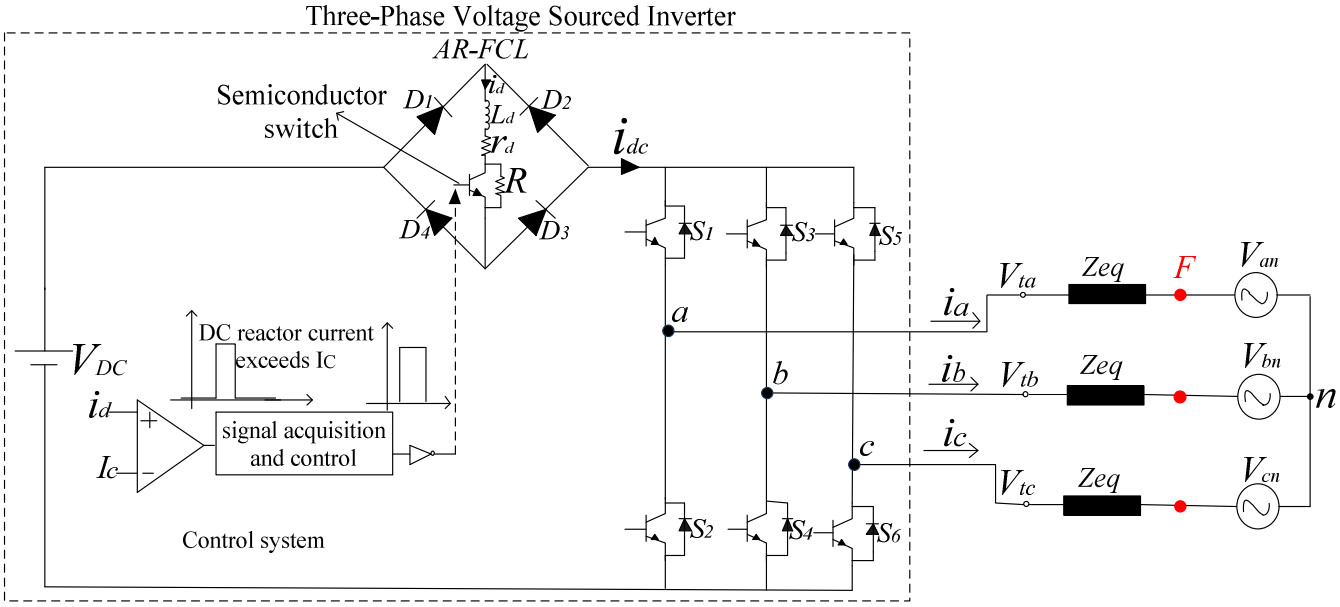


Figure 1. Power circuit topology of the proposed fault ride-through configuration for the VSI

An effective method to control the fault current level is to use fault current limiters (FCLs). Several types of FCLs have been studied to improve the power system performance in [16]-[18].

This paper proposes a novel DC link fault current limiter (DLFCL) based VSI FRT scheme to enhance the FRT capability of the VSIs during symmetrical fault. The DLFCL does not have effect on the VSI system performance during the normal operation of utility grid but it limits the inverter's output current to the safe area operation of the SDs during symmetrical fault. In this way, the VSI can stay connected to the utility during the fault even at zero grid voltage as recommended by "*E.ON*" grid code [10]. Moreover, the proposed DLFCL can use a non-superconducting inductor to decrease initial cost of superconducting inductor as well as the cost and volume of cryogenic system. Besides, according to [32], the problems of latch-up and wind-up arise when the inverter control strategy changes from the normal to the fault mode operation, during the fault condition. However, in the proposed scheme, the VSI operates as the VCS in the normal condition as well as in the fault condition.

## II. Proposed Fault Ride Through Scheme

Fig. 1 shows the configuration of the proposed FRT scheme of the VSI system. The model of the VSI for the purpose of the fault analysis can be made up under an assumption that the DC input voltage of the inverter is essentially fixed in the time frame of 0-1.0 s [20]. This voltage is shown with $V_{DC}$ in Fig. 1. To improve the FRT capability of the VSI, application of the DLFCL is proposed. The DLFCL includes diode rectifier bridge, $D_1$ to $D_4$ diodes, a non-superconductor coil (copper coil) that is modeled by a resistor $r_d$ and an inductor $L_d$ and finally a parallel connection of fully controllable semiconductor switch (SS) and a resistor (R) that are connected in series with the DC reactor. A two-level VSI is used to convert DC power provided by the primary DC energy source such as DGs to AC electrical power which is compatible with the utility. The DLFCL is connected in series with $V_{DC}$ as shown in Fig. 1. Also, equivalent impedance between high voltage side of the grid-connected transformer and inverter output terminals are modeled by $Z_{eq}=r_s+j\omega L_s$ in Fig. 1. The utility is modeled by an infinite bus AC system; thus, it is an ideal sinusoidal three-phase voltage source with a constant frequency and voltage ($V_{an}$, $V_{bn}$ and $V_{cn}$ in Fig. 1), where ω and $V_{\square}$ stand for its angular frequency and effective voltage value in each phase, respectively.

In common current limiting strategies, to limit the fault current, the FCLs should be connected in series with the individual phases in the AC side of the VSI. This approach is the well-known application of the FCLs in the power system as discussed in [16]. But in the proposed scheme, just one single set of the DLFCL, which is placed in the DC side of the VSI, is employed to limit the VSI's fault current in all three phases during all types of the grid fault. Also, from the power circuit topology point of view, the DLFCL uses the diode rectifier bridge and the fully controllable SS as a high speed switch. So, the application of the DLFCL in DC side of the VSI, in comparison with the previously introduced structures for AC side application results in considerable reduction in the current limiting costs of the FCLs.

## III. Principle of Operation of the DLFCL

In the normal operation of the power system, the SS is close and bypasses the R. By selecting the proper value for $L_d$, it is possible to achieve a nearly DC current through the DC reactor. However, it is evident that increasing the $L_d$ decreases the ripple of DC reactor current ($i_d$). This leads to short circuit of $L_d$ during the steady state operation. If the voltage drops on the diodes of single phase rectifier, the SS, and the small DC reactor resistances are neglected, the DLFCL does not affect the normal operation of the VSI. When the fault occurs in the power system in any phase of the three phases or two or three

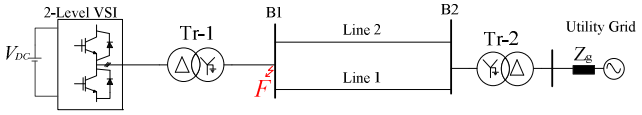


Figure 2. The simulated power system.

phases, the DC reactor of the DLFCL, prevents severe *di/dt* at the first moments of the fault and its current increases almost linearly. If the fault lasts for a long time, the current through the DC reactor will continue to increase. As soon as the current through the DC reactor reaches to a pre-defined value, the control circuit operates and turns OFF the SS. So, the R connects in series with the DC reactor. Therefore, the absorbed energy of the DLFCL's inductance discharges and the current of the DC reactor decreases. It is evident that, as the $i_d$ lies below the pre-defined value, the control circuit operates and turns ON the SS. In this way, the $i_d$ as well as the inverter output AC currents are restrained to the pre-defined value during the fault. So, the VSI can stay connected with the utility grid during the fault condition.

The control circuit of the DLFCL is shown in Fig. 1. In this study, the $i_d$ is utilized as the control signal to turn ON and turn OFF the SS. This control system does not need any parameters to measure in the AC side of the VSI. Therefore, when the $i_d$ lies above the pre-defined value $I_c$, that is higher than steady state current through the DC reactor, the control circuit turns ON the SS. The value of $I_c$ should be determined based on the SDs current rating.

## IV. Simulation Results

Single line diagram of the test system is shown in Fig.2. As shown in Fig. 2, the primary source is interconnected to the utility grid through the two level VSI, step-up transformer (with the same power rating of corresponding to the VSI) and a double-line transmission line. The utility grid is represented by a three phase AC voltage source with equivalent impedance of $Z_g$. To demonstrate the effectiveness of the proposed FRT scheme, its performance is evaluated during LLLG fault. PSCAD/EMTDC software is implemented to simulate fault condition. Out of all the different grid codes which are regulated by the various operators, "*E.ON*" grid code has severe FRT requirements [10]. According to "*E.ON*", when voltage at point of common coupling drops to zero for 0.15 (s), the DG must not be disconnected from the grid. So, in the all simulations, the fault lasts 0.15 (s). Furthermore, in the literature, the fault current magnitude of the VSI is considered between 1 (*p.u*) and 2 (*p.u*) [2], [8]-[9].

However, in the present paper, the maximum permissible current magnitude for the VSI is assumed to be 2 (*p.u*) [8]. The VSI simulation parameters can be found in [20] and network data are given in [21]. In this scenario, a temporary LLLG fault is applied in point F, as shown in Fig. 2, at t = 0.8s, that continues for 0.15s. This fault type, as a worst one, causes a severe voltage dip (100%) in the VSI terminal. At first, the simulation is carried out without the DLFCL. The results are shown in Fig. 3(a) to Fig. 3(d). As shown in Fig. 3(a), once the fault occurs, the voltage at the VSI terminal drops to zero value. In this condition, the VSI output current abruptly increases. As shown in Fig. 3(b), its peak value reaches to around 4 (*p.u*). Because, the maximum permissible current of the semiconductor switches is approximately two times of the nominal current [4], these over-currents can damage the VSI. As aforementioned, a 2-level VSI employs six power electronic switches for DC to AC power conversions. The current through *A-phase* (switches $S_1$ and $S_2$ in Fig. 1) are shown in Fig. 3(c). As Fig. 3(c) shows, these over-currents reach to about four times of the nominal value and tend to damage the semiconductor switches or trips out the VSI in the practical cases. Also, the DC link current is shown in Fig. 3(d). It is clear that there is a high level current that may cause large distortions in DC link current waveform during the fault.

To demonstrate the effectiveness of the proposed FRT approach, the temporary LLLG fault with the same fault characteristics of the previous study is occurred at point F, in Fig. 2, whereas the DLFCL is connected in series with the DC link of the VSI. Corresponding results are provided in Fig. 4(a) to Fig 5(d). The $i_d$ is shown in Fig. 4(a). It is clear that during the fault, the $i_d$ is effectively restricted to the pre-defined fault current level. Moreover, considering Fig. 4(b), the effective operation of the proposed DLFCL limits the VSI three phase fault current to less than twice of the nominal current. Also, the currents through *A-phase* SDs are shown in Fig. 4(c). It is obvious that during the voltage dip, *A-phase* SDs currents are limited to the pre-defined current value. So, the SDs operate in the safe area during the fault conditions. In addition, the DC link current is also presented in Fig. 4(d). Considering this figure, the DC link current has slightly smooth variation during the fault and is limited to the pre-defined value.

The other fact, which should be considered about employing the DLFCL, is about the limiting characteristic of the DC reactor during the first moments of the fault and before the operation of the SS. It is clear that the time interval between the fault initiation and the SS operation is very small [22] than required time for operating the protection devices and disconnecting the VSI from the utility grid. So, the severe *di*/*dt* which is initiated during the initial instants of the fault can damage the SDs of the VSI. The rate of change of current through one of the SDs of the VSI, at the first moment of fault, for both situations including with and without the proposed DLFCL in the DC link of the VSI, is compared to each other in Fig. 5. According to Fig. 5, the DLFCL can suppress the severe *di*/*dt* in the initial instants of fault occurrence in comparison with the case that does not include any FRT measure. According to this analysis, by implementation of the proposed FRT scheme, the VSI can stay connected to the utility during the worst case of short circuit fault at the point F. So, it compliances with the new grid code requirements.

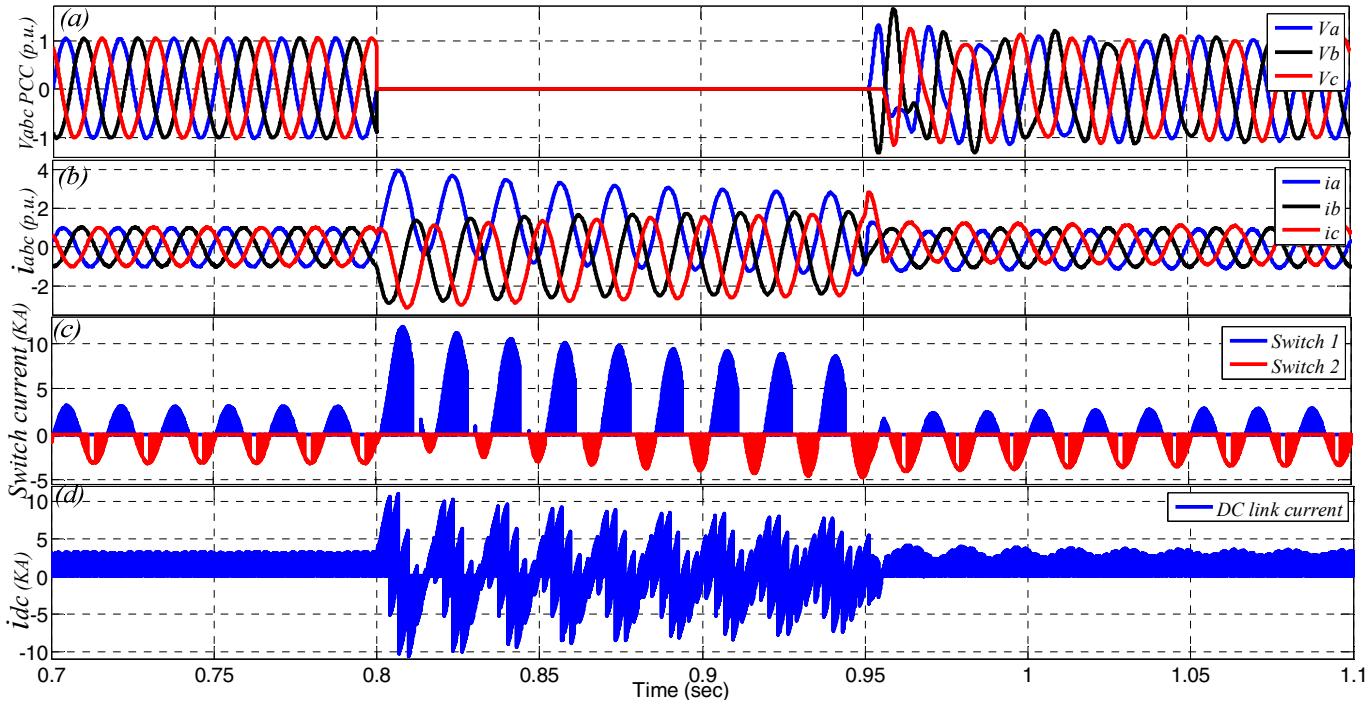


Fig. 3. Simulation results for the LLLG fault at point F without the proposed DLFCL, (a) three-phase voltages at point F ($V_a$, $V_b$ and $V_c$), (b) three-phase output current of the VSI ($i_a$, $i_b$ and $i_c$), (c) *A-phase* switch current of the inverter (switch 1 and switch 2), (d) the DC link current ($i_{dc}$).

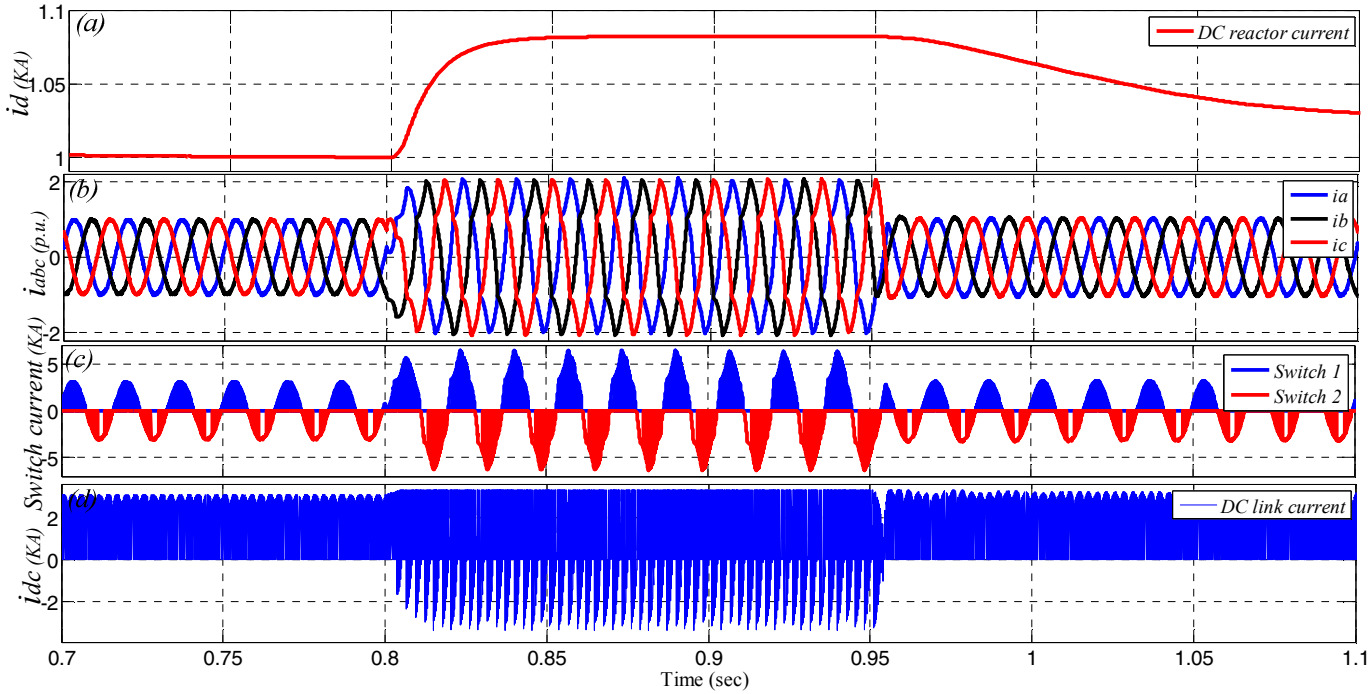


Figure 4. Simulation results for the LLLG fault at point F when the proposed DLFCL is employed: (a) the DC reactor current ($i_d$), (b) three-phase output current of the VSI ($i_a$, $i_b$ and $i_c$), (c) *A-phase* switch current of the inverter (Switch 1 and switch 2), (d) DC link current ($i_{dc}$).

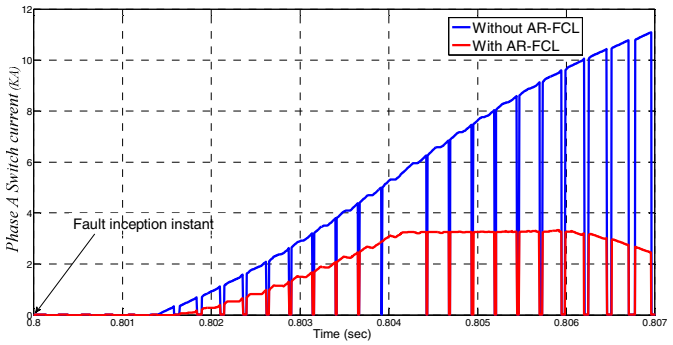

Figure 5. Effectiveness of the proposed FRT scheme in suppressing the initial rate of current change in the SDs of the VSI.

## V. CONCLUSION

This paper presents the novel DC link FCL based FRT scheme to improve the FRT capability in the three-phase VSI. The proposed approach uses one set of single phase DLFCL only which is placed in the DC side of the VSI. Therefore, this approach reduces the number of the required FCLs which are used in the AC side of the VSI. In addition, in the proposed DLFCL due to implementing the non-superconductor DC reactor, the initial cost also decreases. The VSC strategy is employed during the normal operation as well as during the fault condition with the DLFCL. The proposed DLFCL can suppress severe *di/dt* at the first moments of the fault and protect the SDs of the VSI from damage, even at zero grid voltage as recommended by new grid codes with a high degree of reliability. Simulation studies have been carried out for worst-case scenario. From the results, it is clear that the proposed approach provides reliable performance during symmetrical fault.

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