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Application of saturated core fault current limiters to interconnected distribution networks

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Abstract

There is an increasing need for electricity utilities to limit fault levels in critical locations in power systems so that existing switchgear can continue to function as expected. This is particularly true in electrical distribution systems, where the increased penetration of renewable and decentralised generation is forcing the network to be highly interconnected in order to allow for higher integration capacity and reliable operation. Consequently, the short-circuit currents in distribution systems have increased significantly. In this background, application of fault current limiting devices is one of the solutions that is being considered by the Distribution Network Service Providers (DNSPs). A saturated core Fault Current Limiter (FCL) is one such device that can be used in existing and future electrical distribution systems to reduce the fault currents to a manageable level. This paper presents the potential performance of a saturated core FCL, in an interconnected 11kV test system, utilising a new comprehensive time-domain model to represent the FCL. PSCAD/EMTDC studies and numerical fault analysis are carried out to simulate the efficacy of an FCL when placed on a bus-Tie of a looped circuit. The effect of the bus-Tie FCL impedance on the network impedance and the subsequent fault current contributions is investigated. It is demonstrated that in a circuit with complex interconnections, suppression of fault currents need multiple FCLs in critical feeders.

Application of Saturated Core Fault Current Limiters to Interconnected Distribution Networks

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Abstract—**There is an increasing need for electricity utilities to limit fault levels in critical locations in power systems so that existing switchgear can continue to function as expected. This is particularly true in electrical distribution systems, where the increased penetration of renewable and decentralised generation is forcing the network to be highly interconnected in order to allow for higher integration capacity and reliable operation. Consequently, the short-circuit currents in distribution systems have increased significantly. In this background, application of fault current limiting devices is one of the solutions that is being considered by the Distribution Network Service Providers (DNSPs). A saturated core Fault Current Limiter (FCL) is one such device that can be used in existing and future electrical distribution systems to reduce the fault currents to a manageable level. This paper presents the potential performance of a saturated core FCL, in an interconnected 11kV test system, utilising a new comprehensive time-domain model to represent the FCL. PSCAD/EMTDC studies and numerical fault analysis are carried out to simulate the efficacy of an FCL when placed on a bus-tie of a looped circuit. The effect of the bus-tie FCL impedance on the network impedance and the subsequent fault current contributions is investigated. It is demonstrated that in a circuit with complex interconnections, suppression of fault currents need multiple FCLs in critical feeders.**

Index Terms—**Distribution networks, electromagnetic transients, fault current limiter (FCL), interconnected networks, PSCAD/EMTDC**

I. Introduction

CONVENTIONAL distribution networks have been designed with a radial network configuration to operate with a unidirectional power flow. The application of a Fault Current Limiter (FCL) in such a network is quite straightforward, since the short-circuit current flow is also unidirectional and could be managed with the insertion of an FCL between the source and the load in a critical feeder of the network [1], [2]. However, with the advent of decentralised generation, the modern electrical distribution systems have become more interconnected to enable higher integration capacity and reliable operation [1], [3], [4]. Consequently, with these meshed and looped network configurations, FCL placement in distribution systems has become a far more complex problem. Installing an FCL at a bus-tie location in the network, has often been preferred by the utilities due to the additional benefits such a placement offers [5]. A bus-tie FCL typically allows two buses to be tied without significantly raising the fault current level of the system while enabling greater network flexibility and improved reliability. However, in a meshed network the power flow is not unidirectional and a fault in the system could be fed from many directions from different sources. In such a system, application of a single FCL at a bus-tie location may not provide the desired fault current reduction effect.

In this paper, network simulation studies are undertaken in PSCAD/EMTDC transient simulation package to analyse the operational behaviour and performance of a saturated core FCL in an interconnected distribution network. The saturated core FCL is a current limiting device that utilises the change in permeability between saturated and unsaturated states of the core material to provide a very low impedance during normal network operation and a relatively higher transient impedance during fault conditions. A major advantage of this technology is that it provides instantaneous reaction to a fault event and instantaneous recovery. A new nonlinear reluctance model for the saturated core FCL is used to represent the FCL in a hypothetical 11kV system, with the efficacy of the FCL placed on a bus-tie location in a looped circuit investigated. A numerical approach to fault analysis for the test system is also presented, with expressions for total fault current and fault contributions from each unfaulted bus derived. The effect of the bus-tie FCL impedance on the bus impedance matrix of the system and on the subsequent fault current contributions are also examined. It is demonstrated that in an interconnected circuit to achieve the desired fault current reduction multiple FCLs, placed on critical sources and feeders, are required.

II. Saturated Core FCLs

A. Operating Principle

A number of studies on the subject of saturated core FCLs, ranging from operational behaviour, material aspects, core designs, prototypes and testing, have been reported in the literature [6]–[8]. The saturated core FCL, essentially utilises the dynamic and nonlinear magnetic behaviour of steel cores to operate as a variable inductance reactor. The device consists of steel cores placed inside two coils carrying AC current and connected in series with the circuit to be protected. Each AC coil is wound and connected in such a way that the flux is set up in opposite directions in each coil. A DC coil, encompassing both the AC coils and the associated steel cores, is used to initially bias the cores into saturation.

During normal operation, the AC current is not large enough to drive the cores out of saturation and hence the FCL operates completely within the saturated region of the B-H curve. The device, under such conditions, has a very low impedance and is almost transparent to the grid. During a fault event, the increased current in the AC coils generates an AC magnetic flux sufficient to drive each core out of saturation alternately (during each half cycle) and the FCL operates in a region of much higher permeability. Hence, the impedance of the AC coils increases significantly during a fault, consequently limiting the fault current.

B. Modelling Saturated Core Fault Current Limiter

When modelling electromagnetic systems, the magnetic circuit concept [9] has often been used to derive analytical models with adequate accuracy [10], [11]. Recently, this concept was extended to saturated core FCLs in [12], where the magnetic field of the device was represented by a magnetic circuit of lumped reluctances. A PSCAD/EMTDC model of the saturated core FCL [13], developed based on this magnetic reluctance circuit, is used to represent the FCL in this paper. The model is implemented in PSCAD/EMTDC as a page module, containing three mutually dependent circuits: (1) the AC circuit, consisting of the two AC windings and the interconnection to the grid side network (illustrated in Fig. 1a) (2) the DC circuit consisting of the biasing arrangement of the FCL (illustrated in Fig. 1b) and (3) the magnetic reluctance circuit (illustrated in Fig. 1c). The coupling between the electric circuits and the magnetic circuit is achieved through an iterative process, where the parameters derived from solving the magnetic circuit are used to solve the electric circuits and vice versa [13].

III. APPLICATION OF AN FCL

A. 11kV Test Network

To study the current limiting behaviour of an FCL when inserted into the bus-tie of an interconnected distribution network, a simple representative test network (as shown in Fig. 2) was chosen. The test network under consideration, has two interconnected substations, with each substation having a fault current in-feed, modelled as voltage sources. Each of the sources shown in Fig. 2 could represent a grid in-feed, a distributed generation or an incoming feed from another distribution substation. The system parameters are summarised in Table I. For simplicity, each substation is assumed to have the same capacity. Note that these parameters are representative and do not reflect actual values of a real 11kV system.

B. FCL Model Parameter Determination

The saturated core FCL design process is a multi-variable optimisation problem that ideally involves the use of both Finite Element Analysis (FEA) and optimisation software to determine the optimal FCL design parameters that would meet given performance specifications. Following this process, an FCL design that was best suited for the the test network illustrated in Fig. 2 was determined. The parameters of the
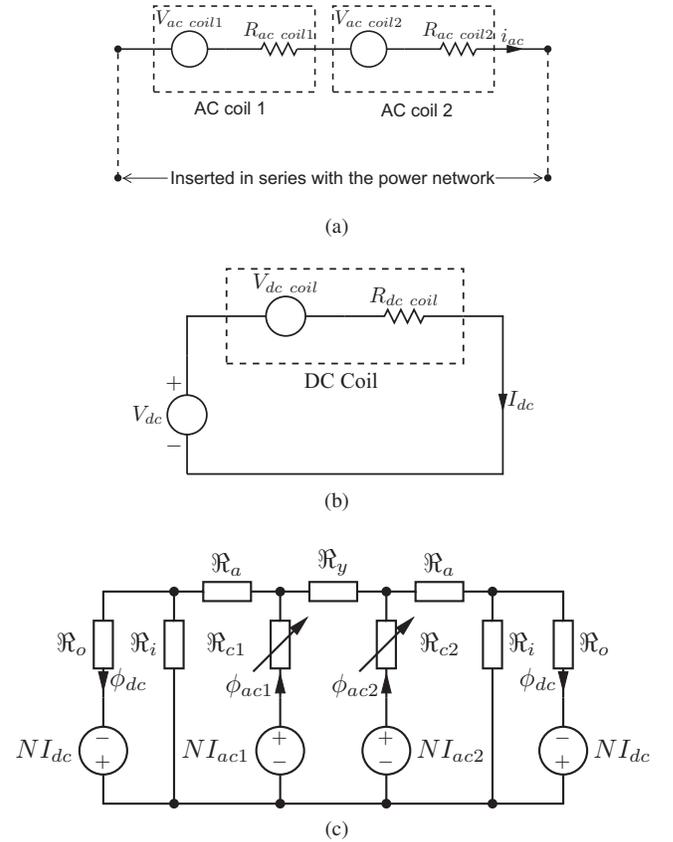

Fig. 1. PSCAD/EMTDC model of the FCL (a) AC circuit (b) DC circuit (c) Magnetic reluctance circuit
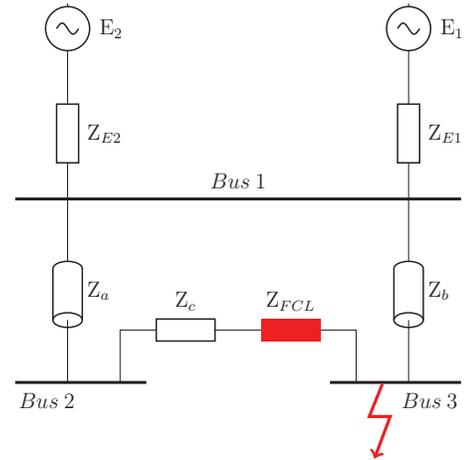
Fig. 2. $11\,kV$ test distribution system

reluctance circuit of the FCL (shown in Fig. 1c) were obtained from flux measurements using FEA [12], [13]. Table II summarises the model parameters including the values of the leakage reluctance elements derived for this particular saturated core FCL device. A characteristic reluctance curve, developed using the methodology set out in [12], was used to estimate the core reluctances $\Re_{c1}$ and $\Re_{c2}$.

Table I
POWER SYSTEM PARAMETERS

Parameter	Value	Unit
System voltage (Line to line, RMS)	11	kV
Nominal frequency	50	Hz
Source MVA base (3 phase) (each)	100	MVA
Source series resistance (each)	0.03104	p.u.*
Source series reactance (each)	0.19868	p.u.*
Line impedance (each for Z_a and Z_b)	0.00273+j0.01708	p.u.
Impedance of the shorted bus-tie (Z_c)	$j1.0e^{-05}$	p.u.

*p.u. on machine base MVA

Table II
FCL MODEL PARAMETERS

Parameter	Value	Unit
AC voltage (Line to line, RMS)	11	kV
DC bias	87	kAT
Number of turns: AC coil	64	–
AC coil resistance	0.04023	Ω
Number of turns: DC coil	200	–
DC coil resistance	0.0702	Ω
$\Re_y$ [a]	322	AT/Wb
$\Re_a$ [a]	1748	AT/Wb
$\Re_i$ [a]	10906000	AT/Wb
$\Re_o$ [a]	5	AT/Wb

[a]Leakage reluctance elements of the FCL equivalent electric circuit as indicated in Fig. 1

C. Initial PSCAD/EMTDC Network Simulations

The test system was modelled in PSCAD/EMTDC using the system parameters specified in Table I. Subsequent simulations were carried out in PSCAD/EMTDC with and without the saturated core FCL model inserted to the bus-tie.

During normal operation, both busbars are fed approximately the same current and a very small current passes through the bus tie. When a three-phase to ground fault was applied at Bus 3, without the FCL in the network, the fault current contribution fed from each source was approximately the same with a steady-state current of 24.5kA rms, as illustrated in Fig. 3a and Fig. 3b (red dashed waveforms). The fault current contribution from each source when the bus-tie FCL is in service is also shown in Fig. 3a and Fig. 3b (blue solid waveforms). Note that, the current contribution from Bus 2, which flows through the bus-tie FCL, has been limited to 3.8kA rms (84% reduction). However, the contribution from Bus 3 is directly fed and is approximately 40.46kA rms, a 77% increase when compared to the case without the FCL.
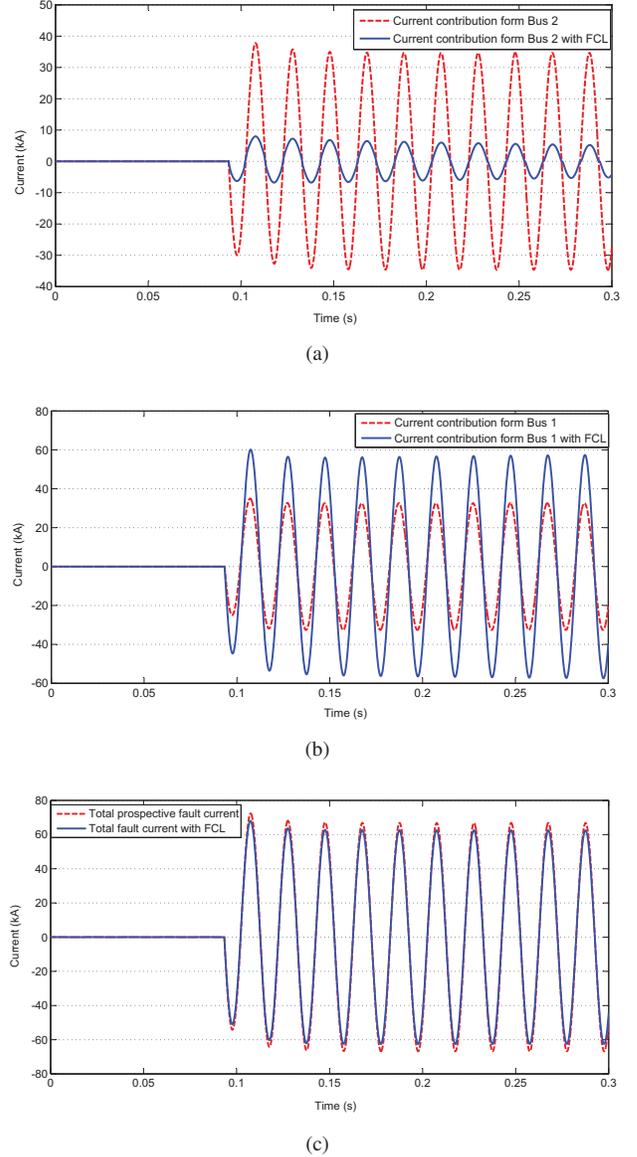

(a)

(b)

(c)

Fig. 3. The fault currents with and without the bus-tie FCL in service (a) contribution fed from Bus 2 (b) contribution fed from Bus 1 (c) total fault current

Consequently, the total fault current clipping achieved by the FCL for this particular fault scenario was 7% as shown in Fig. 3c.

IV. NUMERICAL CALCULATIONS

A. Derivation of Bus Impedance Matrices

To understand and theoretically verify the PSCAD/EMTDC simulation results in Section III, a fault analysis of the 11kV test system using a bus impedance matrix approach was carried out. For the network shown in Fig. 2, without the bus-tie FCL, the bus impedance matrix Z_{bus} derived using the impedance values in Table I is given by,

$Z_{bus} =$

$$0.01 \begin{bmatrix} 1.55 + j9.93 & 1.55 + j9.93 & 1.55 + j9.93 \\ 1.55 + j9.93 & 1.68 + j10.78 & 1.68 + j10.78 \\ 1.55 + j9.93 & 1.68 + j10.78 & 1.68 + j10.78 \end{bmatrix} \quad (1)$$

where each element Z_{ii} on the principal diagonal represents the Thevenin impedance at Bus i and the off-diagonal elements represent the transfer impedances of the buses.

When modifying a bus impedance matrix by adding a new branch impedance Z_o, between buses m and n, each original element of Z_{ij} can be modified as [14],

$$Z_{ij\,(new)} = Z_{ij} - \frac{(Z_{im} - Z_{in})(Z_{mj} - Z_{nj})}{Z_{mm} + Z_{nn} - 2Z_{mn} + Z_o} \quad (2)$$

The effect of inserting an FCL with a fault impedance of Z_{FCL} into the bus-tie can be considered as adding a new branch with the following impedance to the system [15]:

$$Z_T = (-Z_c)//(Z_c + Z_{FCL}) = -\frac{Z_c(Z_c + Z_{FCL})}{Z_{FCL}} \quad (3)$$

where Z_c is the original line impedance of the bus-tie (before inserting the FCL).

Therefore the modification to the entries of Z_{bus} when the bus-tie FCL is active (during a fault) in the bus-tie between Buses 2 and 3 is given by,

$$Z_{ij\,(new)} = Z_{ij} - \frac{(Z_{i2} - Z_{i3})(Z_{2j} - Z_{3j})}{Z_{22} + Z_{33} - 2Z_{23} + Z_T} \quad (4)$$

Similar to most FCL technologies, the actual FCL impedance during a fault event is not a constant for saturated core FCLs. Hence, the fault impedance of an FCL is typically defined as the equivalent steady-state impedance that would result in the same fault current limiting effect [6]. Based on this definition the fault impedance of the FCL device in Section III-B can be estimated to be, $Z_{FCL} = 0.267\Omega$. Using this Z_{FCL} estimation, the modified bus impedance matrix with the bus-tie FCL in service is,

$Z_{bus,\,FCL} =$

$$0.01 \begin{bmatrix} 1.55 + j9.93 & 1.55 + j9.93 & 1.55 + j9.93 \\ 1.55 + j9.93 & 1.79 + j11.55 & 1.58 + j10.03 \\ 1.55 + j9.93 & 1.58 + j10.03 & 1.79 + j11.55 \end{bmatrix} \quad (5)$$

As can be seen from (5), the Thevenin's impedance of the network at Bus 2 ($Z_{22,\,FCL}$) and Bus 3 ($Z_{33,\,FCL}$) increase, while the transfer impedance elements Z_{23} and Z_{32} decrease, when the bus-tie FCL in service.

B. Fault Current Calculations

Assuming a three-phase to ground fault was applied at Bus 3, the short-circuit currents for the test system shown in Fig. 2 were calculated with and without the FCL inserted to the system. The expressions derived to calculate the total fault current at Bus 3, and the fault currents contributed to Bus 3 by the adjacent unfaulted buses (Bus 1 and Bus 2) are given in Table III. Note that, in deriving these equations, the faulted network was assumed to be without load before the fault occurred and hence with no pre-fault current flow. Following that assumption, all bus voltages in the test system were then assumed to be the same as the pre-fault voltage at the faulted bus (V_i).

Table III
FAULT CURRENT CALCULATIONS - WITH AND WITHOUT THE BUS-TIE FCL

	Without FCL	With FCL
Total fault current at Bus 3, $I_{3,f}$	$\dfrac{V_i}{Z_{33}}$	$\dfrac{V_i}{Z_{33,\,FCL}}$
Current contribution from Bus 1, $I_{13,f}$	$\dfrac{V_i}{Z_b}\left(1 - \dfrac{Z_{13}}{Z_{33}}\right)$	$\dfrac{V_i}{Z_b}\left(1 - \dfrac{Z_{13,\,FCL}}{Z_{33,\,FCL}}\right)$
Current contribution from Bus 2, $I_{23,f}$	$\dfrac{V_i}{Z_c}\left(1 - \dfrac{Z_{23}}{Z_{33}}\right)$	$\dfrac{V_i}{Z_c + Z_{FCL}}\left(1 - \dfrac{Z_{23,\,FCL}}{Z_{33,\,FCL}}\right)$

where the pre-fault voltage at Bus 3 is given by V_i, the elements of the original bus impedance matrix in (1) are denoted by Z_{ij}, and elements of the modified bus impedance matrix (with the bus-tie FCL in service) are denoted by $Z_{ij,\,FCL}$.

Using the expressions derived for the fault current contributions (given in Table III) and the bus impedance matrices of the system (Z_{bus} and $Z_{bus,\,FCL}$), the fault current magnitudes were calculated over a range of FCL impedance values. Note that, the pre-fault voltage at the faulted bus (Bus 3) was assumed to be $V_i = 1.0\,pu$ and the FCL impedance values were varied from 0 to $0.4\,pu$. Fig. 4a shows how the Thevenin's impedance of the network at the faulted Bus 3 varies with the FCL impedance. The Thevenin's impedance of the network increases rapidly as the magnitude of the FCL impedance is increased, and subsequently plateaus at higher FCL impedance values. The resulting variation of total fault current ($I_{3,f}$) at Bus 3, with the FCL impedance is shown in Fig. 4b. As expected, the total fault current decreases with the addition of the FCL. However the decay is exponential and hence, the additional clipping offered by higher values of FCL impedance is marginal. The fault current contributed to Bus 3 by adjacent unfaulted Bus 2 and Bus 1 are shown in Fig. 4c and Fig. 4d respectively. While the fault current that flows through the FCL from Bus 2 side is reduced by the FCL action, the fault current that is directly fed to Bus 3 from Bus 1 increases when the bus-tie FCL is in service. Note that, these calculated bus impedance matrices and the behaviour of the resulting fault current contributions, corroborate with the PSCAD/EMTDC simulated results presented in Section III-C.
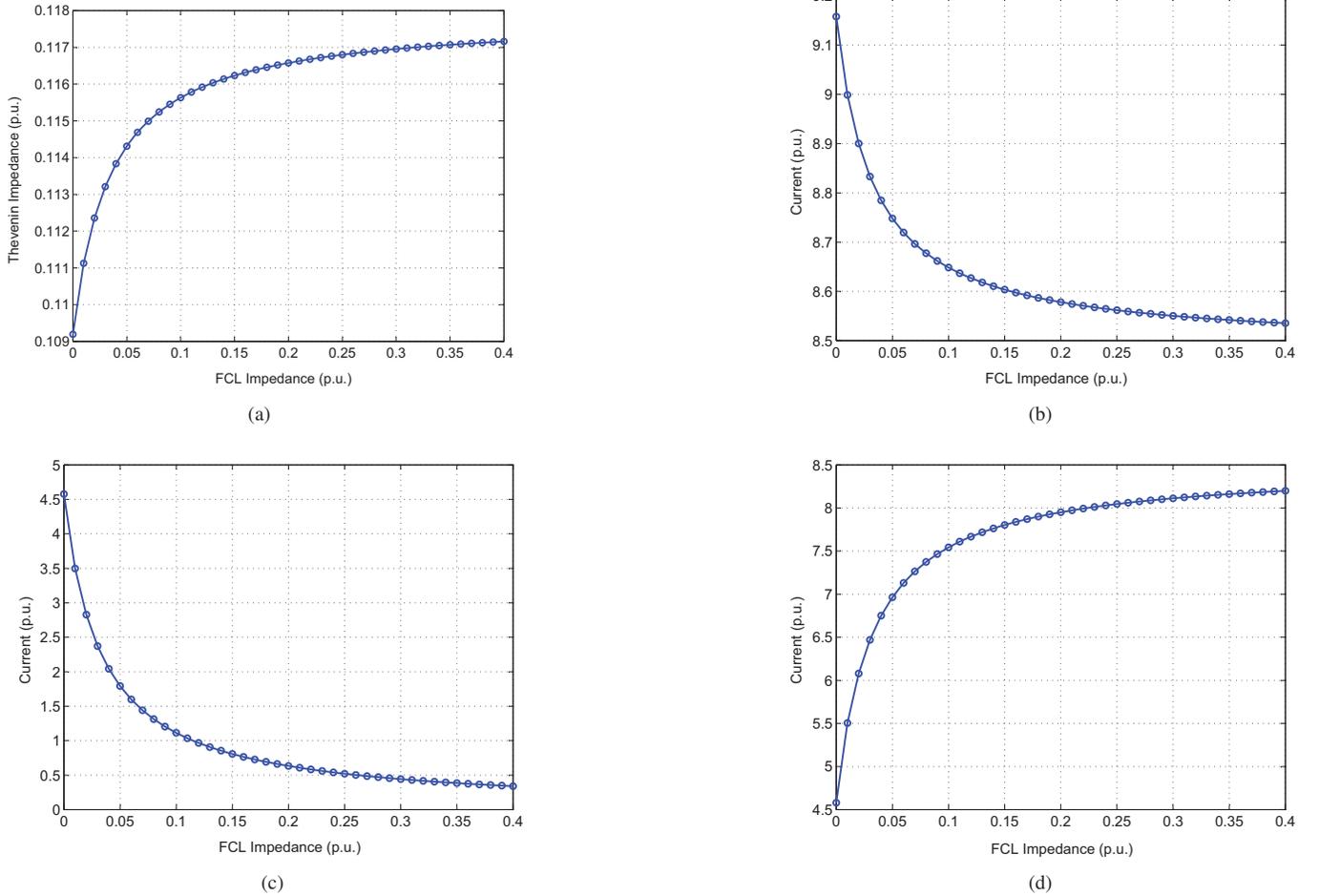
Fig. 4. Effect of bus-tie FCL impedance on (a) Thevenin impedance of the network at Bus 3 (Z_{33}) (b) total 3-phase to ground fault current at Bus 3 ($I_{3,f}$) (c) fault current contribution from Bus 2 ($I_{23,f}$) (d) fault current contribution from Bus 1 ($I_{13,f}$)

V. DISCUSSION

In Sections III and IV it was shown that installing a single FCL at a bus-tie location, in an interconnected circuit, may not provide the desired fault current reduction. In such cases, multiple FCLs may need to be applied at critical locations of the circuit to achieve the necessary fault current reduction. For the 11kV test system, installation of two identical FCLs, one in each incoming feeder, was considered as a possible solution, as illustrated in Fig. 5. Each FCL was modelled with the design parameters given in Table II. When a three-phase to ground fault was applied at Bus 3, the total fault current at Bus 3 and the fault currents contributed to Bus 3 by the adjacent unfaulted buses (Bus 1 and Bus 2), with and without the FCLs, are shown in Fig 6. The fault current contribution fed from each source, with the in feeder FCLs in service, was approximately 9.95 kA rms at the steady-state (58% reduction), as illustrated in Fig. 6a and Fig. 6b. Consequently for this particular fault scenario, the total fault current at Bus 3 with the in feeder FCLs, was approximately 19.88 kA rms (58% reduction).

In a large power system with complex interconnections, suppression of fault currents may need many FCLs. However, installation of multiple FCL devices (one or two FCLs per
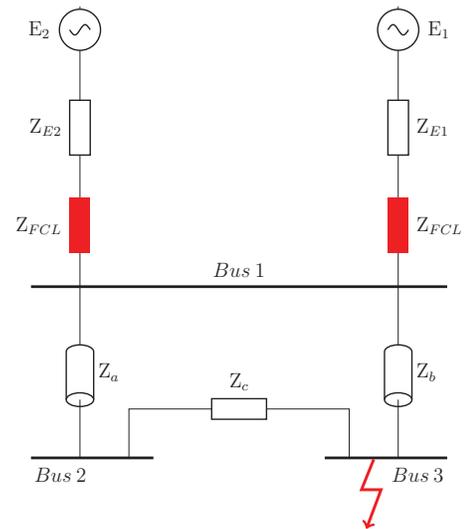

Fig. 5. $11\,kV$ test distribution system with multiple FCLs

circuit) may not be an economically viable solution. Several methods have been proposed to determine the optimum number and the best placement of FCLs (for S/N transition-type superconducting FCLs [15] and rectifier-type superconducting FCL [16]) for a meshed system. A technique similar to those in [15], [16] may need to be adopted when determining optimum placement for saturated core FCLs in a meshed/looped network.
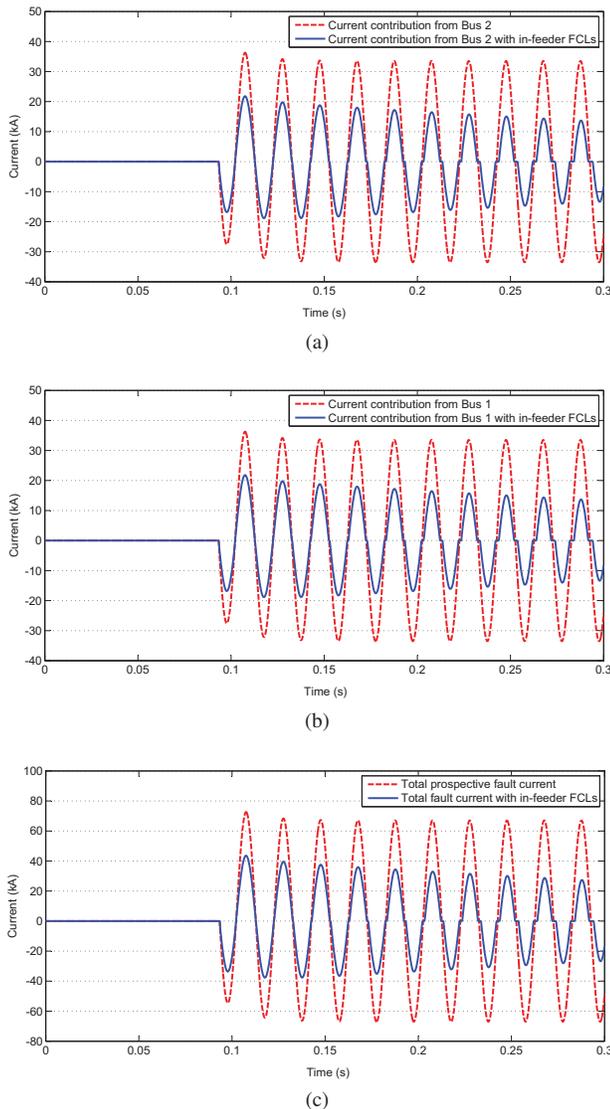

Fig. 6. The fault currents with and without the in feeder FCLs in service (a) contribution fed from Bus 2 (b) contribution fed from Bus 1 (c) total fault current

VI. CONCLUSIONS

The potential performance of a saturated core FCL in an interconnected 11kV distribution system was analysed in this paper, utilising a new comprehensive time-domain model of the FCL. A potential FCL design was presented for the test network, and the efficacy of an FCL device placed on a bus-tie location, in a looped circuit, was investigated using PSCAD/EMTDC simulations. It was shown that while the bus-tie FCL limits the current that flows through it, the current contribution that is directly fed to the fault from the opposite side significantly rises. Hence, the total effective current limiting achieved by the FCL was shown to be marginal. Through a numerical approach to fault analysis, the simulation results were theoretically verified, with the effects of the bus-tie FCL impedance on the fault current contributions by the adjacent unfaulted buses demonstrated. It was also shown that, in such an interconnected system, in order to to achieve the desired fault current reduction effect, application of multiple FCLs at critical locations of the circuit is necessary. However, cost might be a prohibitive factor in implementing this commercially and hence a suitable FCL placement technique may need to be adopted when determining optimum placement for saturated core FCLs in interconnected systems.

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