Impacts of crystal orientation of GaAs on the interfacial structures and electrical properties of Hf0.6La0.4Ox films

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Abstract
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Keywords
electrical, properties, hf0.6la0.4ox, structures, films, gaas, orientation, crystal, impacts, interfacial

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One of the major challenges in realizing the GaAs channel in the metal oxide semiconductor field effect transistor is the degrading in electron transport properties at the interface between GaAs and the gate oxide. In this study, Hf$_{0.6}$La$_{0.4}$O$_x$ gate oxide films were deposited at a low temperature (200°C) on GaAs(111)A and GaAs(100) substrates by plasma enhanced atomic layer deposition. Microstructure analysis indicates that residuals of gallium oxide, arsenic oxide, and As element remained at the interface of Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(100). On contrast, a smoother interface is observed between Hf$_{0.6}$La$_{0.4}$O$_x$ thin film and GaAs(111)A substrate. Furthermore, a reduction of interfacial layer is observed in Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A. Electrical characterization of the metal-insulator-semiconductor Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(111)A capacitor indicated a reduction of $D_i$ and leakage current compared with the capacitor fabricated on GaAs(100).

I. INTRODUCTION

With the continuous down scaling of complementary metal oxide semiconductor (CMOS) devices, searching for new materials to provide enhanced performance and stability for CMOS is in need. GaAs channel materials attracts considerable attentions for developing metal oxide semiconductor field effect transistors (MOSFETs) because of its higher intrinsic electron mobility and lower effective mass compared to Si. However, realizing GaAs’s potential in this regard has proven to be difficult, partly due to the highly reactive GaAs surface. The complex native oxides of GaAs is quite unstable, it’s structure and properties can be affected when exposed to light, moisture, or even with moderate heat treatments. The native oxide of GaAs presents a surface that is neither easily characterized nor passivated. A lot of efforts have been made to improve the interface quality of conventional high-k oxide GaAs. Recently, significant improvements of MOS transistor’s performance have been achieved through replacing the surface orientation of traditional GaAs(100) or Hf$_{0.55}$Ga$_{0.47}$As by the polar GaAs(111)A (Ga or In-rich) crystal face, in combination with thermal atomic layer deposition (ALD) of Al$_2$O$_3$.

HfO$_2$ is one of the most promising high-k candidates for future CMOS devices, however, HfO$_2$ on GaAs showed abnormal capacitance-voltage (C-V) characteristics with no accumulation observed, which is attributed to the native oxides induced interface pining between GaAs substrate and HfO$_2$. Fortunately, by doping La into HfO$_2$ to form HfLaO$_x$, the performance of gate dielectrics can be enhanced considerably due to its high permittivity, relatively large conduction band (CB) offset, high crystallization temperature, and less Fermi-level pinning.

GaAs has a zinc blende structure with double fcc cubic lattice of Ga atoms and As atoms. At the (111) directions, atomic planes are occupied alternatively by Ga and As atoms forming double layers, each atom has 3 bonds within the same double layer and one bond in the exterior of the double layer (Figure 1). The surfaces terminated by Ga atoms are called [111]A, of which we will be focusing on in this work. On the other hand, along the (100) directions the atomic planes are also occupied alternatively by Ga and As atoms. However, the planes are equidistant and each atom is symmetrically bonded with neighboring layers. The [111]A facets maybe more stable assuming that the three bonds (within the same double layer) are much more difficult to break. In this paper, we will discuss the influence of the

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**FIG. 1. Schematic atomic displacement of GaAs in (111)A and (100) orientation.**

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crystal orientation of GaAs on the interfacial structures and the electrical properties of Hf$_{0.6}$La$_{0.4}$O$_x$ gate dielectrics.

II. EXPERIMENT

N-type GaAs substrates in (100) and (111)A orientation were used in this work. It is reported a high La/(La + Hf) atomic ratio results in a better thermal stability than pure HfO$_2$.$^{11}$ However, high La/(La + Hf) atomic ratio would lead to a low deposition rate. Thus, in this work, we choose the La percentage around 40%. The plasma enhanced ALD (PEALD) system was used to prepare Hf$_{0.6}$La$_{0.4}$O$_x$ dielectric films. GaAs substrates were cleaned by acetone and alcohol for 10 min and then in a dilute HCl solution (HCl:H$_2$O = 1:1) for 1 min to remove organic and native oxide, respectively. Hf[N(CH$_3$)(C$_2$H$_5$)$_2$]$_4$ and La[N(TMS)$_2$]$_3$ were used as metal precursors, and O$_2$ plasma served as oxidant. The growth temperature was set to 200°C. The total deposition of Hf$_{0.6}$La$_{0.4}$O$_x$ film on GaAs substrate consists of 10 cycles of alternately deposited La$_2$O$_3$-HfO$_2$ nanolaminates and 5 cycles of HfO$_2$ cap layer to avoid hydrolyzed of La-component when exposed in air. Each nanolaminates cycle consists of three sub-cycles La$_2$O$_3$ and one sub-cycle HfO$_2$: 3 cycles of La$_2$O$_3$ is first deposited on GaAs surface and then followed by 1 cycle HfO$_2$.

As we known, due to the interfacial traps between the dielectric film and GaAs substrate which induced interface pining near the midgap, directly deposited high-k gate dielectrics on GaAs sometimes even showed abnormal capacitance voltage (C-V) characteristics with no accumulation observed.$^{12}$ Chang et al.$^{13}$ investigated the impacts of post-deposition annealing (PDA) on the GaAs MOS device; they found that post annealing lead to significant reduction of interfacial state density ($D_{it}$) near the midgap. Moreover, the post annealing higher than 500°C would result in a charge transfer effect between La and Hf and improve the Hf-La-O bonding state.$^{14}$ However, annealing temperature higher than 550°C would lead to a thicker interfacial layer which deteriorates the interfacial quality.$^{12}$ Therefore, we carried out a PDA in a N$_2$ ambient at 500°C for 1 min by the rapid thermal annealing (RTA) technique. Metal-insulator-semiconductor (MIS) capacitors were formed with a Pt top electrodes formed by shadow mask sputtering, and a bottom electrode formed by blanket sputtering of Pt. Post metallization annealing (PMA) in forming gas (5% H$_2$/95% N$_2$) at 450°C was performed to form ohmic contact. The microstructure and chemical states were analyzed by cross-sectional high resolution transmission electron microscopy (HRTEM) and X-ray photoelectron spectroscopy (XPS). High frequency capacitance-voltage (C-V) and leakage current-voltage (J-V) measurements of the MIS capacitors were carried out using an Agilent B1500A Semiconductor Device Analyzer.

III. RESULTS AND DISCUSSION

A. Interfacial microstructures

Interfacial morphology was studied using cross-sectional TEM. It is shown in Figure 2 that the interface of the Hf$_{0.6}$La$_{0.4}$O$_x$ on GaAs(111)A is smoother than that on GaAs(100). A reduction of interfacial layer is observed on the GaAs(111)A-substrate film. The thickness of the Hf$_{0.6}$La$_{0.4}$O$_x$ film is 9.6 nm and 8.2 nm on GaAs(100) and GaAs(111)A, respectively. The reduction of the film thickness was partially due to the reduction of the interfacial layer, and the deposition rate was found to be different on the GaAs substrates with different orientations.

To further investigate the chemical structure of the interface between the Hf$_{0.6}$La$_{0.4}$O$_x$ films and the GaAs substrates, XPS measurements were performed to determine the interfacial structures. XPS was performed ex-situ using a monochromatic Al K$_x$ X-ray source at a power of 150 W. The binding energy was calibrated with the position of C 1s peak at 284.8 eV. According to the XPS analysis, the atomic ratio of La/(La + Hf) in Hf$_{0.6}$La$_{0.4}$O$_x$ is 40.9% and 41.9% for the film deposited on GaAs(100) and GaAs(111) A, respectively. Arsenic oxides were commonly observed in the XPS results of the thin films deposited on GaAs(100), which was generally located at 43.20 eV, 43.98 eV, and 44.86 eV corresponding to AsO, As$_2$O$_3$, and As$_2$O$_5$, respectively. The As 3d spectra of Hf$_{0.6}$La$_{0.4}$O$_x$ on GaAs(111)A is shown in Figure 3(a), besides the strongest peak of As-Ga bond, there is a weak peak at 43.20 eV which is ascribed to AsO, As$_2$O$_3$, and As$_2$O$_5$, respectively. The As 3d spectra of Hf$_{0.6}$La$_{0.4}$O$_x$ on GaAs(100) as shown in Figure 3(c), besides the As-Ga bond, two peaks located at 43.57 eV and 44.47 eV related to Arsenic oxide was...
detected, indicating the existence of residual As$_2$O$_3$ and As$_3$O$_5$ at Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(100) interface. Furthermore, the As element at 42.28 eV was also detected at the interface due to the exchange reaction between GaAs substrate and Arsenic oxide.\textsuperscript{16} For the Ga 2p spectra (Figures 3(b) and 3(d)), gallium oxide was detected in both of the samples. There are two possible causes responsible for the Ga-O bond, one is the residual Ga$_2$O$_3$ exists at the interface; the other is that the Ga$_2$O$_3$ is formed by the scattering during ALD growth and PDA process. Although there are peaks from As-O and Ga-O bonds detected in both of the samples, we observe a reduction of Ga$_2$O$_3$ and Arsenic oxides in Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A. Based on these XPS results, the ALD growth on GaAs(111)A substrate would minimum amount of interfacial Ga$_2$O$_3$ and arsenic oxides which is responsible for causing large D$_{it}$ and Fermi level pinning.\textsuperscript{12} Thus, GaAs(111)A would be more favorable as a substrate for high-k dielectrics.

### B. Band alignment of Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A

One of the most fundamental physical properties for characterizing a semiconductor interface is the band alignment. In order to determine the CB offset value, the band gap ($E_g$) energies of the Hf$_{0.6}$La$_{0.4}$O$_x$ films on GaAs(111)A were determined from O 1s energy loss for photoelectrons. In Figure 4(a), the onset of band to band excitation which corresponds to $E_g$ is defined as an intercept of linear extrapolation of the leading edge to the background level. The $E_g$ was determined to be 4.33 eV for the Hf$_{0.6}$La$_{0.4}$O$_x$ film. To study the relationship of the energy band for Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A, the valence band (VB) spectra were measured for the Hf$_{0.6}$La$_{0.4}$O$_x$ films grown on GaAs(111)A substrates, as well as the bare GaAs(111)A samples, after the Ar$^+$ etching of the XPS measurements. The measurement is based on the assumption that the energy difference between the core level and VB edge of the GaAs substrate remains constant with/without the deposition of Hf$_{0.6}$La$_{0.4}$O$_x$ films.\textsuperscript{17} Figure 4(b) shows the VB spectra of GaAs(111)A substrate and the as-received Hf$_{0.6}$La$_{0.4}$O$_x$ film on GaAs(111)A. In our work, the As 3d peak and VB edge from the GaAs(111)A substrate were chosen as the reference to determine the VB offset between the Hf$_{0.6}$La$_{0.4}$O$_x$ film and GaAs(111)A substrate. The core level positions and VB maximum of bulk materials combined with core level difference of heterojunction are used to calculate the VB offset. The VB maximum is determined by using a linear extrapolation method.\textsuperscript{17} The Hf$_{0.6}$La$_{0.4}$O$_x$ VB offset can be obtained by eliminating the VB spectra of the GaAs substrate from the Hf$_{0.6}$La$_{0.4}$O$_x$ VB spectrum using the following formula:

$$\Delta E_v = \left( E_{As3d}^{As3d} - E_v^{GaAs} \right)_{GaAs} - \left( E_{Hf4f}^{Hf4f} - E_{HLO}^{HLO} \right)_{HLO}$$

where $E_{As3d}^{As3d}$ and $E_{Hf4f}^{Hf4f}$ are the binding energy of As 3d and Hf 4f, $E_v^{GaAs}$ and $E_{HLO}^{HLO}$ are the VB maximum of GaAs and Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs. Consequently, the VB offset value is 1.61 eV obtained at the top of the VB maximum at the Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs interface. The CB offset can be evaluated by subtracting the VB offset and the $E_g$ of GaAs substrate from the $E_g$ of Hf$_{0.6}$La$_{0.4}$O$_x$ film by the following formula:\textsuperscript{18}

$$\Delta E_{C}^{High-k/GaAs} = \Delta E_{High-k/GaAs}^{As} - \Delta E_{High-k/GaAs}^{Hf} - \Delta E_{g}^{GaAs}$$

where $\Delta E_{C}^{High-k/GaAs}$ represents the CB offset between high-k films and GaAs, $\Delta E_{High-k/GaAs}^{As}$ is the band gap of high-k, $\Delta E_{High-k/GaAs}^{Hf}$ is the VB offset between high-k and GaAs, and $\Delta E_{g}^{GaAs}$ is the band gap of GaAs which is 1.42 eV. Consequently, the Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A CB offset ($\Delta E_{C}^{High-k/GaAs}$) is calculated to be 1.30 eV. The energy band diagram for Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A stack is obtained as Figure 4(c).
C. Electrical properties

The capacitance-voltage (C-V) and the leakage current density-voltage (J-V) of Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(111)A and Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(100) MIS capacitors were measured using a HP4194A impedance analyzer and an Agilent 4156 C precision semiconductor parameter analyzer, respectively. As shown in Figure 5(a), the C-V measurements were performed at 10 kHz and 1 MHz. In the top inset of Figure 5(a), the inversion, depletion, and accumulation modes are clearly shown in the C-V curves, a frequency dispersion ($\Delta C_{ox}$) in accumulation is also observed, which suggests that a high leakage current exists in both of the samples while applying high voltage. $\Delta C_{ox}$ between 10 kHz and 1 MHz is evaluated as 10.1% and 16.2% for Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A and Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(100), respectively. In GaAs/high-k system, the complex nature of the interface with a high density of interface states (Dit) can exhibit an interface state capacitance (Cit) that contributes significantly to the measured capacitance. The existence of Cit is also responsible for the frequency dispersion which is origin from a low resistivity interfacial layer adjacent to the interface.\textsuperscript{19}

The reduction of frequency dispersion in Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A indicates a suppression of the interface traps. In order to remove the effect of leakage current and interface states,\textsuperscript{20,21} an equivalent circuit is used to correct the capacitance as shown in the left bottom of Figure 5(a). The actual frequency independent capacitance (C$_{true}$) can be calculated as follows:\textsuperscript{22}

\[
C_{true} = \frac{(\omega^2 C_m C_E - G_m^2 - \omega^2 C_m^2)(G_m^2 + \omega^2 C_m^2)C_E}{(\omega^2 C_E^2)|G_m(1 - R'_m G_m) - \omega^2 R'_m C_E^2|^2 + (\omega^2 C_m^2 + G_m^2 - \omega^2 C_m C_E)^2},
\]

where $R'_m = \frac{G_m}{G_m + \omega^2 C_m}$ and $C_E = \frac{-C_{ox}(G_m^2 + \omega^2 C_m^2)}{\omega^2(C_m^2 + C_E C_{ox}) + G_m^2}$. $C_m$ and $G_m$ are the measured capacitance and conductance, respectively. $C_{ox}$ and $G_{ox}$ represent the measured capacitance and conductance in strong accumulation, respectively. $C_{ox}$ is the maximum accumulation capacitance, $\omega$ denotes angular frequency. From the actual frequency independent device capacitance curves as shown in Figure 5(a), the $C_{ox}$ of Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(111)A capacitor is 2.5 $\mu$F/cm$^2$ higher than that of Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(100) (2.3 $\mu$F/cm$^2$). The slope of the C-V curve of Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(111)A is greater than that of Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(100), which indicates that the interface trap density is lower in Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A. However, the C-V curve of Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A in depletion region stretches out indicates a presence of slow interface states in GaAs band gap. The equivalent oxide thickness (EOT) for Hf$_{0.6}$La$_{0.4}$O$_x$/GaAs(111)A and GaAs(100) is about 1.4 nm and 1.5 nm, the corresponding $k$ value of as-deposited Hf$_{0.6}$La$_{0.4}$O$_x$ film is 22.8 and 24.9, respectively. The corresponding interfacial state density (D$_{ox}$) of the samples is extracted by the
conductance method. The $D_{it}$ at midgap of the band gap energy is $1.62 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$ and $3.25 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$ for Hf$_0.6$La$_0.4$O$_x$/GaAs(111)A and Hf$_0.6$La$_0.4$O$_x$/GaAs(100), respectively. Lower $D_{it}$ value for Hf$_0.6$La$_0.4$O$_x$ film on GaAs(111)A indicated a better interface quality. This result is consistent with the TEM and XPS result. We have to note that the $D_{it}$ is still as high as $10^{12}$ order of magnitude which is due to the injection from substrate. We consider that the underestimate $\varepsilon_r$ value is due to the existence of low permittivity interfacial layer between Hf$_0.6$La$_0.4$O$_x$ film and GaAs substrate.

For F-P emission, the current density is given by

$$J_{FP} = J_0 \exp \left( \frac{q(-\varphi_{FP} + \sqrt{qE/\pi\varepsilon_0\kappa})}{kT} \right).$$

(4)

In addition, the current density due to Schottky emission can be expressed as follows:

$$J_S = A^*T^2 \exp \left( \frac{q(-\varphi_B + \sqrt{qE/4\pi\varepsilon_0\kappa})}{kT} \right).$$

(5)

Moreover, ohmic transportation can be expressed as

$$J_O = AE \exp(\Delta E_{ac}/kT),$$

(6)

where $J_O$ represents low field current density, $A^*$ is Richardson constant, $q$ denotes electronic charge, $\epsilon_r$ represents dynamic dielectric constant, $\kappa$ is Boltzmann constant, $T$ denotes absolute temperature, $\varphi_{FP}$ is the height of trap potential well, $\varphi_B$ represents contact potential bottleneck, $A$ is a constant, $\Delta E_{ac}$ represents the activation energy of the electron, and $E$ denotes applied electric field. The inset of Figure 5(b) plots $J$ vs. $E$ at low electric field from 0.1 to 0.5 MV/cm, a linear shape suggests that the conduction mechanism at low electric field is ohmic transportation which is due to the injection from substrate. Figures 5(c) and 5(d) show a logarithmic current density divided by the electric field as a function of the square root of the electric field [$\ln(J/E)$ vs. $E^{1/2}$] and a logarithm of the current density versus the square root of electric field [$\ln(J)$ vs. $E^{1/2}$], respectively. A linear fitting appears while the applied electric field ($E^{1/2}$) in the range of 0.5–1.3 (MV/cm)$^{1/2}$ For F-P emission, the slope of the straight line is 10.4 and 18.7 for Hf$_0.6$La$_0.4$O$_x$/GaAs(111) and Hf$_0.6$La$_0.4$O$_x$/GaAs(100), respectively. As to Schottky emission, the slope for Hf$_0.6$La$_0.4$O$_x$/GaAs(111)A and Hf$_0.6$La$_0.4$O$_x$/GaAs(100) is 12.6 and 21.5, respectively. The dynamic dielectric constant ($\varepsilon_r$) could be extracted from the slope of the linear region. The slope of 21.5 for Hf$_0.6$La$_0.4$O$_x$/GaAs(100) and 12.6 for Hf$_0.6$La$_0.4$O$_x$/GaAs(111)A in Schottky emission is closer to the dielectric constant which is extracted by the C-V measurement. This indicates that when the $E^{1/2}$ is in the range of 0.5–1.3 (MV/cm)$^{1/2}$, Schottky emissions would be the dominant leakage mechanism in Hf$_0.6$La$_0.4$O$_x$ films on GaAs(100) and GaAs(111) due to a substrate injection. In general, the electrons generated under positive gate bias could be from the interfaces states, traps in depletion region and back electrode of substrate. We consider that the underestimate $\varepsilon_r$ value is due to the existence of low permittivity interfacial layer between Hf$_0.6$La$_0.4$O$_x$ film and GaAs substrate.

IV. SUMMARY AND CONCLUSIONS

Hf$_0.6$La$_0.4$O$_x$ film was successfully deposited on GaAs(111)A and GaAs(100) substrates by the PEALD method in which Hf[N(CH$_3$)$_2$]$_4$, La[N(TMS)$_2$]$_3$, and C$_2$H$_5$OH precursor and oxygen plasma as oxidant. Microstructure analysis shows a smooth interface and a reduction of interfacial layer between the Hf$_0.6$La$_0.4$O$_x$ films and the GaAs(111)A substrates. XPS results indicated a reduction of...
Ga$_2$O$_3$ and arsenic oxides in the interfacial layer between Hf$_{0.6}$La$_{0.4}$O$_x$ and GaAs(111)A. Electrical properties of Pt/Hf$_{0.6}$La$_{0.4}$O$_x$/n-GaAs(111)A MIS capacitors show a reduction of $D_{it}$ and leakage current comparing with the capacitor fabricated on GaAs(100).