Real-time FPGA realization of an UWB transceiver physical layer

Darryn W. Lowe
University of Wollongong

Recommended Citation
NOTE

This online version of the thesis may have different page formatting and pagination from the paper copy held in the University of Wollongong Library.

UNIVERSITY OF WOLLONGONG

COPYRIGHT WARNING

You may print or download ONE copy of this document for the purpose of your own research or study. The University does not authorise you to copy, communicate or otherwise make available electronically to any other person any copyright material contained on this site. You are reminded of the following:

Copyright owners are entitled to take legal action against persons who infringe their copyright. A reproduction of material that is protected by copyright may be a copyright infringement. A court may impose penalties and award damages in relation to offences and infringements relating to copyright material. Higher penalties may apply, and higher damages may be awarded, for offences and infringements involving the conversion of material into digital or electronic form.
REAL-TIME FPGA REALIZATION OF
AN UWB TRANSCEIVER PHYSICAL LAYER

A thesis submitted in fulfilment of the
requirements for the award of the degree

MASTER OF ENGINEERING – RESEARCH

from

UNIVERSITY OF WOLLONGONG

by

Darryn W. Lowe, BEng (Hons 1)
School of Electrical, Computer and Telecommunications Engineering
2005
I, Darryn W. Lowe, declare that this thesis, submitted in partial fulfilment of the requirements for the award of Master of Engineering – Research, in the School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, is wholly my own work unless otherwise referenced or acknowledged.

The document has not been submitted for qualifications at any other academic institution.

Darryn W. Lowe
14 November 2005
Contents

1 Introduction .............................................................. 1
  1.1 Design Methodology ................................................. 3
  1.2 Contributions ....................................................... 5

2 A Novel UWB PHY ......................................................... 9
  2.1 MCIDS ................................................................. 10
  2.2 CCDM ................................................................. 13
  2.3 Specification .......................................................... 19
    2.3.1 Preamble .......................................................... 21
    2.3.2 SFD ............................................................... 22
    2.3.3 PHY Header Definition ............................................. 22
    2.3.4 HCS ............................................................... 24
    2.3.5 Scrambling ........................................................ 24
    2.3.6 Symbol Mapping ................................................... 25
    2.3.7 Prespreading ..................................................... 27
    2.3.8 CCDM .............................................................. 27
    2.3.9 Pilot Insertion .................................................... 27
    2.3.10 MCIDS Spreading ............................................... 29
    2.3.11 Spectral Mask .................................................. 29

3 Transmitter ................................................................. 31
  3.1 Top-Level Architecture .............................................. 31
3.2 Bus Interfacing ........................................ 34
  3.2.1 Control Word .................................. 34
  3.2.2 Status Word ................................ 37
  3.2.3 Packet Buffer ................................ 38
3.3 Header Preparation .................................. 42
  3.3.1 Header Timing ................................ 43
  3.3.2 Header Check Sum ............................ 45
  3.3.3 Scrambler .................................... 45
3.4 Symbol Creation .................................... 46
  3.4.1 Symbol Buffer ................................ 47
  3.4.2 Constellation Mapping ........................ 55
3.5 CCDM .............................................. 59
  3.5.1 Spreading Architecture ....................... 62
  3.5.2 Control ...................................... 66
  3.5.3 Separating I/Q Components .................... 71
3.6 MCIDS ............................................. 71
  3.6.1 Buffering .................................... 72
  3.6.2 Pilot Insertion ................................ 76
  3.6.3 Preamble Generation ......................... 77
  3.6.4 Interleaving .................................. 79
  3.6.5 Spreading .................................... 83
  3.6.6 Transmitted Signal .......................... 83

4 Receiver ............................................... 87
  4.1 MCIDS Despreading ............................... 89
    4.1.1 MCIDS RAKE ................................ 91
    4.1.2 Frame Detection ............................ 105
    4.1.3 Equalization ............................... 111
    4.1.4 Automatic Gain Control ..................... 115
    4.1.5 DetectSFD .................................. 117
4.2 CCDM Demodulation ..................................... 119
  4.2.1 Removing Pilots ................................ 119
  4.2.2 Buffering .................................... 121
  4.2.3 Despreading .................................. 122
4.3 Constellation Demapping ................................ 130
  4.3.1 I/Q Buffer .................................. 130
  4.3.2 Demapping .................................. 134
4.4 Header Processing ................................... 138
  4.4.1 Data Rate Management ......................... 138
  4.4.2 Descrambling ................................ 138
  4.4.3 Header Validation ............................ 139
4.5 Bus .................................................. 139
  4.5.1 Packet Buffer ............................... 140
  4.5.2 Control Registers ............................ 141

5 Analysis .............................................. 145

5.1 Test Environment .................................... 145
  5.1.1 RF Front-end Models ......................... 145
  5.1.2 Channel Models ............................. 148
  5.1.3 MAC Models ................................. 150
5.2 Performance ........................................ 155
  5.2.1 AWGN ........................................ 155
  5.2.2 Multipath Channel ........................... 157
5.3 Sensitivity to Word Length ........................... 163
5.4 Complexity ......................................... 164
  5.4.1 Device Selection ................................ 164
  5.4.2 Synthesis Results ............................ 165

6 Conclusions .......................................... 167

A Transmitter Models .................................. 171
B Receiver Models

C Parametrization Scripts
   C.1 Constants .................................. 209
      C.1.1 Global Constants ....................... 209
      C.1.2 Parameters ............................ 211
   C.2 ROMs .................................... 214
      C.2.1 Transmitter CCDM Codeset ROM .......... 214
      C.2.2 Receiver CCDM Codeset ROM ............. 215
      C.2.3 Receiver MCIDS Codeset ROM ............ 215
      C.2.4 Receiver Synchronization Codeset ROM ... 216
      C.2.5 Receiver RAKE Correlator Interleaver ... 216

D Simulation .................................. 219
   D.1 Functional Blocks .......................... 219
      D.1.1 CRC ................................ 219
      D.1.2 Scrambler ............................. 220
      D.1.3 Constellation Mapping .................... 220
      D.1.4 CCDM .................................. 223
      D.1.5 Pilots .................................. 225
      D.1.6 Preamble .............................. 226
      D.1.7 MCIDS .................................. 226
   D.2 Simulation Framework ...................... 230
      D.2.1 Top-Level Simulation ..................... 230
      D.2.2 End-to-End Link Model .................... 231
      D.2.3 Packet Constructor ........................ 232
      D.2.4 Transmitter Baseband Model ............... 233
      D.2.5 Multipath Channel Model ................... 233
      D.2.6 Receiver Front-end Model .................. 235
      D.2.7 Receiver Baseband Model .................. 236
# List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Example of an MCIDS Spread Signal for $M = N = 4$</td>
<td>12</td>
</tr>
<tr>
<td>2.2</td>
<td>Example of MCIDS Despreading for $M = 4$</td>
<td>13</td>
</tr>
<tr>
<td>2.3</td>
<td>Preamble Sequence</td>
<td>22</td>
</tr>
<tr>
<td>2.4</td>
<td>SFD Sequence</td>
<td>22</td>
</tr>
<tr>
<td>2.5</td>
<td>PHY Header Definition</td>
<td>23</td>
</tr>
<tr>
<td>2.6</td>
<td>Data Rate Mappings for PHY Header</td>
<td>23</td>
</tr>
<tr>
<td>2.7</td>
<td>Initial Values for PRBS</td>
<td>25</td>
</tr>
<tr>
<td>2.8</td>
<td>Normalization Constants for Symbol Constellations</td>
<td>25</td>
</tr>
<tr>
<td>2.9</td>
<td>Prespread Codes</td>
<td>27</td>
</tr>
<tr>
<td>2.10</td>
<td>Transceiver Spectral Mask</td>
<td>29</td>
</tr>
<tr>
<td>3.1</td>
<td>Example of Buffer Signal Mask Generation</td>
<td>41</td>
</tr>
<tr>
<td>3.2</td>
<td>Derivation of Header Control Signal Constants</td>
<td>45</td>
</tr>
<tr>
<td>3.3</td>
<td>Data Bits for Modulation Types</td>
<td>49</td>
</tr>
<tr>
<td>3.4</td>
<td>Relationship between Symbol Density and FIFO Reads</td>
<td>54</td>
</tr>
<tr>
<td>3.5</td>
<td>Constellation Mapping for BPSK &amp; QPSK</td>
<td>58</td>
</tr>
<tr>
<td>3.6</td>
<td>Construction of $Out_{Code}$</td>
<td>69</td>
</tr>
<tr>
<td>3.7</td>
<td>Calculation of MCIDS Buffer Read Address</td>
<td>76</td>
</tr>
<tr>
<td>3.8</td>
<td>BPSK Modulation of Preamble Bits</td>
<td>78</td>
</tr>
<tr>
<td>4.1</td>
<td>Adder Coefficient Modification for RAKE Finger Correlator</td>
<td>98</td>
</tr>
<tr>
<td>4.2</td>
<td>MCIDS Code ROM</td>
<td>104</td>
</tr>
<tr>
<td>4.3</td>
<td>Synchronization Constants for RAKE Finger Correlators</td>
<td>107</td>
</tr>
</tbody>
</table>
List of Figures

1.1 Transceiver Development Methodology .................................................. 3
2.1 Transceiver Block Diagram ................................................................. 10
2.2 Example of CCDM Sequence Set for L=28 and K=2 .......................... 17
2.3 PHY Frame Format ........................................................................... 20
2.4 Example of Spreading Process for PHY Header ................................. 21
2.5 Bits-to-Symbol Mappings for BPSK, QPSK, 16-QAM and 64-QAM ........ 26
2.6 Codeset Definitions for CCDM and MCIDS ..................................... 28
2.7 Insertion of Pilots ............................................................................. 29
2.8 FCC Emissions Limit on UWB and Transceiver Spectral Mask ....... 30
3.1 Tx Overall Timing ............................................................................ 33
3.2 Transmitter Scrambler & HCS Timing .............................................. 42
3.3 Tx Map ......................................................................................... 48
3.4 Timing of **Tx-Map-Buffer-Group**A.22 Block .............................. 51
3.5 FIFO Refilling .............................................................................. 52
3.6 Counter Synchronization ................................................................. 57
3.7 Impact of Pre-spreading on Symbol Timing ..................................... 58
3.8 Timing of Transmitter’s CCDM Spreading .................................... 61
3.9 Architecture of CCDM Spreading ...................................................... 64
3.10 Tx CCDM Spreader Timing – Load Cycle ...................................... 68
3.11 Tx CCDM Spreader Timing – Write Cycle ..................................... 70
3.12 Tx MCIDS Buffer Addressing ......................................................... 73
5.6 Receiver State Machine ........................................... 154
5.7 Theoretical BER vs. $\frac{E_b}{N_0}$ in AWGN. ......................... 156
5.8 Simulated BER vs. $\frac{E_b}{N_0}$ in AWGN. .......................... 157
5.9 Simulated BER vs. $\frac{E_b}{N_0}$ in CM1. .............................. 158
5.10 Simulated BER vs. $\frac{E_b}{N_0}$ in CM2. .............................. 159
5.11 Simulated BER vs. $\frac{E_b}{N_0}$ in CM3. .............................. 160
5.12 Simulated BER vs. $\frac{E_b}{N_0}$ in CM4. .............................. 161
5.13 Simulated BER vs. $\frac{E_b}{N_0}$ for QPSK in all channels. .......... 162
5.14 Simulated PER vs. ADC Bit Width. .................................. 163
## List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog to Digital Convertor</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>ASR</td>
<td>Addressable Shift Register</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>CCDM</td>
<td>Complementary Code Division Multiplexing</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Convertor</td>
</tr>
<tr>
<td>DSSS</td>
<td>Direct Sequence Spread Spectrum</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal Communications Commission</td>
</tr>
<tr>
<td>FCS</td>
<td>Frame Check Sequence</td>
</tr>
<tr>
<td>FIFO</td>
<td>First-In First-Out</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>HCS</td>
<td>Header Check Sequence</td>
</tr>
<tr>
<td>I</td>
<td>In-Phase</td>
</tr>
<tr>
<td>ISI</td>
<td>Inter-Symbol Interference</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LOS</td>
<td>Line Of Sight</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>LUT</td>
<td>Look Up Table</td>
</tr>
<tr>
<td>MAC</td>
<td>Medium Access Control</td>
</tr>
<tr>
<td>MCIDS</td>
<td>Multicode Interleaved Direct Sequence</td>
</tr>
<tr>
<td>MPDU</td>
<td>MAC Protocol Data Unit</td>
</tr>
<tr>
<td>MRC</td>
<td>Maximal Ratio Combining</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>NLOS</td>
<td>Non-Line Of Sight</td>
</tr>
<tr>
<td>OPB</td>
<td>On-chip Peripheral Bus</td>
</tr>
<tr>
<td>PAR</td>
<td>Place and Route</td>
</tr>
<tr>
<td>PER</td>
<td>Packet Error Rate</td>
</tr>
<tr>
<td>PHY</td>
<td>Physical Layer</td>
</tr>
<tr>
<td>PRBS</td>
<td>Pseudo-Random Binary Sequence</td>
</tr>
<tr>
<td>PSD</td>
<td>Power Spectral Density</td>
</tr>
<tr>
<td>Q</td>
<td>Quadrature</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>ROM</td>
<td>Read Only Memory</td>
</tr>
<tr>
<td>RTL</td>
<td>Register Transfer Level</td>
</tr>
<tr>
<td>S-V</td>
<td>Saleh-Valenzuela</td>
</tr>
<tr>
<td>SFD</td>
<td>Start Frame Delimiter</td>
</tr>
<tr>
<td>SIFS</td>
<td>Short Inter-Frame Spacing</td>
</tr>
<tr>
<td>TDM</td>
<td>Time Division Multiplex</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra-WideBand</td>
</tr>
</tbody>
</table>
Abstract

An original ultra-wideband (UWB) physical layer (PHY) specification is developed and implemented in digital logic. The novelty of this UWB PHY is based on a combination of complementary code division multiplexing (CCDM), which yields a low-interference signal with a variable process gain, and multicode interleaved direct sequence (MCIDS) spreading, which provides an additional fixed process gain as well as multipath robustness. To operate at the high sample rates needed for UWB, the digital logic, realized in a Virtex-II field programmable gate array (FPGA), has a highly-pipelined architecture for real-time signal processing. In addition, the gate count is minimized by avoiding the use of explicit buffer memory wherever possible. The performance of the transceiver is analyzed under a variety of UWB channels and impairments. It is concluded that the proposed UWB PHY offers robust performance in real-world environments and that it is viable for use in future communication systems.
Acknowledgements

*Cry havoc! And let slip the dogs of war.*

Thanks to my supervisor, my family and my friends.