On the improvement of boost and buck-boost converters for battery applications

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Recommended Citation

ON THE IMPROVEMENT OF BOOST AND BUCK-BOOST CONVERTERS FOR BATTERY APPLICATIONS

A thesis submitted in partial fulfilment of the requirements for the award of the degree

Doctor of Philosophy

from

University of Wollongong

by

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November 2017
This doctoral thesis is dedicated to my family.
Certification

I, NENG ZHANG, declare that this thesis, submitted in partial fulfilment of the requirements for the award of Doctor of Philosophy, in the Institute for Superconducting and Electronic Material, Australian Institute for Innovation Material, University of Wollongong, is wholly my own work unless otherwise referenced or acknowledged. This document has not been submitted for qualifications at any other academic institution.

Neng ZHANG

17th October 2017
Acknowledgements

I would like to extend many thanks to all the people who generously contributed to and supported the work presented in this thesis.

Special thanks go to my principle supervisor Dr. Khay Wai See for his excellent guidance. Also, I am deeply grateful to Distinguished Professor Shi Xue Dou for his impartial co-supervision throughout my doctoral degree. Without their enlightened instruction, impressive kindness and patience, I could not have completed my thesis.

Secondly, I shall extend my thanks to the staff in the School of Electrical, Computer and Telecommunications Engineering (SECTE) and Institute for Superconducting and Electronics Material who have helped me to develop a fundamental and essential academic competence.

Financial supports from China Scholarship Council and University of Wollongong for my Ph.D. scholarship are gratefully acknowledged.

Finally, but by no means least, I wish to express my deepest love and gratitude to my wife, my parents in-law, my parents, and other families for their boundless and almost unbelievable support. They are the most important people in my world and I dedicate this thesis to them.
Publications

Publications in Refereed Journals:


Buck-Boost Converter," Under preparation for submission to *IEEE Transactions on Power Electronics*.

**Publications in Conference Proceedings:**


Declaration of Publications included in this thesis:

As the principle supervisor, I, Khay Wai See, declare that the greater part of the work in each publication listed above is attributed to the candidate, Neng ZHANG. In each of the above publication, the candidate contributed to development of the main idea or concept, which has been extended, refined and tuned for improvement with advice from me and the co-authors. The candidate has prepared the first draft of each of the publication and revised those according to the suggestions provided by the co-authors. The candidate has been responsible for submitting each of the manuscripts for publication to relevant publishers, and he has been in charge of responding to the reviewers’ comments with assistance from his co-authors.

Dr. Khay Wai SEE

Principle supervisor

17th October 2017
Abstract

Battery systems have become essential roles in our daily life from portable devices to renewable energy generation systems. In order to fulfil the requirements in different battery included practical applications, to use batteries more efficiently, and to ensure its long-term safe operation, specific technologies, especially the power electronics technology, are required to regulate the power supplied by batteries. Hence, the research work in this thesis is focused on the improvement and enhancement of the boost and buck-boost converters used in battery applications.

First, a novel high gain quadratic boost converter with a voltage multiplier circuit is proposed to extend the voltage conversion ratio of the traditional boost converter.

Then, in order to solve the input current ripple issue existed in the traditional boost converter, a ∆-Y hybrid impedance network based converter is proposed. The proposed converter can remain the voltage conversion feature of the traditional boost converter while effectively reduce the input current ripple and the average current flowing through the main inductor.

Further, a single-switch quadratic buck-boost converter with non-pulsating input port current and non-pulsating output port current is proposed to improve the performance of the existing buck-boost converters and quadratic buck-boost converters.

Finally, the origin of the dead-zone existed in the non-inverting buck-boost converter operating in two mode (buck mode and boost mode) scheme has been demystified. Based on this, a series of multi-mode modulation schemes are systematically derived to completely eliminate the dead zone to improve the performance including efficiency and output voltage ripple of the converter.

All the proposed converters and modulation methods are theoretically analysed and experimentally validated in this thesis.
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Chapter 1 Introduction

1.1 General Background

Batteries have been widely used in our daily life from low power level daily applications like portable devices as the power source to high power level industrial applications like the renewable energy generation applications as the energy storage system. However, the battery has a nominal output voltage, certain power capability, and a limited cycle life, which is determined by its material chemical characteristic. In order to fulfil the requirements in different practical applications, to use batteries more efficiently, and to ensure its long-term safe operation, specific technologies are required.

There are many ways to regulate the output voltage of a battery system. The simplest way is to connect several battery cells in series to achieve a higher output voltage of the battery system. However, this method is not applicable when the demanded voltage is lower than the output voltage of the single battery cell. Another method is to use a linear voltage regulator to obtain the required voltage. However, this method normally requires the input voltage (the output voltage of the battery) being higher than the output voltage (the desired voltage). Also, the efficiency of the linear voltage regulators is relatively low due to the use of the power consuming variable resistor or the transistor. In order to address these problems, switched power circuits, which is based on the power electronics technology, has been adopted in battery applications to fulfil various practical applications and improve the efficiency of using batteries.

Within the limited cycle life, the lifetime of a battery system mainly depends on the operation condition. The amplitude, fluctuations, micro-cycles, and ripple components of the current flowing through the battery can all place negative impacts on the battery lifetime [1-5]. Also, to ensure safe operation of a battery system, some protection such as overcharge and overdischarge protection should be considered in the design. Therefore, appropriate power electronics converters included battery management systems are normally required in battery applications to control the power conversion
process, to improve the operation conditions, and to enhance the reliability of the overall system.

1.2 Motivation

With the features of voltage boosting capability and continuous input current, the traditional boost converter is preferably used in the battery applications when the demanded voltage is always higher than the output voltage of the battery system.

However, when the demanded voltage is significantly (e.g. 10 times) higher than the output voltage of the battery system, the traditional boost converter will lose its applicability as it could not be used to achieve such a high voltage conversion ratio $V_{out}/V_{in}$, where $V_{out}$ is the output voltage of a converter (the demanded voltage) and $V_{in}$ is the input voltage of a converter (the voltage of the battery system), due to some practical limitations such as an extremely short turn-off time and high voltage stress for the switch and significantly degraded efficiency. Therefore, novel high efficiency converters with high boosting capability are required in this type of battery applications such as the battery bank based energy storage system [6-7], non-interruptible power supply system [8], lighting technology [9-10], and transportation technology [11-13].

Besides, although the input current of the boost converter (the current flowing through the battery) is inherently continuous, the switching frequency current ripple can still negatively affect the operation condition of the battery and cause degradation in the lifetime of the battery [5]. Hence, the input current ripple reduction technologies including advanced control algorithm and novel topologies are required for the boost converters used in battery applications to lengthen the battery lifetime.

In some applications, the battery pack is required to be dynamically reconfigurable to increase its flexibility, reliability, and fault tolerance [14-18]. In this case, the input voltage of a converter (output voltage of the battery pack) tends to vary in a range that is possible to overlap with the output voltage of the converter (demanded voltage). Hence, a converter with both voltage bucking and voltage boosting capability is desired to be applied to interface the battery pack and the load. The traditional buck-boost converter, Cuk converter, Sepic converter, and Zeta converter are candidates to fulfil this voltage
conversion requirement, However, the output polarity of the traditional buck-boost converter and Cuk converter is reversed and the Cuk, Sepic, and Zeta converters apply more than one inductor and an extra capacitor in the middle for power processing which may reduce the efficiency and make the converter bulky. Compared to these converters, the non-inverting buck-boost converter can implement both buck and boost power conversion using only one inductor and output a voltage with the same polarity as the input voltage. Also, voltage stresses of the power switches in this converter are lower than ones of the aforementioned buck-boost converters. With these advantages, the non-inverting buck-boost converter can be a better candidate for such applications. However, there are four active switches included in the converter, which may result in low efficiency operation when all of the four switches are turned ON and OFF in a single switching period. It is therefore critical to control the converter to operate with high efficiency and stable output voltage over the entire input voltage range.

When the input voltage of a converter (output voltage of the battery pack) tends to vary in a sufficiently large range while the output voltage of the converter (demanded voltage) is fixed or the output voltage of a converter varies in a sufficiently large range while the input voltage of the converter is fixed, the converter with a traditional buck-boost voltage conversion ratio will not be applicable. In such applications, novel buck-boost converter with wider voltage conversion ratio range is desired. The converter with a quadratic buck-boost voltage conversion ratio is a good solution for this type of applications. Unfortunately, the input current of the existing quadratic buck-boost converters is normally inherently pulsating, which can result in increased input current ripple that may shorten the lifetime of the battery. Therefore, it is of interest to develop novel quadratic buck-boost converters with non-pulsating input current to fulfil practical requirements in battery applications.

1.3 **Research Objectives and Contributions**

The main objective of this thesis is focused on the improvement and enhancement of the traditional boost and buck-boost converters used in battery applications, which can be classified as follows.

1. *Develop a novel step-up converter with high voltage conversion ratio.*
2. Reduce the input current ripple of the traditional boost converter.

3. Develop a novel quadratic buck-boost converter with non-pulsating input current.

4. Investigate advanced modulation and control methods for the non-inverting buck-boost converter to improve its operating efficiency.

The contributions of this thesis can be summarised as follows.

1. A novel high step-up boost converter based on the integration of the voltage multiplier circuit has been developed.

   The developed converter can provide a much higher output voltage with a low input voltage and reduce the voltage stresses in the power devices. The efficiency and the reliability of the converter can be improved by using semiconductors with low voltage level and high performance.

   2. An impedance network based technology has been derived to reduce the input current ripple of the traditional boost converter.

   With the application of the proposed impedance network, the new obtained boost converter can remain voltage conversion feature of the traditional boost converter while effectively reduce the input current ripple and the average current flow through the main inductor.

   3. A single-switch quadratic buck-boost converter with non-pulsating input port current and non-pulsating output port current has been designed.

   The designed converter can operate with non-pulsating input port current and non-pulsating output port current compared to the existing counterparts with inherently pulsating input port current and pulsating output port current. The comparison between the designed converter and the existing quadratic buck-boost converters has been conducted to demonstrate the unique features of the proposed one.

   4. The origin of the dead-zone existed in the operation process of the non-inverting buck-boost converter operating in buck and boost mode has been derived from a mathematical point of view.
The non-inverting synchronous converter is preferable to operate in buck and boost mode to obtain a high operating efficiency. However, the dead zone, which degrades the performance of the converter, will occur when the converter shifts from buck operating mode to boost operating mode or vice versa. Therefore, the origin of the dead zone is derived by analysing the relationship between the voltage conversion ratio and the duty cycles of the switches.

5. Based on the derivation of the dead zone, a series of multi-mode modulation methods have been derived to completely eliminate the dead zone.

A series of three-mode and four-mode modulation schemes are derived to completely eliminate the dead zone. The ripple and average value of the inductor current under different modulation schemes have been investigated. With the derived modulation methods, the performance and efficiency of the non-inverting buck-boost converter has been significantly improved.

1.4 Thesis Outline

The remainder of this thesis is organised as follows.

In Chapter 2, reviews about the high gain boost converter are conducted first followed by the review of the existing input current ripple elimination methods. Then, the review of quadratic converters especially the quadratic buck-boost converters is provided and the technologies proposed in the literature to improve the performance of the non-inverting buck-boost converter are summarized.

In Chapter 3, a novel high gain quadratic boost converter with a voltage multiplier circuit is proposed for high voltage conversion required battery applications. The theoretical analysis and experimental validation of the proposed converter are presented.

In Chapter 4, a Δ-Y hybrid impedance network based boost converter with reduced input current ripple is proposed. The operating principle of the proposed converter is explained and the mechanism of current ripple reduction is analysed. Experimental results are carried out to validate the effectiveness of the proposed converter.
In Chapter 5, a single-switch quadratic buck-boost converter with non-pulsating input port current and non-pulsating output port current is proposed. The operating principle and steady-state performance of the proposed converter under continuous inductor current mode is analysed in detail. The comparison between the proposed converter and the existing quadratic buck-boost converters has been conducted. Experimental results from a prototype built in the lab are recorded to verify the effectiveness and validity of the proposed quadratic buck-boost converter.

In Chapter 6, the origin of the dead-zone existed in the operation process of the non-inverting buck-boost converter operating in buck and boost mode has been derived by analysing the relationship between the voltage conversion ratio and the duty cycles of the switches. Based on this, a series of three-mode and four-mode modulation schemes are systematically derived to completely eliminate the dead zone. The ripple and average value of the inductor current under different modulation schemes are investigated to evaluate the performance of these modulation schemes. Two implementations of a four-mode modulation scheme are presented and experimentally tested as the examples for all modulation schemes to demonstrate the effectiveness of the proposed modulation schemes.

In Chapter 7, a conclusion of the thesis is drawn and some recommendations for the research in the future are presented.
Chapter 2 Literature Review

2.1 Foreword

This chapter aims to review the related work in the published literatures. First, reviews about high gain boost converters are conducted. Then, the analysis of input current ripple elimination methods are presented followed by the overview of existing quadratic converters. Finally, the technologies to improve the performance of the non-inverting buck-boost converter are summarized.

2.2 Review of High gain step-up converters

In recent years, the research about high gain boost converters has become one of the hottest topics in the field of power electronics, since such converters are increasingly required in many industrial applications, such as fuel cell systems, distributed photovoltaic (PV) generation systems and uninterruptable power supply (UPS) systems [19-24]. In these applications, the voltage conversion ratio, $V_{\text{out}}/V_{\text{in}}$ (where $V_{\text{out}}$ is the output voltage and $V_{\text{in}}$ is the input voltage) is required to be relatively high. However, conventional boost converters could not be used to realize such a high step-up voltage conversion ratio due to some limitations such as an extremely small off-time for the switches, high voltage stresses of the switches, and low efficiency [25-26]. Therefore, high-gain, high-efficiency converters without above limitations are required.

Switched-capacitors can be adopted in basic DC-DC converters to extend the voltage conversion ratio [27-31], and switch-capacitor integrated converters normally have simple structures and high efficiency. But with the increase in the voltage conversion ratio, the structure of these converters will become more complex and the current ripple will increase significantly [32]. A multiplier made up of diodes and capacitors can improve the drawbacks indicated above [33-35]. However, further improvements of the voltage conversion ratios of these converters using these two methods are limited as the voltage gain is controlled only by the duty cycle.
The voltage gain of a converter with coupled inductors [36-42] can be extended by regulating its duty cycle or enlarging the turns’ ratio of the coupled inductor. Unfortunately, most of these converters have a relatively high input current ripple. Inserting a built-in transformer into the converter has been proved to be an effectively approach to relieve this problem [43-45].

![Circuit configuration of the converter](image)

Figure 2-1 (a) Circuit configuration of the converter in [50], (b) Circuit configuration of the converter in [51].

Quadratic converters can also boost the gain of the traditional boost converters [46-49], and they have gained a lot of attention of the power electronic researchers. However, these converters cannot utilize low-voltage-level and high-performance switches due to the high voltage stresses of the switches during the normal operation. Besides, their voltage conversion ratios are limited as they are controlled only by duty cycle. In order to address this problem, studies about quadratic converters with coupled-inductors were conducted in [50] and [51], and the extension of the voltage gain was demonstrated. In [50], the first-stage inductor and the second-stage inductor in a
quadratic converter were coupled, which is shown in Fig. 2-1 (a), and in [51], a coupled-inductor was applied in the second-stage circuit of a cascaded quadratic converter, which is shown in Fig. 2-1 (b).

2.3 Input voltage ripple cancellation techniques for the boost converter

Various impedance networks have been successively developed and studied in the literatures to be adopted in the traditional boost converter (TBC) to enhance its output port characteristic [52], [53], i.e., the voltage conversion ratio, to fulfill different industrial applications such as the distributed generation systems powered by renewable energy sources like wind, solar, and fuel cells [54], [55] and the battery based back-up energy conversion systems [56] over the past decades. However, few attentions have been put into improving its input port characteristic, i.e., the input current ripple, using impedance networks.

Different from the traditional way to deal with the input current ripple issue of the TBC by using a sufficiently large inductor [57] or different types of LC filters in the input port of the converter shown in Fig. 2-2(a), which may lower the dynamic response of the converter and make the converter unnecessarily bulky as well as degrade the efficiency [58]–[60], applying the coupled inductor based impedance network is another solution [61]–[65]. However, most of these techniques are implemented by replacing the TBC’s main inductor with the coupled inductor based impedance network as shown in Fig. 2-2(b), which may not be an economical and convenient solution in practical applications as it needs to break the original structure of the TBC. Recently, another coupled inductor based impedance network method has been proposed in [66] to reduce the input current ripple without the demand to replace the TBC’s main inductor as shown in Fig. 2-2(c). However, two additional capacitors are required in this method and the additional resonant inductor is expected to be relatively large. Also, the impedance network in this method is only used to deal with the input current ripple issue but without help for reducing the average current of the TBC’s main inductor.
Figure 2-2 Illustrations of existing passive input current ripple reduction techniques for the TBC.

Except from the aforementioned passive solutions, active solutions can also be adopted to reduce the input current ripple for the TBC [67] – [69]. The typical and most attractive active solution is to combine several basic converters using an interleaved parallel structure. The input current is then evenly distributed to the inductor in each basic converter and the input current ripple can correspondingly be reduced by controlling basic converters appropriately. Also, the current stress on each basic converter’s inductor has been distributed evenly. However, this approach may lead to the increase of the cost and complexity of the converter as more active and passive components are required. Meanwhile, accurate control algorithms are demanded to achieve zero current ripple, which means that completed current ripple cancellation can
only be achieved under the condition that the duty ratio of each basic converter is $1/N$ and the phase difference of the switching sequence among each basic converter is $360^\circ/N$ in an $N$-phase interleaved topology [15].

In face of the existing background, this thesis is to propose a $\Delta$-Y hybrid impedance network based boost converter to deal with the input current ripple issue for the TBC. The $\Delta$-Y hybrid impedance network is formed by the TBC’s main inductor, an additional coupled inductor, and an additional resonant inductor and capacitor pair. The proposed converter remains the TBC’s original structure and voltage conversion feature while effectively reduce the input current ripple and the average current flow through the main inductor.

### 2.4 Overview of quadratic converters

Renewable energy such as photovoltaic (PV) panels and wind turbines are increasingly being used because of the environmental awareness and advances in technology with decreasing manufacturing cost. Power electronics circuits are usually required to regulate their output voltage and power characteristics to match the load demand. In some industrial applications, such as PV-supplied LED street lighting, the supplying voltage might be varying significantly, while the demanded voltage is required to be relatively constant. The variation in the supplying voltage can be much larger than that in the demanded voltage. Also, some multi-functional power supplies may require a wide range of output voltages while supplied by a power source with a constant voltage. In these cases, a buck-boost DC/DC converter with wide gain is in need. It is well known that the voltage conversion ratio $M (M=V_{\text{out}}/V_{\text{in}}, \text{where } V_{\text{out}} \text{ is the output voltage and } V_{\text{in}} \text{ is the input voltage})$ of the PWM DC-DC converters is a function of the duty cycle of the switch. The quadratic converter, whose voltage conversion ratio has a quadratic relationship in terms of the duty cycle, has the potential for the applications that require a wide input-output voltage conversion [70-72].

A lot of studies about quadratic buck converters [73-80] and quadratic boost converters [81-87] have been developed and reported. Therein, some researchers have studied the mathematical model and control methods for the quadratic buck converters [73-77], while others focused on the soft-switching techniques [78-79]. Also, the
reduction of redundant power processing approach was used to develop new quadratic buck converters [80]. Some novel quadratic boost converter topologies were also proposed and analysed [82-87]. However, very few research works have been carried out on the topology of the quadratic buck-boost converter.

A cascaded quadratic buck-boost converter, which is shown in Fig. 2-3(a) and named as traditional quadratic buck-boost converter in this thesis, has been proposed in [70] and [71]. This converter is formed by cascading two traditional buck-boost converters using a single switch. It is obvious that the input current of this converter is equal to the current of the inductor \( L_1 \) while the output voltage (the current of the diode \( D_3 \)) is zero when the switch is turned ON, the input current is zero while the output current is equal to the current of the inductor \( L_2 \) when the switch is turned OFF. Therefore, the input current and output current of the traditional quadratic buck-boost converter are inherently pulsating, which is possible to result in increased input and output current ripples and complicate the design of the input and output filters. Another transformer-
less quadratic buck-boost converter has been proposed in [88] as shown in Fig. 2-3(b), in which two synchronously operating and floating connected switches are required. Meanwhile, similar as the traditional quadratic buck-boost converter, the input port current and the output port current of this converter are naturally pulsating. Hence, it is of interest to develop novel quadratic buck-boost converters with single switch and non-pulsating input port current and continuous output port current to overcome the shortages of the existing converters.

2.5 Technologies to improve the performance of the Non-inverting buck-boost converter

The non-inverting synchronous buck-boost converter shown in Fig. 2-4 can both boost and buck the input voltage to a non-inverting output voltage. Also, voltage stresses of the power switches in this converter are lower than ones of other basic buck-boost converters, e.g. the inverting buck-boost converter, Cuk converter, Sepic converter and Zeta converter [89-90]. Therefore, the non-inverting synchronous buck-boost converter has been investigated as a suitable candidate for those applications where the input voltage tends to vary in a wide range and overlap with the output voltage, such as power factor correction applications [91-92] and fixed-configuration battery pack or reconfigurable battery pack based power systems [93-94].

![Diagram of Non-Inverting Buck-Boost Converter](image)

Figure 2-4 The configuration of the non-inverting buck-boost converter.

In order to operate with a high power conversion efficiency over the entire input voltage range, this converter is expected to operate in pure buck mode when the input voltage is higher than the output voltage and in pure boost mode when the input voltage is lower than the output voltage [95-102], which is called two-mode operating scheme.
in this thesis. However, the converter will wigwag between the buck mode and the boost mode due to the practical unavoidable limitation of the electronic components when the input voltage is in a small range around the output voltage. Also, the discontinuity of the voltage conversion ratio will happen in this small range, which means that the voltage conversion ratio cannot reach the values around 1, therefore, this small range becomes a dead zone. The existence of the dead-zone will lead to the increase of the output voltage ripple and potential instability of the converter [103-105].

Several solutions have been developed to mitigate the dead-zone issue in the literature [93-108]. The simplest way is to control the converter solely operating in buck-boost mode at the cost of a decreased efficiency [107]. A complicated compensation method is proposed in [94] to avoid the dead zone. However, this method requires precise measurement of the details about the operating performance of the power devices, which is relative difficult to execute in practical applications. A tri-mode two edge modulation method is proposed in [95]. In this modulation method, one duty cycle is clamped at the maximum value when the input voltage reaches the pre-assigned small range around the output voltage while the other duty cycle is controlled to regulate the output voltage. This method results in the fact that the limitation of the two duty cycles differ from each other and the lower limitation of the active duty cycle is required to be zero to completely eliminate the dead zone. However, the duty cycle can never reach zero due to the practical limitation of electronic components. A mix-mode modulation technique is proposed in [96] by inserting two additional buck-boost modes in the dead zone. This modulation method requires the switching frequency in the two additional buck-boost modes to be reduced by a half. A four-mode modulation scheme is proposed in [106]. The smooth mode transition can be obtained in this method by dividing the dead zone into two subzones and accordingly inserting two different buck-boost operating modes. By overlapping the duty cycles of both buck mode and boost mode and setting appropriate limitations of the duty cycles, an improved duty-cycle-overlap control method is proposed in [108]. With this control method, the pulse-skipping phenomenon can be well eliminated and smooth mode transition can be achieved. A comprehensive derivation of the dead zone avoiding methods is conducted in [104] and further improved in [109] based on introducing a new nonlinear state machine into the control loop. The dead zone issue can be effectively released and high power efficiency
can be obtained with these methods. However, this work is based on the complicated theory and it is relative difficult to be applied in practical cost-sensitive fields.

Although many existing researches focus on the dead zone mitigation methods, each method has its specific deriving theory. It is hard to find a general rule or a systematic principle to develop dead zone mitigation methods in the literature. Therefore, it of interest to investigate the relationship between the duty cycles of the active switches and the voltage conversion ratio of the converter from a novel perspective, to demystify the origin of the dead zone, and to develop novel solutions to eliminate the dead zone issue systematically.

2.6 Summary

The reviews in this chapter show that the converter with a quadratic gain is a good way to enhance the voltage conversion ratio. This chapter also shows that novel impedance network is an alternative solution to improve the input current ripple issue for the traditional boost converter. This chapter indicates that a general rule or a systematic principle to develop dead zone mitigation methods for improving the performance of the non-inverting buck-boost converter is necessarily required in practical applications.
Chapter 3 A Novel High-Voltage-Gain Quadratic Boost Converter with Voltage Multiplier

3.1 Foreword

In this chapter, a novel high gain quadratic boost converter with a voltage multiplier circuit is presented to give an alternative power electronic circuit for high voltage conversion required battery applications. The proposed converter combines the traditional quadratic boost converter and a coupled-inductor-based voltage multiplier circuit. Compared with the traditional quadratic boost converter, the proposed converter can obtain a much higher output voltage under the same duty cycle and input voltage, and can also reduce the voltage stresses in the power devices. Moreover, the serious input current ripple issue existing in other coupled-inductor based high gain converters is relieved. Consequently, the efficiency and the reliability can be improved by using semiconductors with low voltage level and high performance. The theoretical analysis of the proposed converter is verified by the experimental results.

3.2 Configuration of the Proposed Converter

A novel high-voltage-gain quadratic boost converter with a voltage multiplier, which combines the advantages of the voltage multiplier circuit and the traditional quadratic converter, is proposed in this chapter. The advantages of the proposed converter are summarised as follows:

1) The converter has low input current ripple and low conduction loss, making it suitable for low to medium power battery applications;

2) The proposed converter achieves a much higher step-up voltage gain comparing with that of a traditional quadratic boost converter;
3) The voltage stresses of the main switch and diodes in the converter are much lower than those experienced in a traditional quadratic boost converter when they have the same output voltage.

The proposed converter is mainly composed of a switch \( S \), two input inductors \( L_1 \) and \( L_2 \), diodes \( D_1, D_2 \) and \( D_3 \), storage capacitor \( C_1 \), output capacitor \( C_5 \), and the voltage multiplier circuit which includes a coupled inductor, three capacitors \( C_2, C_3 \) and \( C_4 \), and two diodes \( D_3, D_4 \), as shown in Fig. 3-1 (a). The coupled inductor can be represented by an ideal transformer with a turns’ ratio \( N = n_2/n_1 \), where \( n_1 \) and \( n_2 \) stands for the number of turns of the primary side (\( L_{31} \)) and the secondary side (\( L_{32} \) respectively), a paralleled magnetic inductor \( L_{3m} \) and a leakage inductor \( L_{3k} \). The simplified equivalent circuit of the proposed converter is shown in Fig. 3-1 (b).

![Configuration of the proposed converter](image1)

(a)

![Simplified equivalent circuit](image2)

(b)

Figure 3-1 (a) Configuration of the proposed converter, (b) Simplified equivalent circuit.

### 3.3 Operation Principle of the Proposed Converter

In order to simplify the analysis of the operation principle, some assumptions are made as follows:
The converter operates with high switching frequency and input inductors \( L_1 \) and \( L_2 \) are assumed to be large enough such that \( i_{L1} \) and \( i_{L2} \) are continuous and the converter works under current continues mode (CCM); all capacitors are adequately large, and the voltage across each capacitor is considered to be constant during a single switching period;

2) All components are ideal except for the leakage inductance of the coupled inductor;

Based on these assumptions, some key waveforms under CCM operation in a single switching period are illustrated in Fig. 3-2 and the corresponding equivalent circuits are shown in Fig. 3-3. The operating modes are described as follows.

Mode 1 \([t_0 - t_1]\): At \( t = t_0 \), the switch \( S \) is conducting, and diodes \( D_1 \) and \( D_4 \) are in turn-on state. Diodes \( D_2 \), \( D_3 \) and \( D_5 \) are reverse-biased by \( V_{c1} \), \( V_{c3} \) and \( V_o - V_{c3} \), respectively. The corresponding equivalent circuit and current paths are shown in Fig. 3-3 (a). The energy stored in the input source \( V_d \) is transferred to the inductor \( L_1 \) through \( D_1 \) and \( S \). Therefore, the current \( i_{L1} \) is increasing linearly. The current \( i_{L2} \) is also increasing linearly as the energy stored in capacitor \( C_1 \) is released to the inductor \( L_2 \) through \( S \). Meanwhile, capacitor \( C_2 \) is releasing its energy to the primary side of the coupled inductor, and capacitor \( C_3 \) is discharging its energy to capacitor \( C_4 \) through \( D_4 \). The load \( R \) is supplied by the capacitor \( C_5 \). This mode ends at \( t = t_1 \), when the switch \( S \) is turn-off. Some of the main equations among the components in this mode are as follows,

\[
L_1 \frac{di_{L1}(t)}{dt} = V_d
\]  \hspace{1cm} (3-1)

\[
L_2 \frac{di_{L2}(t)}{dt} = V_{c1}
\]  \hspace{1cm} (3-2)

\[
L_3 \frac{di_{L3}(t)}{dt} = V_{L3m} - V_{c2}
\]  \hspace{1cm} (3-3)

\[
i_s(t) = i_{L1}(t) + i_{L2}(t) + i_{L3}(t) + \frac{1}{N} i_{L3}(t)
\]  \hspace{1cm} (3-4)

\[
V_{L32} = V_{c4} - V_{c3}
\]  \hspace{1cm} (3-5)
Figure 3-2 Key waveforms of the proposed converter.
Figure 3-3 Operation processes of proposed converter mode: (a) Mode1 \([t_0-t_1]\), (b) Mode2 \([t_1-t_2]\), (c) Mode3 \([t_2-t_3]\), (d) Mode4 \([t_3-t_4]\), (e) Mode5 \([t_4-t_5]\).
Mode 2 \([t_1 - t_2]\): The corresponding equivalent circuit and current paths in this transition interval are shown in Fig. 3-3 (b). Once the switch \(S\) is turned off at \(t_1\), diodes \(D_2, D_3,\) and \(D_4\) are conducting, and diodes \(D_1\) and \(D_5\) are reverse-biased by \(V_{c3} - V_{c1}\) and \(V_o - V_{c3}\), respectively. The energy stored in the inductor \(L_1\) is released to the capacitor \(C_1\) through \(D_2\) and the current \(i_{L1}\) decreases linearly. The energy stored in the inductor \(L_2\) is released to the capacitor \(C_3\) through \(D_3\) and the current \(i_{L2}\) decreases linearly. Since the leakage inductor current \(i_{L3k}\) is greater than zero in this mode, the energy stored in \(L_{3k}\) is discharging to the capacitor \(C_3\) through \(D_3\), and the current \(i_{L3k}\) decreases quickly in a linear way. This mode ends when the current \(i_{L3k}\) reaches zero at \(t = t_2\). Some main relations among the components in this mode are as follows,

\[
L_1 \frac{di_{L1}(t)}{dt} = V_{c1} - V_d \tag{3-6}
\]

\[
L_2 \frac{di_{L2}(t)}{dt} = V_{c2} + V_{L3m} - V_{c1} \tag{3-7}
\]

\[
L_{3k} \frac{di_{L3k}(t)}{dt} = V_{c3} - V_{L3m} - V_{c2} \tag{3-8}
\]

\[
V_{L32} = -V_{c4} \tag{3-9}
\]

Mode 3 \([t_2 - t_3]\): During this transition interval, the switch \(S\) remains in turn-off state and the diodes \(D_2, D_3\) and \(D_5\) are conducting. The corresponding equivalent circuit and current paths are shown in Fig. 3-3 (c). The energy stored in capacitor \(C_4\), inductors \(L_1\) and \(L_2\) as well as the input source \(V_d\) is being delivered to the output capacitor \(C_5\) and load \(R\) through the diode \(D_5\) and to the capacitors \(C_1, C_2,\) and \(C_3\) through diodes \(D_2\) and \(D_3\). Therefore, capacitors \(C_1, C_2, C_3\) and \(C_5\) start to be charged. This mode ends when the current flowing through the diode \(D_3\) reaches zero at \(t = t_3\) and \(D_3\) turns off naturally. Some of the main equations among the components in this mode are as follows,

\[
i_{L2}(t) = i_{c5}(t) + i_{L3k}(t) + \frac{1}{N}i_{L3k}(t) \tag{3-10}
\]

\[
V_{L32} = V_o - V_{c1} - V_{c4} \tag{3-11}
\]

\[
V_{L3m} = V_{c3} - V_{c2} \tag{3-12}
\]
Mode 4 \([t_3 - t_4]\): During this mode, the corresponding equivalent circuit and current paths are shown in Fig. 3-3(d). Only diodes \(D_2\) and \(D_5\) keep conducting, while the other diodes and the switch \(S\) are in turn-off state. The current flowing through the inductor \(L_2\), \(i_{L2}\), is the summation of the leakage inductor current \(i_{L3k}\) and the current flowing through the diode \(D_5\). One of the main equations among the components in this mode is as follows,

\[
i_{L2}(t) = i_{L3k}(t) + \frac{1}{N}i_{L3k}(t)
\]  

(3-13)

Mode 5 \([t_4 - t_5]\): At \(t_4\), the switch \(S\) is turned on and diodes \(D_1\) and \(D_5\) are conducting. The current of the leakage inductance \(L_{3k}\), \(i_{L3k}\), and that of diode \(D_5\) decrease rapidly to zero at \(t_5\), which is the end of this mode. The corresponding equivalent circuit and current paths are shown in Fig. 3-3 (e). Some of the main equations among the components in this mode are as follows,

\[
L_{3k} \frac{di_{L3k}(t)}{dt} = V_{L3m} - V_{C2}
\]  

(3-14)

\[
V_{L32} = V_o - V_{C4}
\]  

(3-15)

### 3.4 Performance Analysis and Discussion of the Proposed Converter

#### 3.4.1 Voltage Gain Expression

To simplify the analysis, only modes 1, 3 and 4 are considered because mode 2 and 5 are transition modes and their time durations are significantly short compared to other modes. It is also reasonable to neglect the leakage inductance of the coupled inductor and assume the voltage ripples on all capacitors are zero. Moreover, the losses of the power devices such as the switch and the diodes are not considered. During mode 1, the related voltage relations can be derived as

\[
\begin{align*}
V_{L1} &= V_o \\
V_{L2} &= V_{C1} \\
V_{L3m} &= V_{C2} \\
V_{C4} &= V_{C3} + NV_{L3m}
\end{align*}
\]  

(3-16)
During mode 3 and mode 4, the related voltage relations can be derived as

\[
\begin{align*}
V_{c1} &= V_{c1} - V_d \\
V_{c2} &= V_{c3} - V_{c1} \\
V_{c3m} &= V_{c3} - V_{c2} \\
V_o &= V_{c4} + V_{c3} + NV_{L3m}
\end{align*}
\]  

(3-17)

Considering the aforementioned voltage relations and using the voltage-second balance principle on the inductors \(L_1\) and \(L_2\), and the magnetic inductor \(L_{3m}\) of the coupled inductor, the following relation can be achieved.

\[
\begin{align*}
V_{c1}D &= (V_{c1} - V_o)(1 - D) \\
V_{c2}D &= (V_{c2} - V_c)(1 - D) \\
V_{c3}D &= (V_{c3} - V_{c2})(1 - D) \\
V_o &= (N + 2)V_{c3}
\end{align*}
\]  

(3-18)

According to (3-18), the voltages of some capacitors can be obtained as

\[
V_{c1} = \frac{1}{1 - D} V_d ,
\]  

(3-19)

\[
V_{c3} = \frac{1}{(1 - D)^2} V_d ,
\]  

(3-20)

\[
V_{c2} = (1 - D)V_{c3} = \frac{1}{1 - D} V_d .
\]  

(3-21)

Substituting (3-20) to (3-18), the voltage conversion ratio of the proposed converter can be derived as

\[
M = \frac{V_o}{V_d} = \frac{N + 2}{(1 - D)^2} .
\]  

(3-22)

According to (3-22), the voltage gain of the proposed converter with different values of \(N\) can be clearly depicted as shown in Fig. 3-4. It can be observed from Fig. 3-4 that the voltage conversion ratio of the proposed converter is much higher than that of a traditional quadratic boost converter, and the voltage gain of the proposed converter can increase dramatically with the increase of the turns’ ratio \(N\) of the coupled inductor.

When taking the voltage drops of diodes into consideration and assuming the voltages of all diodes are equal to \(V_D\), the output voltage and the voltages of the capacitors can be derived as
Figure 3-4 Voltage gain of the proposed converter with different value of $N$

$$V_{C1} = \frac{V_d - V_D}{1-D}, \quad (3-23)$$

$$V_{C2} = \frac{V_d - V_D}{(1-D)^2} - V_D, \quad (3-24)$$

$$V_{C2} = (1-D)V_{C1} = \frac{V_d - V_D}{1-D}, \quad (3-25)$$

$$V_{C4} = \frac{N(V_d - V_D)}{1-D} + \frac{V_d - V_D}{(1-D)^2} - 2V_D, \quad (3-26)$$

$$V_o = \frac{(N+2)(V_d - V_D)}{(1-D)^2} - 3V_D. \quad (3-27)$$

3.4.2 Current Ripples of the Inductors $L_1$ and $L_2$

The current ripples of inductors $L_1$ and $L_2$ can be derived from the aforementioned analysis as follows,

$$\Delta i_{L1} = \frac{V_o D}{L_1 f_s} = \frac{V_o D(1-D)^2}{(N+2)L_1 f_s} \quad (3-28)$$

$$\Delta i_{L2} = \frac{V_o D}{(1-D)L_2 f_s} = \frac{V_o D(1-D)}{(N+2)L_2 f_s} \quad (3-29)$$
In order to ensure the converter operating under CCM, inductances of the inductors is required to be larger than the critical inductances, which can be expressed as shown in (3-30) and (3-31),

\[ L_i > \frac{D(1-D)^4 R}{2(N+2)^2 f_i} \]  

(3-30)

\[ L_i > \frac{D(1-D)^2 R}{2(N+2)f_i} \]  

(3-31)

As for the traditional quadratic boost converter, the current ripples and CCM operating inductances of inductors can be expressed as,

\[ \Delta i_{1s} = \frac{V_i D}{L_i f_i} = \frac{V_i D(1-D)^2}{L_i f_i} \]  

(3-32)

\[ \Delta i_{1s} = \frac{V_i D}{(1-D)L_i f_i} = \frac{V_i D(1-D)}{L_i f_i} \]  

(3-33)

\[ L_i > \frac{D(1-D)^4 R}{2f_i} \]  

(3-34)

\[ L_i > \frac{D(1-D)^2 R}{2f_i} \]  

(3-35)

According to equations (3-28) - (3-35), it can be seen that the proposed converter and the traditional quadratic boost converter will have the same input current ripple when the two converters are supplied by the same input voltage. But when the output voltages of the converters are equal, the input current ripple of the proposed converter will decrease with the increase of the turns’ ratio \( N \) of the coupled inductor. Also, it is obviously that the CCM operating inductances of the inductors for the proposed converter is much smaller than those for the traditional quadratic boost converter.

3.4.3 Power Device Voltage and Current Stresses Analysis

According to the aforementioned descriptions and analysis, the maximum voltage stresses of all the power devices in the proposed converter can be derived as shown in Tab. 3-1. Meanwhile, in order to show the difference between the proposed converter
and the traditional quadratic boost converter, the maximum voltage stresses of all power devices of the traditional quadratic boost converter are also shown in Table 3-1.

Table 3-1 Comparison of the maximum voltage stresses of the power devices between the proposed converter and the traditional quadratic boost converter

<table>
<thead>
<tr>
<th>Power devices</th>
<th>The proposed converter</th>
<th>The traditional quadratic boost converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>( \frac{1}{N+2} V_o )</td>
<td>( V_o )</td>
</tr>
<tr>
<td>( D_1 )</td>
<td>( \frac{1-D}{N+2} V_o )</td>
<td>((1-D)V_o)</td>
</tr>
<tr>
<td>( D_2 )</td>
<td>( \frac{D}{N+2} V_o )</td>
<td>( DV_o )</td>
</tr>
<tr>
<td>( D_3 )</td>
<td>( \frac{1}{N+2} V_o )</td>
<td>-</td>
</tr>
<tr>
<td>( D_4 )</td>
<td>( \frac{N+1}{N+2} V_o )</td>
<td>-</td>
</tr>
<tr>
<td>( D_5 )</td>
<td>( \frac{N+1}{N+2} V_o )</td>
<td>( V_o )</td>
</tr>
</tbody>
</table>

Table 3-2 Expression of Peak value and root-mean-square (rms) value of the currents of the power devices

<table>
<thead>
<tr>
<th>Power devices</th>
<th>Peak value of the proposed converter</th>
<th>Root-mean-square value of the proposed converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>( \frac{2(N+2)}{(1-D)^2} I_o + \frac{D(1-D)^2}{(N+2)L_1f_s} V_o + \frac{(N+1)D(1-D)}{N(N+2)L_{3m}f_s} V_o )</td>
<td>( \frac{3(N+2)}{2(1-D)^2} I_o + \frac{D(1-D)^2}{4(N+2)L_1f_s} V_o + \frac{(N+1)D(1-D)}{2N(N+2)L_{3m}f_s} V_o \sqrt{D} )</td>
</tr>
<tr>
<td>( D_1 )</td>
<td>( \frac{N+2}{(1-D)^2} I_o + \frac{D(1-D)^2}{2(N+2)L_1f_s} V_o )</td>
<td>( \frac{N+2}{(1-D)^2} I_o \sqrt{D} )</td>
</tr>
<tr>
<td>( D_2 )</td>
<td>( \frac{N+2}{(1-D)^2} I_o + \frac{D(1-D)^2}{2(N+2)L_1f_s} V_o )</td>
<td>( \frac{N+2}{(1-D)^2} I_o \sqrt{1-D} )</td>
</tr>
<tr>
<td>( D_3 )</td>
<td>( \frac{N+2}{1-D} I_o + \frac{D(1-D)}{2(N+2)L_1f_s} V_o )</td>
<td>( \frac{N+2}{1-D} I_o \sqrt{1-D} )</td>
</tr>
<tr>
<td>( D_4 )</td>
<td>( \frac{D(1-D)}{N(N+2)L_{3m}f_s} V_o )</td>
<td>( \frac{D(1-D)}{N(N+2)L_{3m}f_s} V_o \sqrt{D/3} )</td>
</tr>
<tr>
<td>( D_5 )</td>
<td>( \frac{N+2}{(N+1)(1-D)} I_o + \frac{D(1-D)}{2(N+1)(N+2)L_2f_s} V_o )</td>
<td>( \frac{N+2}{(N+1)(1-D)} I_o \sqrt{1-D} )</td>
</tr>
</tbody>
</table>
Table 3-1 shows that, taking \( V_o \) as the reference, although the proposed converter has two more diodes than the traditional quadratic boost converter, the voltage stresses across all diodes and the switch \( S \) decrease significantly with increase of the turns’ ratio \( N \) of the coupled inductor. Even the coupled inductor is removed from the proposed converter, the corresponding voltage stresses is just half of that of the traditional quadratic boost converter. So, it is possible to use low-voltage-level and high-performance switch and diodes to improve the overall efficiency of the proposed converter.

The expression of peak value and root-mean-square value of the currents of the power devices can also be derived as shown in Table 3-2, it should be claimed that some approximations were made in the calculation.

### 3.5 Performance Comparison

The voltage gain of the proposed converter, converters in the references [19], [39], [50], [51] and the traditional quadratic boost converter at continuous current mode operation are given in Table 3-3. In order to make clearer comparison, the voltage gain versus the duty cycle of the above converters under \( N=1 \) is plotted in Fig. 3-5.

<table>
<thead>
<tr>
<th>Converters</th>
<th>Voltage Gain</th>
<th>Quantities of switches</th>
<th>Quantities of diodes</th>
<th>Switch voltage stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed converter</td>
<td>( \frac{N+2}{(1-D)^2} )</td>
<td>1</td>
<td>5</td>
<td>( \frac{1}{N+2}V_o )</td>
</tr>
<tr>
<td>Traditional quadratic boost converter</td>
<td>( \frac{1}{(1-D)^2} )</td>
<td>1</td>
<td>3</td>
<td>( V_o )</td>
</tr>
<tr>
<td>Converter in [19]</td>
<td>( \frac{2N+2}{1-D} )</td>
<td>2</td>
<td>4</td>
<td>( \frac{1}{2N+2}V_o )</td>
</tr>
<tr>
<td>Converter in [39]</td>
<td>( \frac{2ND+2}{1-D} )</td>
<td>2</td>
<td>4</td>
<td>( \frac{1}{2}V_o )</td>
</tr>
<tr>
<td>Converter in [50]</td>
<td>( \frac{2}{(1-D)^2} )</td>
<td>1</td>
<td>5</td>
<td>( \frac{1}{2}V_o )</td>
</tr>
<tr>
<td>Converter in [51]</td>
<td>( \frac{ND+1}{(1-D)^2} )</td>
<td>1</td>
<td>4</td>
<td>( \frac{1}{ND+1}V_o )</td>
</tr>
</tbody>
</table>
According to Table 3-3 and Fig. 3-5, it can be observed that once the duty cycle is larger than 0.25, the proposed converter has the highest voltage gain among these converters. Fortunately, the duty cycle is normally larger than 0.5 in boost applications. In addition, the switch voltage stress of the proposed converter is lower than those of the converters in [39], [51] and that of the traditional quadratic boost converter. Although the switch voltage stress of the proposed converter is larger than the converter in [19], the converter in [19] has 2 switches, which may result in the increase of the complexity of the circuit and its related control algorithm and driving method.

3.6 Key Parameters Design

3.6.1 Turns Ratio of the Coupled Inductor

The turns’ ratio of the coupled-inductor is one of the most important parameters for the proposed converter because it relates to the duty cycle, the power devices voltage and current stress, which can be obtained as,

\[ N = \frac{V_o}{V_i} \left(1 - D\right)^2 - 2. \]  (3-36)

From (3-36), it can be seen that once the duty cycle is determined, the turns’ ratio of the coupled-inductor can be calculated.
3.6.2 Selection of Inductors

According to the equations (3-28) and (3-29), one can easily obtain the inductance of inductors $L_1$ and $L_2$, which can be derived as follows,

$$L_1 = \frac{V_o D(1-D)}{(N+2)\Delta t_{i1}f_s}.$$  \hspace{1cm} (3-37)

$$L_2 = \frac{V_o D(1-D)}{(N+2)\Delta t_{i2}f_s}.$$  \hspace{1cm} (3-38)

Once the current ripples, duty cycle, output voltage, turns’ ratio and switching frequency are determined, the theoretical value of the inductances of the inductors can be calculated easily. The inductances of the inductor can be designed larger than the calculated value in practical applications since parasitic parameters can degrade the performance of the converter.

3.6.3 Selection of Power Devices

According to the aforementioned theoretical analysis, once other related parameters are designed, the voltage and current level of the power devices can be obtained and appropriate diodes and switch can be selected.

3.6.4 Selection of Capacitors

The design of capacitors is to control the voltage ripples of the capacitors to an acceptable extent since the voltage ripples may affect the performance of the converter.

In terms of the differential equation of the capacitor, i.e. $C = \frac{I_C dt}{dV_C}$ (where $I_C$, $dt$ and $dV_C$ are the current, voltage rising time interval and voltage ripple of the capacitor, respectively), when the permitted voltage ripple of the capacitor is pre-assigned and the $I_C$, $dt$ are obtained, the theoretical value of capacitance of the capacitor can be obtained. The capacitances can be approximately calculated as follows.

$$C_1 \approx \frac{(N+2)I_C D \sqrt{D}}{(1-D)f_s \Delta V_{c1}}.$$  \hspace{1cm} (3-39)

$$C_2 \approx \frac{D^2(1-D)V_o \sqrt{D/3}}{(N+2)L_{3m} f_s^2 \Delta V_{c2}}.$$  \hspace{1cm} (3-40)
where, \( \Delta v_{c1}, \Delta v_{c2}, \Delta v_{c3}, \Delta v_{c4}, \) and \( \Delta v_{c5} \) are the pre-assigned voltage ripples of the capacitors \( C_1, C_2, C_3, C_4 \) and \( C_5 \), respectively.

It is to be noted that it is appropriate to select larger capacitance than the calculated value in practical applications when the parasitic parameters and random errors between the real value and labelled value of the capacitance of the capacitor, which can degrade the performance of the converter, are taking into account.

### 3.7 Experimental results

In order to demonstrate the validity and effectiveness of the theoretical analysis, a prototype of the proposed converter, which is shown in Fig. 3-6, is built and tested in the laboratory. The specifications of the built prototype are described as follows. The rated input voltage is 11V, the rated output voltage is 120V, the rated output current is 0.6A, the rated power is 72W and the switching frequency is 50 kHz. The main parameters of the utilized components are shown in Table 3-4. For the power devices, diodes of type RHRP3060 are selected for diodes \( D_1 \) and \( D_2 \), diodes of type MUR8100 are selected for diodes \( D_3, D_4 \) and \( D_5 \) and a MOSFET of type IRFP260 is selected for the switch \( S \). The prototype was tested with different resistor loads, \( R=200\Omega \) (rated), and \( R=400 \Omega \). The experimental results under the load condition of \( R=200\Omega \) are shown in Fig. 3-7 and results under the load condition of \( R=400\Omega \) are given in Fig. 3-8.
Figure 3-6 Prototype of the proposed converter

Table 3-4 Parameters of utilized components

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters</th>
<th>Components</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N=n_2:n_1$</td>
<td>13:16</td>
<td>$L_1$</td>
<td>100 $\mu$H</td>
</tr>
<tr>
<td>$L_2$</td>
<td>200 $\mu$H</td>
<td>$L_{3m}$</td>
<td>300 $\mu$H</td>
</tr>
<tr>
<td>$L_{3k}$</td>
<td>3 $\mu$H</td>
<td>$C_1$</td>
<td>220 $\mu$F</td>
</tr>
<tr>
<td>$C_2$</td>
<td>22 $\mu$F</td>
<td>$C_3$</td>
<td>10 $\mu$F</td>
</tr>
<tr>
<td>$C_4$</td>
<td>4.7 $\mu$F</td>
<td>$C_5$</td>
<td>220 $\mu$F</td>
</tr>
</tbody>
</table>

The waveforms of the driving signal, the voltage of capacitor $C_3$, and the current and drain-source voltage of the switch are shown in Fig. 3-7 (a). It can be observed from Fig. 3-7 (a) that the drain-source voltage of the switch is approximately equal to the voltage of the capacitor $C_3$, which is only about 35 percent of the output voltage.

The waveforms of the voltage of capacitor $C_1$, the output voltage, and the currents of inductors $L_1$ and $L_2$ are provided in Fig. 3-7 (b). Fig. 3-7 (b) shows that the output voltage is about 102V and the voltage of the capacitor $C_1$ is about 18 V, which are very near to the theoretical values. The results also show that the currents of the inductors are corresponding well with the theoretical analysis.

Fig. 3-7 (c) shows the current waveforms of the leakage inductance and the diode $D_5$ while Fig. 3-7 (d) gives the current waveforms of the diodes $D_1$ and $D_2$. The results are all in satisfied agreement with the theoretical analysis.
Similarly, Fig. 3-8 provides the recorded experimental results of the built prototype under the load condition of $R=400\Omega$, it can be seen that the results are also in well correspondences with the theoretical analysis.

The efficiency of the converter in terms of the duty cycle, the input voltage, and the turns’ ratio of the coupled inductor can be approximately derived as

$$
\eta = \frac{(V_d - V_D)(N + 2) - 3V_d(1-D)^2}{V_d(N + 2)}.
$$

(3-43)
Given that $V_D = 1.2\text{V}$ and $N = 13:16$, the efficiency versus the duty cycle and the input voltage can be depicted in Fig. 3-9 according to (3-43). It can be found from Fig. 3-9 that the efficiency of the proposed converter will increase with the increase of the input voltage when the converter operating with a constant duty cycle and will also increase with the increase of the duty cycle when supplied by a constant input voltage, which indicates that the converter can operate highly efficiently in those high input voltage and high voltage conversion ratio desired applications. The calculated values and experimental results about the efficiency and the output voltage versus the duty cycle are shown in Fig. 3-10 (a) and Fig. 3-10 (b) respectively. The results demonstrated the theoretical analysis.

![Figure 3-8 Experimental results $R=400\Omega$](image)

(a) (b) (c) (d)

Figure 3-8 Experimental results $R=400\Omega$ (a) from the top to the bottom are waveforms of driving signal, voltage of capacitor $C_3$, current and drain-source voltage of the switch, (b) from the top to the bottom are waveforms of voltage of capacitor $C_3$, output voltage, current of inductor $L_1$ and current of
inductor $L_2$. (c) from the top to the bottom are waveforms of $i_{L3k}$ and current of the diode $D_5$, (d) from the top to the bottom are waveforms of current of $D_1$ and $D_2$

Figure 3-9 Efficiency versus the duty cycle and input voltage under: $V_D=1.2V$, $N=13:16$.

Figure 3-10 The calculated and experimental efficiencies and output voltage versus the duty cycle (a) efficiencies, (b) output voltage.

3.8 Summary

In this chapter, a novel high-voltage-gain quadratic boost converter with voltage multiplier is proposed for industry applications. The proposed converter combines a
traditional quadratic boost converter and a coupled inductor. Compared with other high gain converters, there is only one switch required in the proposed converter, which can contribute to the simplification of the circuit structure and the improvement of the system reliability. Moreover, the voltage stresses of the power devices included in the proposed converter are much lower than the high output voltage, which makes it possible for low-voltage-rated power devices with low conducting resistance to be used to improve the performance of the converter. The experimental results from a laboratory built prototype have demonstrated the validity and effectiveness the proposed converter. The proposed converter is a satisfied candidate for those step-up conversion systems requiring a high voltage conversion ratio.
Chapter 4 A ∆-Y Hybrid Impedance Network Based Boost Converter with Reduced Input Current Ripple

4.1 Foreword

This chapter is to propose a ∆-Y hybrid impedance network based boost converter with reduced input current ripple. Comparing to the existing impedance network based boost converters to enhance the output port characteristic, i.e., voltage conversion ratio, of the traditional boost converter (TBC), the proposed converter applies the impedance network to improve its input port performance, i.e., the input current ripple issue. The proposed ∆-Y hybrid impedance network consists of the TBC’s main inductor, an additional coupled inductor and an additional resonant inductor and capacitor pair. With the application of the ∆-Y hybrid impedance network, the proposed converter can remain TBC’s voltage conversion feature while effectively reduce the input current ripple and the average current of the main inductor. The operating principle of the proposed converter is explained and the mechanism of current ripple reduction is analysed in detail. Experimental results from a prototype are carried out to validate the effectiveness of the proposed converter.

4.2 Configuration of the Proposed Converter

![Figure 4-1 Configuration of the proposed converter.](image-url)
The configuration of the proposed converter is shown in Fig. 4-1, in which the TBC’s original structure is remained consisting of the main inductor $L_{bo}$, diode $D$, switch $S$, output capacitor $C_{out}$, and the load $R$ while the $\Delta$-$Y$ hybrid impedance network is constructed by the main inductor $L_{bo}$, the coupled inductor ($L_1$ is the primary side and $L_2$ is the secondary side), the resonant inductor $L_r$ and capacitor $C_r$. By using Kirchoff’s circuit law, the converter can be equivalently transformed as shown in Fig. 4-2, in which

$$
\begin{align}
L_a &= L_1 + M \\
L_r &= L_2 + M \\
L_c &= L_r - M
\end{align}
$$

(4-1)

where, $L_a$ and $L_b$ represent the equivalent primary side and secondary side of the coupled inductor, respectively, $L_c$ is the equivalent inductor of the series connected inductors $L_r$ and the mutual inductor of the coupled inductor $M$.

![Equivalent circuit of the proposed converter.](image)

**4.3 Operation Principle of the Proposed Converter**

To simplify the analysis of the operation principle, some assumptions are made as follows,

1) All components are assumed to be ideal;

2) All capacitors are large enough that the voltage across each capacitor is considered to be nearly constant in a single switching period;
Similar to the TBC, the proposed converter can theoretically operate in both continuous inductor current mode and discontinuous inductor current mode. However, since the continuous inductor current mode is normally preferred in many industrial applications, the proposed converter will be analysed in continuous inductor current mode in this letter. Based on the above assumptions of the components and equivalent transformation of the converter configuration, the operating process of the converter in a single switching period can be separated into four modes. The equivalent circuits in the four operating modes are shown in Fig. 4-3 and key waveforms of the converter are illustrated in Fig. 4-4. The four operating modes are described as follows,

**Mode 1 \([t_0-t_1]\):** As shown in Fig. 4-3 (a), the switch \(S\) is conducting and the diode \(D\) is reverse-biased by the output voltage. The main inductor \(L_{bo}\) is charged by the input voltage and its current \(i_{L_{bo}}\) increases. The current flowing through the inductor \(L_a (i_{La})\) is decreasing while the current flowing through the inductor \(L_b (i_{Lb})\) is increasing as shown in Fig. 4-4. Since \(i_{La}\) is larger than \(i_{Lb}\), the current flowing through the inductor \(L_c (i_{Lc})\) is positive (from top to bottom) and the capacitor \(C_r\) is storing energy. As the input current
equals to the sum of $i_{Lbo}$ and $i_{La}$ and the decreased amount in $i_{La}$ can balance the increased amount in $i_{Lbo}$, the input current ripple can therefore be reduced as shown in Fig. 4-4. If the decreased amount in $i_{La}$ equals to the increased amount in $i_{Lbo}$, the completed elimination of the input current ripple can be achieved. This mode ends at the time $i_{La} = i_{Lb}$. Some of the main equations during this mode are as follows,

\[
\begin{align*}
L_{bo} \frac{di_{Lbo}}{dt} &= v_{in} \\
L_{a} \frac{di_{La}}{dt} + L_{c} \frac{di_{La}}{dt} &= v_{in} - v_{Cr} \\
L_{b} \frac{di_{Lb}}{dt} - L_{c} \frac{di_{La}}{dt} &= v_{Cr} \\
i_{La} - i_{Lc} &= i_{Lb}
\end{align*}
\]  

(4-2)

where, $v_{in}$ stands for the input voltage, $v_{Cr}$ is the voltage of the capacitor $C_r$.

Figure 4-4 Key waveforms of the proposed converter.
Mode 2 \([t_1-t_2]\): As shown in Fig. 4-3 (b), the switch \(S\) is still conducting and the diode \(D\) is still reverse-biased by the output voltage. The difference between this mode and Mode 1 is that the current flowing through the inductor \(L_c\) becomes negative (from bottom to top) and the capacitor \(C_r\) is releasing energy as \(i_{La}\) becomes smaller than \(i_{Lb}\) in this mode. In this mode, the input current ripple reduction is also implemented by using the decreased amount in \(i_{La}\) to balance the increased amount in \(i_{Lbo}\). This mode lasts till the switch \(S\) is turned OFF. Some of the main equations during this mode are as follows,

\[
\begin{align*}
L_{bo} \frac{di_{Lbo}}{dt} &= v_o \\
L_c \frac{di_{Lc}}{dt} - L_v \frac{di_v}{dt} &= v_o - v_{Cr} \\
L_b \frac{di_{Lb}}{dt} + L_v \frac{di_v}{dt} &= v_{Cr} \\
i_{La} + i_{Lc} &= i_{Lb}
\end{align*}
\]  
(4-3)

Mode 3 \([t_2-t_3]\): As shown in Fig. 4-3 (c), the switch \(S\) is turned OFF and the diode \(D\) is conducting. The main inductor \(L_{bo}\) is releasing energy and its current \(i_{Lbo}\) is decreasing. The current flowing through \(L_a\) \((i_{La})\) is increasing while the current flowing through the inductor \(L_b\) \((i_{Lb})\) is decreasing as shown in Fig. 4-4. Since \(i_{La}\) is smaller than \(i_{Lb}\), the current flowing through the inductor \(L_c\) \((i_{Lc})\) is negative and the capacitor \(C_r\) is releasing energy. In this mode, the increased amount in \(i_{La}\) can balance the decreased amount in \(i_{Lbo}\), the input current ripple can therefore be reduced as shown in Fig. 4-4. If the increased amount in \(i_{La}\) equals to the decreased amount in \(i_{Lbo}\), the completed elimination of the input current ripple can be achieved. This modes ends at the time \(i_{La} = i_{Lb}\). Some of the main equations during this mode are as follows,

\[
\begin{align*}
L_{bo} \frac{di_{Lbo}}{dt} &= v_o \\
L_a \frac{di_{La}}{dt} - L_v \frac{di_v}{dt} &= v_o - v_{Cr} \\
L_b \frac{di_{Lb}}{dt} + L_v \frac{di_v}{dt} &= v_{Cr} - v_o \\
i_{La} + i_{Lc} &= i_{Lb}
\end{align*}
\]  
(4-4)

where, \(v_o\) represents the output voltage.

Mode 4 \([t_3-t_4]\): As shown in Fig. 4-3 (d), the switch \(S\) is still turned OFF and the diode \(D\) is still conducting. The difference between this mode and Mode 3 is that the current flowing through the inductor \(L_c\) becomes positive and the capacitor \(C_r\) is storing energy.
as $i_{La}$ becomes larger than $i_{Lb}$. The input current ripple reduction is implemented by using the increased amount in $i_{La}$ to balance the decreased amount in $i_{Lbo}$ in this mode. This mode lasts till the end of the switching period. Some of the main equations during this mode are as follows,

\[
\begin{align*}
L_{bo} \frac{di_{Lbo}}{dt} &= v_{in} - v_o \\
L_a \frac{di_{Lb}}{dt} + L_c \frac{di_{Lc}}{dt} &= v_{in} - v_{Cr} \\
L_b \frac{di_{Lb}}{dt} - L_c \frac{di_{Lc}}{dt} &= v_{Cr} - v_o \\
i_{La} - i_{Lc} &= i_{Lb}
\end{align*}
\]  

(4-5)

### 4.4 Performance Analysis of the Proposed Converter

#### 4.4.1 Voltage Conversion Ratio Expression

To simplify the analysis, the converter is assumed to be a lossless system and all components are ideal. According to equations (4-2) – (4-5) and applying volt-second balance principle on the inductors, the voltage relationships among the components can be derived as,

\[
\begin{align*}
V_{Cr} &= V_s \\
V_o &= \frac{1}{1-D} V_s
\end{align*}
\]

(4-6)

where, $D$ is the duty cycle of the switch.

From (4-6), it can be found that the voltage conversion ratio of the proposed Δ-Y hybrid impedance network based boost converter is exactly the same as that of the TBC. The voltage stress on the capacitor $C_r$ equals to the input voltage.

#### 4.4.2 Currents of the Inductors

According to (4-2) - (4-5) the current ripples of the inductors, namely, $\Delta i_{Lbo}$, $\Delta i_{Lc}$, $\Delta i_{Lb}$, and $\Delta i_{Lc}$ can be deduced as

\[
\Delta i_{Lbo} = \frac{V_o D}{L_{bo} f_s}
\]

(4-7)
\[
\Delta i_{Ld} = \frac{(V_s L_d - V_o)D}{(L_o L_d + L_o L_i + L_i L_d) f_s},
\]
\[
\Delta i_{Lb} = \frac{(V_s L_b - V_o)D}{(L_o L_b + L_o L_i + L_i L_b) f_s},
\]
\[
\Delta i_{Lc} = \frac{(V_s L_c - V_o)D}{(L_o L_c + L_o L_i + L_i L_c) f_s}.
\]

Equation (4-7) shows that the current ripple of the main inductor \(L_{bo}\) in the proposed converter is the same as that of the TBC.

The average current of the main inductor \(L_{bo}\), namely, \(I_{avg_{Lbo}}\), can be derived as

\[
I_{avg_{Lbo}} = \frac{V_o^2}{V_s R} - I_{avg_{La}}.
\]

It can be found from (4-11) that the average current of the inductor \(L_{bo}\) in the proposed converter is smaller than that of the TBC with the same size main inductor as \(I_{avg_{La}}\) is always greater than zero. Combining (4-11) with equation (4-7), it is further indicated that the peak current flowing through the main inductor \(L_{bo}\) in the proposed converter is smaller than that of the TBC with the same size main inductor as the peak current equals to the sum of the average current and half of the current ripple.

**4.4.3 Power Device Voltage and Current Stresses Analysis**

The voltage stresses of the diode \(D\) and the switch \(S\) in the proposed converter, namely, \(V_D\) and \(V_S\), are equal to the output voltage \(V_o\), which is the same as those in the TBC.

The average current of the diode \(D\) \((I_{avg_{D}})\) and the switch \(S\) \((I_{avg_{S}})\) can be derived as

\[
I_{avg_{D}} = I_{in}(1 - D),
\]
\[
I_{avg_{S}} = I_{in} D,
\]

where, \(I_{in}\) is the average input current.

It can be seen that the average current of the diode and the switch are the same as that of the TBC.
The peak current flowing through the diode $D$ ($I_{\text{peak}_D}$) and the switch $S$ ($I_{\text{peak}_S}$) can be derived as

$$I_{\text{peak}_D} = I_{\text{in}} + \frac{\Delta i_{\text{Lbo}} + \Delta i_{\text{Lb}}}{2}. \quad (4-14)$$

$$I_{\text{peak}_S} = I_{\text{in}} + \frac{\Delta i_{\text{Lbo}} + \Delta i_{\text{Lb}}}{2}. \quad (4-15)$$

Equations (4-14) and (4-15) shows that the peak currents flowing through the diode and the switch are relatively larger than those flowing through the traditional boost converter and the difference depends on the current ripple of the inductor $L_{\text{bo}}$, which is shown in (4-9).

### 4.4.4 Input Current Ripple Analysis

According to Fig. 4-3, the input current can be obtained by using Kirchoff’s circuit law as

$$i_{\text{in}} = i_{\text{Lbo}} + i_{\text{Lb}}. \quad (4-16)$$

Therefore, the input current ripple of the proposed converter can be expressed as

$$\Delta i_{\text{in}} = \Delta i_{\text{Lbo}} + \Delta i_{\text{Lb}}. \quad (4-17)$$

Substituting (4-7) and (4-8) into (4-17), the input current ripple can be rewritten as

$$\Delta i_{\text{in}} = \frac{V_s (L_{\alpha} + L_{\gamma}) - V_s L_{\gamma}}{L_{\alpha} L_{\eta} + L_{\eta} L_{\gamma} + L_{\gamma} L_{\alpha}) f_s} + \frac{V_s D}{L_{\text{bo}} f_s}. \quad (4-18)$$

It is clear that once the first term and the second term on the right side in (4-18) have different varying tendency, i.e., when one is increasing, the other one is decreasing, the input current ripple of the proposed converter can be reduced comparing to the TBC. Further, if the sum of the two terms on the right side in (4-18) equals to zero, which is shown in (4-19), the input current ripple of the proposed converter can be completely eliminated.

$$\frac{V_s (L_{\alpha} + L_{\gamma}) - V_s L_{\gamma}}{L_{\alpha} L_{\eta} + L_{\eta} L_{\gamma} + L_{\gamma} L_{\alpha}) f_s} + \frac{V_s D}{L_{\text{bo}} f_s} = 0. \quad (4-19)$$
Considering equations (4-1) and (4-19), it can be derived that once the inductor $L_r$ in the proposed converter satisfies the condition shown in (4-20), the completed input current ripple cancellation of the boost converter can be achieved.

$$L_r = \frac{LM + M^2 - L_1L_2}{L + L_1 + L_2 + 2M}, \quad (4-20)$$

4.5 Experimental results

For the sake of safety and equipment availability in the lab, a 25W low power prototype has been implemented as shown in Fig. 4-5 and tested to confirm the performance and effectiveness of the proposed converter. For comparison, a TBC with the same specifications and components has also been tested. The main specifications and parameters of the components used in the built prototype are shown in Table 4-1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>TBC</th>
<th>The proposed converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency $f_s$</td>
<td>50 kHz</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Input voltage $V_{in}$</td>
<td>10 V</td>
<td>10 V</td>
</tr>
<tr>
<td>Output voltage $V_o$</td>
<td>20 V</td>
<td>20 V</td>
</tr>
<tr>
<td>Load $R$</td>
<td>15 Ω</td>
<td>15 Ω</td>
</tr>
<tr>
<td>Main inductor $L_{bo}$</td>
<td>93.68 μH</td>
<td>93.68 μH</td>
</tr>
<tr>
<td>Coupled inductor $L_1$</td>
<td>-</td>
<td>19.55 μH</td>
</tr>
<tr>
<td></td>
<td>$L_2$</td>
<td>31.78 μH</td>
</tr>
<tr>
<td></td>
<td>$M$</td>
<td>21.2 μH</td>
</tr>
<tr>
<td>Resonant inductor $L_r$</td>
<td>-</td>
<td>10 μH</td>
</tr>
<tr>
<td>Output capacitor $C_{out}$</td>
<td>470 μF</td>
<td>470 μF</td>
</tr>
<tr>
<td>Resonant capacitor $C_r$</td>
<td>-</td>
<td>22 μF</td>
</tr>
</tbody>
</table>
Figure 4-5 The built prototype with the proposed converter in the blue solid block, the TBC in the red solid block, and the ∆-Y hybrid impedance network in the green dashed block.

Additionally, the lab available MOSFET IRFP260N is used for the switch $S$ and diode DSEP8-06A is used for the diode $D$. The switch $S$ is driven by an IC of type TLP350. A KEITHLEY power supply of type 2231-30-3 is used as the input source in the experimental work. The differential probes of type THDP0200 and the probes of type TPP0250 are used for measuring the voltage information while the current probes of type TCP0030A are used for measuring the current. All the experimental waveforms are recorded by the oscilloscope of type Tektronix MDO3024. The experimental results from the two built prototypes are shown in Figs. 4-6 – 4-8.

Figure 4-6 Output voltage and input current waveforms of (a) the proposed converter, and (b) the TBC.
The output voltages of the two prototypes shown in Fig. 4-6 are both about 19.1 V. Fig. 4-6 (a) also shows that the voltage of the capacitor $C_r$ in the proposed converter is about 10V, which is equal to the input voltage as analysed previously. Fig. 4-6 also shows the input current and its ac components of the proposed converter and the TBC, it can been found that the magnitude of the input current ripple of the proposed converter shown in Fig. 4-6(a) is about 0.39A while that of the TBC shown in Fig. 4-6(b) is about 1A, which indicates a 61% reduction in the input current ripple. It should be claimed that the input current ripple can theoretically be completely cancelled if the selected resonant inductor $L_r$ satisfies the condition given in (4-20).

![Waveforms](image)

Figure 4-7 Waveforms of the voltage and current stresses of the switch S and the diode D in (a) the proposed converter, and (b) the TBC.

The voltage and current stresses of the switch and the diode in the proposed converter and the TBC are shown in Fig. 4-7. It is found that the peak current flow through the switch and the diode in the proposed converter are about 4.3 A, which is higher than those in the traditional boost converter 3.3A. The difference is caused by the current ripple on the secondary side of the coupled inductor $L_{L2}$, which is shown in Fig. 4-8(a) and has been analysed in (4-18).

Fig. 4-8(a) shows the currents flowing through the inductors $L_1$, $L_2$ and the resonant inductor $L_r$ while Fig. 4-8(b) shows the currents flowing through the inductors $L_{bo}$ and $L_1$ in the proposed converter. It can be seen from Fig. 4-8(b) and Fig. 4-6(a) that the sum of the currents flowing through the inductors $L_{bo}$ and $L_1$ is equal to the input current. The experimental results correspond well with the theoretical analysis.
Figure 4-8 Currents flow through the inductors in the proposed converter.

The efficiency of the built TBC at 25W load is around 91.33% while that of the built proposed converter at 25W is around 91.11%, which means that the proposed converter and the traditional boost converter have similar efficiency. Considering that the proposed converter has the same voltage conversion ratio as the TBC, it can be applied as an ideal candidate in those boost converter required practical applications.

4.6 Summary

A Δ-Y hybrid impedance network based boost converter with reduced input current ripple is proposed in this chapter. Compared with the TBC, the input current ripple has been effectively reduced in the proposed converter while the voltage conversion characteristic has been remained. Also, the main inductor’s average current is reduced comparing to the TBC. Comparing to other impedance networks based boost converters with reduced input current ripple, which apply the impedance networks to replace the main inductor in the TBC and break its original structure, the proposed one applies the TBC’s main inductor and an additional coupled inductor and a resonant inductor and capacitor pair to form a novel Δ-Y hybrid impedance network to implement the reduction of the input current ripple. The operation principle and steady-state features have been analysed and a prototype has been built and tested in the lab to confirm the features and validity of the proposed converter.
Chapter 5 A Single-Switch Quadratic Buck-Boost Converter with Non-pulsating Input Port Current and Non-pulsating Output Port Current

5.1 Foreword

This chapter is to propose a novel single-switch quadratic buck-boost converter with non-pulsating input port current and non-pulsating output port current. Compared with the traditional buck-boost converter, the proposed converter can obtain a wider range of the voltage conversion ratio with the same duty cycle range. Moreover, the proposed converter can operate with non-pulsating input port current and non-pulsating output port current compared to the existing counterparts with inherently pulsating input port current and pulsating output port current. The operating principle and steady-state performance of the proposed converter under continuous inductor current mode is analysed in detail. Then, the comparison between the proposed converter and the existing quadratic buck-boost converters has been conducted to demonstrate the unique features of the proposed one. Finally, experimental results from a prototype built in the lab are recorded to verify the effectiveness and validity of the proposed quadratic buck-boost converter.

5.2 Configuration of the Proposed Converter

The configuration of the proposed converter is shown in Fig. 5-1. Therein, a boost converter, a buck-boost converter, and a buck converter are combined to share only one switch, which can result in a relatively simple structure. The boost converter consists of input source $V_g$, diodes $D_1$ and $D_2$, inductor $L_1$, capacitor $C_1$, and switch $S$. The buck-boost converter consists of capacitors $C_1$ and $C_2$, inductor $L_2$, diode $D_3$, and switch $S$. The buck converter consists of capacitors $C_2$ and $C_3$, diodes $D_4$ and $D_5$, inductor $L_3$, switch $S$, and load $R$. It can be seen that the output capacitor of the boost converter is the input source of the buck-boost converter while the output of the buck-boost converter is
the input source of the buck converter. It is of interest to note that there is an inductor connected in the input port and an inductor connected in the output port of the converter, which can contribute to the unique feature of drawing non-pulsating input port current and non-pulsating output port current.

![Figure 5-1 Configuration of the proposed converter.](image)

5.3 **Operation Principle of the Proposed Converter**

To simplify the analysis of the operation principle of the proposed converter, some assumptions are made as follows,

1) All components are assumed to be ideal components;

2) All capacitors are large enough that the voltage across each capacitor is considered to be nearly constant in a single switching period.

Similar to other buck-boost converters, the proposed converter can theoretically operate in both continuous inductor current mode and discontinuous inductor current mode. However, since the continuous inductor current mode is normally preferred in many industrial applications to reduce the current ripple and operating with continuous input and output current is a main benefit of the proposed converter, it will be analysed in continuous inductor current mode in this chapter.

Based on the above assumptions, the converter will have two operating modes, i.e., mode 1 (S is turned ON) and mode 2 (S is turned OFF), in a single switching period. The equivalent circuits in the two operating modes are shown in Fig. 5-2(a) and Fig. 5-2(b). Some key waveforms of the proposed converter in a single switching period are illustrated in Fig. 5-3 to illustrate the operating process.
The two operating modes are described as follows,

**Mode 1 \([t_0-t_1]\):** As shown in Fig. 5-2(a) and Fig. 5-3, the switch \(S\) is conducting, diodes \(D_2\) and \(D_4\) are in ON state, and diodes \(D_1\), \(D_3\), and \(D_5\) are reverse-biased by \(v_{C1}\), \(v_{C1} + v_{C2}\), and \(v_{C2}\), respectively. The input source \(V_g\) delivers power to the inductor \(L_1\) through the diode \(D_1\) and the switch \(S\), meantime, the energy stored in capacitors \(C_1\) and \(C_2\) is being delivered to inductors \(L_2\) and \(L_3\), respectively. Therefore, the currents flowing through inductors \(L_1\), \(L_2\), and \(L_3\), i.e., \(i_{L1}\), \(i_{L2}\), and \(i_{L3}\) are increasing. Some of the main equations among the components in this mode can be expressed as

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= v_g, \\
L_2 \frac{di_{L2}}{dt} &= v_{C1}, \\
L_3 \frac{di_{L3}}{dt} &= v_{C2} - v_o, \\
C_1 \frac{dv_{C1}}{dt} &= i_{L2}, \\
C_2 \frac{dv_{C2}}{dt} &= i_{L3}, \\
C_3 \frac{dv_o}{dt} &= i_{L3} - \frac{v_o}{R}.
\end{align*}
\]  

(5-1)

where, \(v_{C1}\) represents the voltage of the capacitor \(C_1\), \(v_{C2}\) is the voltage of the capacitor \(C_2\), while \(v_o\) is the output voltage.
Mode 2 [$t_1$-$t_2$]: At $t_1$, the mode of the proposed converter changes to Mode 2 from Mode 1, which is shown in Fig. 5-2(b). The switch $S$ is turned OFF, diodes $D_1$, $D_3$, and $D_5$ are in ON state, and diodes $D_2$ and $D_4$ are reverse-biased by $v_{C2}$ and $v_{C1}$, respectively. The energy stored in the inductor $L_1$ as well as the input source is delivered to the capacitor $C_1$, and the capacitor $C_1$ starts to store energy. The inductor $L_2$ discharges energy to the capacitor $C_2$ through the diode $D_3$. At the same time, the inductor $L_3$ discharges energy to the capacitor $C_3$ and load $R$. Therefore, $i_{L1}$, $i_{L2}$, and $i_{L3}$ are
decreasing as shown in Fig. 5-3. Some of the main equations among the components in this mode can be expressed as

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= v_t - v_{c1}, \\
L_2 \frac{di_{L2}}{dt} &= -v_{c2}, \\
L_3 \frac{di_{L3}}{dt} &= -v_o, \\
C_1 \frac{dv_{C1}}{dt} &= -i_{L1}, \\
C_2 \frac{dv_{C2}}{dt} &= -i_{L2}, \\
C_3 \frac{dv_{C3}}{dt} &= i_{L3} - \frac{v_o}{R}.
\end{align*}
\]  
(5-2)

5.4 Steady-State Performance Analysis and Discussion of the Proposed Converter

5.4.1 Voltage Conversion Ratio Expression

To simplify the analysis, the converter is assumed to be a lossless system and the relationship of \( V_i I_o = V_o I_i \) is held, where \( I_i \) and \( I_o \) are the input current and the output current, respectively. It is also assumed that the voltage ripples on all capacitors are zero. Moreover, the losses of the power devices are not considered.

Using volt-second balance principle on the inductors and ampere-second balance principle on the capacitors, the following equations can be obtained.

\[
\begin{align*}
V_g - V_{c1}(1 - D) &= 0, \\
V_{c1}D - V_{c2}(1 - D) &= 0, \\
V_{c2}D - V_i &= 0, \\
I_{L2}D - I_{L1}(1 - D) &= 0, \\
I_{L3}D - I_{L2}(1 - D) &= 0, \\
I_{L3} - \frac{V_o}{R} &= 0.
\end{align*}
\]  
(5-3)

From (5-3), the ideal output voltage and the voltages of the capacitors can be derived in terms of the input voltage \( V_g \) and the duty cycle \( D \) of the switch as

\[
\begin{align*}
V_{c1} &= \frac{1}{1-D}V_g, \\
V_{c2} &= \frac{D}{(1-D)^2}V_g, \\
V_o &= \frac{D}{(1-D)^3}V_g.
\end{align*}
\]  
(5-4)

According to (5-4), the ideal voltage conversion ratio \( M \) of the proposed converter can be obtained as
According to (5-5) and the expression of the ideal voltage conversion ratio of the traditional buck-boost converter, the relationship between the ideal voltage conversion ratio and the duty cycle of the proposed converter as well as the traditional buck-boost converter are plotted in Fig. 5-4. Fig. 5-4 shows that the proposed converter can obtain a wider voltage conversion ratio range than the traditional buck-boost converter.

5.4.2 Currents of the Inductors

The current ripples of the inductors, namely, $\Delta i_{L1}$, $\Delta i_{L2}$, and $\Delta i_{L3}$ can be deduced as,

$$\begin{align*}
\Delta i_{L1} &= \frac{V_o D}{L_1 f_s} = (1-D)^2 V_o \\
\Delta i_{L2} &= \frac{V_o D}{L_2 f_s} = (1-D)V_o \\
\Delta i_{L3} &= \frac{(V_{c1} - V_o) D}{L_3 f_s} = (1-D)V_o
\end{align*}$$

(5-6)

From (5-3), the average currents of the inductors $L_1$, $L_2$, and $L_3$, namely, $I_{L1\_avg}$, $I_{L2\_avg}$, and $I_{L3\_avg}$, can be calculated as follows,
\[
\begin{align*}
I_{L_1,avg} &= \left( \frac{D}{1-D} \right)^2 I_o \\
I_{L_2,avg} &= \frac{D}{1-D} I_o \\
I_{L_3,avg} &= I_o
\end{align*}
\] (5-7)

By manipulating Equations (5-6) and (5-7), it can be derived that the inductances of the inductors must satisfy the following conditions to ensure that all the inductors operate in continuous current mode.

\[
\begin{align*}
L_1 &> \frac{(1-D)^2 R}{2D f_s} \\
L_2 &> \frac{(1-D)^3 R}{2D^2 f_s} \\
L_3 &> \frac{(1-D) R}{2f_s}
\end{align*}
\] (5-8)

where, \( R \) is the load.

### 5.4.3 Power Device Voltage and Current Stresses Analysis

According to the aforementioned analysis, the maximum voltage stresses and average currents of the switch \( S \) and all diodes can be derived as follows.

The voltage stresses of diodes \( D_1 \) and \( D_4 \), namely, \( V_{D1} \) and \( V_{D4} \), are equal to the voltage of the capacitor \( C_1 \), which can be expressed as

\[
V_{D1} = V_{D4} = V_{c1} = \frac{1-D}{D^2} V_o.
\] (5-9)

Similarly, the voltage stresses of diodes \( D_2, D_3, D_5 \), and the switch \( S \), namely, \( V_{D2}, V_{D3}, V_{DS} \), and \( V_{DS} \), can be expressed as

\[
\begin{align*}
V_{D2} = V_{D5} = V_{c2} &= \frac{1}{D} V_o \\
V_{D3} = V_{DS} = V_{c1} + V_{c2} &= \frac{1}{D^2} V_o
\end{align*}
\] (5-10)

Further, the average currents of the switch and diodes can be derived as
\[
\begin{align*}
I_{s_{\text{avg}}} &= \frac{D^3 - D^2 + D}{(1-D)^2} I_o, \quad I_{d_{3_{\text{avg}}}} = D I_o, \\
I_{d_{1_{\text{avg}}}} &= \frac{D^2}{1-D} I_o, \quad I_{d_{4_{\text{avg}}}} = D I_o, \\
I_{d_{2_{\text{avg}}}} &= \frac{D^1}{(1-D)^2} I_o, \quad I_{d_{5_{\text{avg}}}} = (1-D) I_o.
\end{align*}
\] (5-11)

5.4.4 Analysis of the Parasitic Parameters’ Impact

Considering the parasitic resistors of the inductors and power devices and the voltage drops of the power devices, the equivalent circuit of the converter can be drawn as shown in Fig. 5-5. In this figure, \(r_{L1}, r_{L2}\) and \(r_{L3}\) are parasitic resistances of inductors \(L_1, L_2\) and \(L_3\), respectively. \(r_{D1}, r_{D2}, r_{D3}, r_{D4}\) and \(r_{DS}\) stand for the parasitic resistors of the diodes and \(r_{DS}\) is the parasitic resistor of the switch. The voltage drops of the diodes and switch are represented by \(V_{dr1}, V_{dr2}, V_{dr3}, V_{dr4}, V_{dr5}\), and \(V_{drs}\), respectively.

![Equivalent circuit of the converter considering parasitic parameters.](image)

According to the operating principle of the converter and applying volt-second balance principle on the inductors, the voltage relationships of \(V_{C1}, V_{C2}, V_o\) in terms of \(V_g\) and the parasitic parameters can be derived as

\[
V_{c1} = \frac{V_s - \frac{D^3}{(1-D)^2} \frac{V_o}{R} r_{L3} - \frac{D^3}{1-D} \frac{V_o}{R} r_{D1} - \frac{D^1}{(1-D)^2} \frac{V_o}{R} r_{D2} - (D^3 - D^2 + D) \frac{V_o}{R} r_{DS} - V_{o5} D - V_{o2} D - V_{o1} (1-D)}{(1-D)}.
\] (5-12)

\[
V_{c2} = \frac{V_{c1} D(1-D)^2 - D(1-D) \frac{V_s}{R} r_{L2} - D(1-D) \frac{V_o}{R} r_{D3} - (D^3 - D^2 + D) \frac{V_o}{R} r_{DS} - V_{o5} D(1-D)^2 - V_{o3} (1-D)^3}{(1-D)^3}.
\] (5-13)
\[ V_o = V_{c2}D - \frac{V_o}{R} r_{L3} - \frac{D}{R} r_{D4} - (1-D) \frac{V_o}{R} r_{D3} - \frac{D^3 - D^2 + D V_o}{(1-D)^2} r_{DS} - V_{d4}D - V_{d5}D(1-D) . \]

(5-14)

Based on (5-12) – (5-14), the expression of the output voltage considering parasitic parameters can be obtained as,

\[ V_o = \frac{D^3(1-D)^3 V_o}{M_3} - V_{drop} , \quad (5-15) \]

where,

\[ V_{drop} = V_{d1}D^2(1-D)^3 - V_{d2}D^3(1-D)^2 - V_{d3}D(1-D) - V_{d4}D(1-D)^4 - V_{d5}(1-D)^5 - V_{d6}D(1-D)^2(D^2 - D + 1) \]

\[ M_3 = M_2(1-D) + D^4 \frac{r_{L3}}{R} + D^4(1-D) \frac{r_{D4}}{R} + D^5 \frac{r_{D3}}{R} + (D^3 - D^2 - D^2) \frac{r_{DS}}{R} \]

\[ M_2 = M_4(1-D) + D^2(1-D) \frac{r_{L3}}{R} + D^2(1-D)^2 \frac{r_{D4}}{R} + (D^4 - D^3 + D^2) \frac{r_{DS}}{R} \]

\[ M_1 = (1-D)^2 + (1-D)^2 \frac{r_{L3}}{R} + (1-D)^2 \frac{r_{D4}}{R} + (1-D)^3 \frac{r_{D3}}{R} + (D^4 - D^3 + D^3) \frac{r_{DS}}{R} \]

Comparing equations (5-4) and (5-15), the output voltage deviation ratio, which is the percentage of the difference between the ideal output voltage and the output voltage considering parasitic parameters to the ideal output voltage, can be obtained as,

\[ \sigma = \frac{M_3D^2V_o - D^3(1-D)^3V_o + (1-D)^2V_{drop}}{M_3D^2V_o} . \]

(5-16)

If the load \( R \) is large enough comparing to the parasitic resistors of the components, the terms including \( \frac{r_{Lx}}{R} (x=1, 2, 3) \), \( \frac{r_{Dy}}{R} (y=1, 2, 3, 4, 5, S) \) in \( M_1 \), \( M_2 \), and \( M_3 \) will be approaching zero. In this case, \( M_3 \) can be simplified as,

\[ M_3 = (1-D)^4 . \]

(5-17)

Substituting (5-17) into (5-15) and (5-16) and assuming the voltage drops of the diodes and the switch are equal to \( V_{drop} \) for simplification, the expression of the output voltage and the deviation ratio can be obtained as,
\[
V_o = \frac{D^2}{(1-D)^2} V_g - \frac{1+2D^2-D^2}{(1-D)^2} V_{drop}.
\]

(5-18)

\[
\sigma = \frac{1+2D^2-D^2}{D^2 V_g} V_{drop}.
\]

(5-19)

It can be found from (5-19) that the output voltage deviation ratio is directly related to the input voltage and the duty cycle. Through doing partial derivative calculation of \(\sigma\) with respect to the duty cycle \(D\) and the input voltage \(V_g\), respectively, the relationships shown in equation (5-20) can be obtained.

![Figure 5-6](image)

Figure 5-6 Relationships between the output voltage deviation ratio and, (a) the duty cycle at different input voltages, (b) the input voltage under different duty cycle conditions.
The relationship among the output voltage deviation ratio, the duty cycle, and the input voltage can be further depicted in Fig. 5-6 by assuming that the parasitic parameters are constant as \( V_{\text{drop}} = 0.7 \text{V} \) during the operating process. From (5-20) and Fig. 5-6, it is found that the deviation ratio of the output voltage decreases significantly with the increase of the input voltage and the duty cycle. It should be claimed that the deviation ratio will become even smaller with the application of high performance devices with better parasitic parameters.

The joule effect losses of the inductors \( P_L \) can be approximately calculated as

\[
P_{L,\text{con}} = \frac{r_{D1} D^4 P_o}{(1-D)^3 R} + \frac{r_{D2} D^5 P_o}{(1-D)^2 R} + \frac{r_{D3} P_o}{R}.
\]  

(5-21)

where, \( D \) is the duty cycle and \( P_o \) is the output power.

The conduction losses of the diodes and the switch, namely, \( P_{DS,\text{C}} \), can be approximately calculated as,

\[
P_{DS,\text{C}} \approx \frac{r_{D1} D^5 P_o}{(1-D)^4 R} + \frac{r_{D2} D^4 P_o}{(1-D)^3 R} + \frac{r_{D3} D^5 P_o}{(1-D)^2 R} + \frac{r_{D4} P_o}{R} + \frac{r_{D5} (D^3 - D^2 + D) P_o}{(1-D)^2 R}.
\]

(5-22)

The losses of the diodes and the switch caused by the forward voltage drops, namely, \( P_{DS,\text{dr}} \), can be approximately calculated as,

\[
P_{DS,\text{dr}} \approx \frac{V_{D1} D^5 P_o}{(1-D) V_o} + \frac{V_{D2} D^4 P_o}{(1-D) V_o} + \frac{V_{D3} D^5 P_o}{(1-D) V_o} + \frac{V_{D4} P_o}{V_o} + \frac{V_{D5} (D^3 - D^2 + D) P_o}{(1-D) V_o}.
\]

(5-23)

The switching loss of the switch, namely, \( P_{S,S} \), can be calculated as,

\[
P_{S,S} \approx \frac{1}{2} \frac{D^3 - D^2 + D}{D^2 (1-D)^2} P_{\text{off}} f_s.
\]

(5-24)
where, \( t_{\text{off}} \) is the turning-off time of the switch.

Thus, the relatively accurate estimation of the efficiency \( \eta \) for the proposed converter can be obtained by using the equation (5-25).

\[
\eta = \frac{P_o}{P_o + P_L + P_{\text{con},c} + P_{\text{con},d} + P_{\text{s.s}}}. \tag{5-25}
\]

For quick estimation and roughly investigating the varying characteristics of the efficiency, it is assumed that the load \( R \) is large enough comparing to the parasitic resistors of the components and the turning-off time of the switch is short enough comparing to the switching period of the converter, then the expression of the efficiency can be simplified as shown in (5-26) by ignoring the joule effects losses of the inductors, the conduction losses of the diodes and the switch, and the switching loss of the switch. The voltage drops of the diodes and the switch are assumed to be \( V_{\text{drop}} \).

\[
\eta = \frac{V_s D^2 - V_{\text{drop}} (1 + 2D^3 - D^2)}{V_s D^2}. \tag{5-26}
\]

The relationship of the efficiency in regard to the input voltage and the duty cycle can be further illustrated in Fig. 5-7. It can be seen from (5-26) and Fig. 5-7 that the operating efficiency of the proposed converter is generally acceptable. Also, the higher
operating efficiency can be obtained in the applications with higher input voltage. Additionally, the converter can operate more efficiently in step-up mode than in step-down mode as the efficiency of the converter will be increasing with the increase of the duty cycle.

5.5 Performance Comparison

5.5.1 Comparison of Input Port and Output Port Currents

Performances

Comparing the proposed converter with the traditional quadratic buck-boost converter and the converter proposed in [88], the voltage transformation ratios of these three converters are exactly the same. However, the input port current and output port current of them, namely, $i_{in}$ and $i_{out}$, are different.

During the switch turned-ON mode, the input port current and output port current of the traditional quadratic buck-boost converter and the converter proposed in [88] can be both expressed as,

$$i_{in} = i_{L1}, i_{out} = 0.$$  \hspace{1cm} (5-27)

While those of the proposed converter can be expressed as,

$$i_{in} = i_{L1}, i_{out} = i_{L3}.$$  \hspace{1cm} (5-28)

During the switch turned-OFF mode, the input port current and output port current of the traditional quadratic buck-boost converter can be both expressed as,

$$i_{in} = 0, i_{out} = i_{L2}.$$  \hspace{1cm} (5-29)

While those of the proposed converter can be expressed as,

$$i_{in} = i_{L1}, i_{out} = i_{L3}.$$  \hspace{1cm} (5-30)

Equations (5-27) – (5-30) can be clearly illustrated in Fig. 5-8, which shows that both the input port current and output port current of the traditional quadratic buck-boost converter have a step change during the mode transition, which means that the current is
discontinuous. The input port and output port currents of the proposed converter are always equal to the current of inductor $L_1$ and $L_3$, respectively, which indicates that the current is continuous.

![Diagram of current flow](image)

**Figure 5-8** $i_{in}$ and $i_{out}$ of the proposed converter and the traditional quadratic buck-boost converter.

Assuming the three converters operate under the same condition with the same average input port current ($I_{in\_avg}$) and output port current ($I_{out\_avg}$), the root-mean-square values of the input port current ($I_{in\_rms}$) and the output port current ($I_{out\_rms}$) of the traditional quadratic buck-boost converter and the converter proposed in [88] can be derived as

$$I_{in\_rms} = I_{in\_avg} \sqrt{1-D}, I_{out\_rms} = I_{out\_avg} \sqrt{1-D}.$$ (5-31)

While those of the proposed converter are

$$I_{in\_rms} = I_{in\_avg}, I_{out\_rms} = I_{out\_avg}.$$ (5-32)

Equations (5-31) and (5-32) show that the RMS values of both input port current and output port current of the proposed buck-boost converter are much smaller than those of the traditional quadratic buck-boost converter and the converter proposed in [88]. The difference can be clearly illustrated in Fig. 5-9, which shows $I_{in\_avg}/I_{in\_rms}$ and $I_{out\_avg}/I_{out\_rms}$ versus the duty cycle of these three converters.
5.5.2 Comparison of Other Features

The comparison of several other key features including the number of components, voltage stresses of the switch and diodes, the type of input port current and output port current of the proposed converter versus other converters including the traditional quadratic buck-boost converter and the converter proposed in [88] are summarized in Table 5-1, in which all the expressions are derived by assuming that the components are ideal and the converters operate in continuous inductor current mode. From Table 5-1, it can be found that the converter has two more diodes than the traditional quadratic buck-boost converter, which may slightly increase the cost of the converter. However, the proposed converter has much wider operating range than the traditional one. This is because that when the duty cycle is larger than 0.5, the voltage stress of the diode D1 in the traditional quadratic buck-boost converter will become negative, which will result in malfunction of the converter. This fact will limit the traditional quadratic buck-boost converter only working in buck mode. Compared to the converter in [88], the proposed converter requires three more diodes. However, the proposed converter only applies one switch while the converter in [88] requires two switches. Considering the related cost of the extra switch and its control and driving circuits, the increased cost by the three more diodes of the proposed converter compared to the converter proposed in [88] might be
balanced. Although the proposed converter requires one more inductor and one more capacitor than the traditional quadratic buck-boost converter and the converter proposed in [88], the proposed converter has continuous input port current and continuous output port current while those of the other two counterparts are discontinuous, which may result in the demand for extra inductors and capacitors as input and output filters to satisfy the EMI/EMC issues in practical applications. Therefore, the cost of the proposed converter is generally acceptable comparing to the traditional one and the one proposed in [88].

Table 5-1 Comparison between the Proposed Converter and the Existing Converters

<table>
<thead>
<tr>
<th>Topology</th>
<th>Traditional quadratic buck-boost converter</th>
<th>Converter proposed in [88]</th>
<th>Proposed converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of components</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductors</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Capacitors</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Diodes</td>
<td>3</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Switches</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Voltage conversion ratio</td>
<td>$\left(\frac{D}{1-D}\right)^2$</td>
<td>$\left(\frac{D}{1-D}\right)^2$</td>
<td>$\left(\frac{D}{1-D}\right)^2$</td>
</tr>
<tr>
<td>Voltage stress of the switch</td>
<td>$\frac{1-D}{D^2}V_o$</td>
<td>$\frac{1-D}{D^2}V_o$</td>
<td>$\frac{1}{D^2}V_o$</td>
</tr>
<tr>
<td>Voltage stresses of the diodes</td>
<td>$D_1 \frac{1-2D}{D^2}V_o$</td>
<td>$D_1 \frac{1-D}{D^2}V_o$</td>
<td>$D_1 \frac{1-D}{D^2}V_o$</td>
</tr>
<tr>
<td></td>
<td>$D_2 \frac{1-D}{D^2}V_o$</td>
<td>$D_2 \frac{1}{D}V_o$</td>
<td>$D_3 \frac{1-D}{D^2}V_o$</td>
</tr>
<tr>
<td></td>
<td>$D_3 \frac{1}{D}V_o$</td>
<td></td>
<td>$D_4 \frac{1-D}{D^2}V_o$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$D_5 \frac{1}{D}V_o$</td>
</tr>
<tr>
<td>Input port current type</td>
<td>Discontinuous</td>
<td>Discontinuous</td>
<td>Continuous</td>
</tr>
<tr>
<td>Output port current type</td>
<td>Discontinuous</td>
<td>Discontinuous</td>
<td>Continuous</td>
</tr>
</tbody>
</table>
5.6  Key Parameters Design

5.6.1 Parameters Design of Inductors

In practical applications, the current ripple is always pre-assigned. Therefore, the inductance of the inductors $L_1$, $L_2$, and $L_3$ can be obtained as

$$
\begin{align*}
L_1 &= \frac{(1-D)^2V_s}{D\Delta I_{L1}f}, \\
L_2 &= \frac{(1-D)V_s}{DM_{L2}f}, \\
L_3 &= \frac{(1-D)\Delta V_s}{\Delta L_{L3}f_s}.
\end{align*}
$$

(5-33)

At the same time, the inductances should satisfy the equations in (5-8) if the converter is designed to operate in continuous inductor current mode.

5.6.2 Parameters Design of Capacitors

The capacitors are designed to control the voltage ripples of the capacitors, which can affect the stability of the converter, to an acceptable extent. The voltage ripples of the capacitors of the proposed converter, namely, $\Delta V_{C1}$, $\Delta V_{C2}$, and $\Delta V_{C3}$ can be deduced as

$$
\begin{align*}
\Delta V_{C1} &= \frac{D^3I_s}{(1-D)C_1 f}, \\
\Delta V_{C2} &= \frac{D I_s}{C_2 f}, \\
\Delta V_{C3} &= \frac{V_s(1-D)}{8L_3 C_3 f_s^2}.
\end{align*}
$$

(5-34)

Similar to the parameter design of inductors, the voltage ripple is usually pre-assigned in practical applications. Therefore, the capacitance of the capacitors can be designed as

$$
\begin{align*}
C_1 &= \frac{D^3I_s}{(1-D)\Delta V_{C1} f_s}, \\
C_2 &= \frac{D I_s}{\Delta V_{C2} f_s}, \\
C_3 &= \frac{V_s(1-D)}{8L_3 \Delta V_{C3} f_s^2}.
\end{align*}
$$

(5-35)

5.6.3 Selection of Power Devices

The selection of the switch and diodes is to determine the rated voltage and current stresses of them. According to the aforementioned analysis, the corresponding
parameters of the power devices can be easily determined and appropriate devices can be selected.

5.7 Experimental results

For the sake of safety and equipment availability in the lab, a prototype supplied by a low input voltage has been implemented and tested to confirm the effectiveness and validity of the proposed converter. Some main specifications of the built prototype are listed as follows.

\[ C_1 = 47 \mu F, \quad C_2 = 47 \mu F, \quad C_3 = 220 \mu F, \quad L_1 = 100 \mu H, \quad L_2 = 400 \mu H, \quad L_3 = 3 mH, \]

\[ f_s = 40 \text{ kHz}, \quad V_{in} = 20 V, \quad R = 3-70 \Omega. \]

Additionally, the lab available MOSFET IRFP260N is used for the switch \( S \) and DSEP8-06As are used for the diodes \( D_1 – D_8 \). The switch \( S \) is driven by the IC of type TLP350. The detailed driving circuit can be referred to [88] as the function of the ICs TLP350 and TLP250 are similar to each other. A KEITHLEY power supply of type 2231-30-3 is used as the input source in the experimental work. The differential probes of type THDP0200 and the probes of type TPP0250 are used for measuring the voltage information while the current probes of type TCP0030A are used for measuring the current. All the experimental waveforms are recorded by the oscilloscope of type Tektronix MDO3024.

The experimental results of the converter operating in step-up mode with the duty cycle of 0.6 and a pure resistive load of 60 \( \Omega \) are shown in Fig. 5-10. Fig. 5-10(a) shows that the output voltage is about 38.77 V, which is close to the calculated results. Fig. 5-10 (b) shows that the voltages of the capacitors \( C_1 \) and \( C_2 \) are generally constant, about 45.87 V and 68.55 V, respectively. The drain-source voltage of the switch is about 112 V, which is approximately equal to the sum of the voltages of the capacitors \( C_1 \) and \( C_2 \). The current waveform of the inductor \( L_1 \) presented in Fig. 10(a) and the current waveform of the inductor \( L_3 \) presented in Fig. 5-10(b) are noted to be continuous, which indicates the earlier theoretical analysis that the proposed converter has continuous input port current and output port current. The current waveforms presented in Fig. 5-10(a) and Fig. 5-10 (b) show that the current flowing through the switch is
approximately equal to the sum of the three inductors’ current when the switch is turned ON. Hence, the experimental results correspond well with the theoretical analysis. Similarly, Fig. 5-11 shows the experimental results obtained in step-down mode of the converter with a duty cycle of 0.4 and a pure resistive load of 6 Ω. The experimental waveforms are also corresponding well with the theoretical analysis. The features of the proposed quadratic buck-boost converter are therefore verified.

![Waveform Diagram](image)

(a)

![Waveform Diagram](image)

(b)

Figure 5-10 Experimental results with D=0.6 and R=60Ω, (a) voltage waveforms of output voltage and drain-source voltage of the switch S, current waveforms of the inductor L₁ and the switch S, (b) voltage waveforms of the capacitors C₁ and C₂, current waveforms of the inductors L₂ and L₃.

In order to study the dynamic performance of the proposed converter, the built prototype was tested with step changes in the load and the results are shown in Fig. 5-12. Fig. 5-12(a) shows the converter response in step-up mode with the load changing from 60Ω to 45Ω at point A. The output voltage is almost stable under this load variation and the slight change is caused by the parasitic parameters of the components.
Fig. 5-12 (b) provides the waveforms in step-down mode with load changing from 6Ω to 4Ω at point B. The results indicate that the dynamic characteristic of the converter is satisfied even in open-loop condition. The close-loop controller can be designed based on the transfer function of the converter, which can be easily derived by using the small-signal modelling method. The designing method of the controller proposed for other quadratic converters [73-77] can also be referred for designing the controller for the proposed converter.

Figure 5-11 Experimental results with D=0.4 and R=6Ω, (a) voltage waveforms of output voltage and drain-source voltage of switch S, current waveforms of the inductor L₁ and the switch S, (b) voltage waveforms of the capacitors C₁ and C₂, current waveforms of the inductors L₂ and L₃.
Figure 5-12 Dynamic performance of the proposed converter in (a) step-up mode with the load changing from 60Ω to 45Ω, (b) step down mode with the load changing from 6Ω to 4Ω.

The measured results of efficiency and output voltage from the built prototype under different operating conditions as well as the theoretically estimated values are shown in Fig. 5-13. Comparing to the theoretically estimated values, the measured results are generally acceptable. The efficiency increases with the increase of the duty cycle and the increase of the input voltage, which demonstrates the analysis in Section 5.4.4. Since the maximum input voltage applied in the test is only 30V, which is relatively low, and the parasitic parameters of the diodes and MOSFET used in the prototype is comparatively large, which contribute to lots of power losses compared to the output power, the efficiency of the built prototype is not high enough. However, it is expectable that the efficiency of the converter can be effectively improved if the converter is applied in high input voltage applications and built with better graded devices as analysed previously.
5.8 Summary

A novel single-switch quadratic buck-boost converter with non-pulsating input port current and non-pulsating output port current is proposed in this chapter. The proposed converter is constructed by combining one traditional boost converter, one traditional buck-boost converter, and one traditional buck converter using only one switch. The proposed converter has an inductor connected in the input port as well as an inductor connected in the output port, which is capable of making the input port current and output port current to be non-pulsating and contributes to the simplification of the design of input and output filters. The operation principle of the proposed converter operating in continuous inductor current mode is analysed. This chapter also analyses the steady state performance of the circuit and the design of key parameters of the components. Experimental results from a prototype built in the lab are obtained to verify the effectiveness and the validity of the converter. This converter can be a good complement for the existing quadratic buck-boost converters and an appropriate candidate for industrial applications such as battery integrated PV system and battery powered multi-function power supply.
Chapter 6 Systematic Derivation of Dead-Zone Elimination Strategies for the Non-Inverting Buck-Boost Converter

6.1 Foreword

The non-inverting buck-boost converter is preferable to operate in pure buck mode or pure boost mode to obtain a high operating efficiency. However, the dead zone, which degrades the performance of the converter, will occur when the converter shifts from buck operating mode to boost operating mode or vice versa. Therefore, the origin of the dead zone is demystified in this chapter by analysing the relationship between the voltage conversion ratio and the duty cycles of the switches. Based on this, a series of three-mode and four-mode modulation schemes are systematically derived to completely eliminate the dead zone. The ripple and average value of the inductor current under different modulation schemes are investigated to evaluate the performance of these modulation schemes. To demonstrate the effectiveness of the proposed modulation schemes, two implementations of a four-mode modulation scheme are presented and experimentally tested as the examples for all modulation schemes. Experimental results correspond well with the theoretical analysis in both implementations over the entire input voltage range.

6.2 Origin of the Dead Zone

6.2.1 Relationship between the Input and the Output Voltage

The configuration of the non-inverting buck-boost converter is shown in Fig. 6-1. In terms of the voltage-second balance principle of the inductor, the relationship between the input voltage and output voltage of the converter can be derived as,

\[ V_o = \frac{d_1}{1-d_2} V_{in}. \]  

(6-1)
where, \( V_o \) is the output voltage, \( V_{in} \) is the input voltage, \( d_1 \) and \( d_2 \) are the duty cycles of the two active switches \( S_1 \) and \( S_2 \). It should be claimed that in order to simplify the analysis, all components are considered to be ideal components.

![Figure 6-1 The configuration of the non-inverting buck-boost converter.](image)

From (6-1), the voltage conversion ratio of the converter \( M \) can be obtained as,

\[
M = \frac{d_1}{1-d_2}.
\]  

(6-2)

![Figure 6-2 One-mode modulation scheme.](image)

Equations (6-1) and (6-2) show that there are two freedoms, i.e. \( d_1 \) and \( d_2 \), can be used to regulate the voltage conversion ratio simultaneously or independently, which implies that there is a series of combination patterns of \( d_1 \) and \( d_2 \) can be applied to achieve the desired output voltage from the supplying input voltage. The equation (6-2) can be further clearly expressed as shown in Fig. 6-2, in which the vertical axis represents \( d_1 \), the horizontal axis represents \( 1-d_2 \), and the slope of the line \( OP \), which connects the origin \( O \) and the operating point \( P \), represents the voltage conversion ratio.
According to the location of the operating point $P$, different modulation schemes can be obtained, which are to be explained in detail in following sections.

### 6.2.2 One-Mode Modulation

Theoretically, the operating point $P$ can be located at anywhere in the rectangle $ABCO$ including the boundaries and the inner area. When the trajectory of the operating point $P$ is located on the diagonal line of the rectangle, which is line $AC$ as shown in Fig. 6-2, it can be seen that slope of the line $OP$ can vary from zero to infinite. In this case, the voltage conversion ratio is continuous over the entire input voltage range and both duty cycles have a value in the range $[0, 1]$, which means that both of the two active switches $S_1$ and $S_2$ are turned-ON/OFF in a single switching period. As the converter only operates in buck-boost mode under this modulation scheme, it is called one-mode modulation in this chapter. This modulation method has been investigated experiencing low power conversion efficiency in the literature. Also, this modulation method will generate high inductor current ripple as well as high inductor current average value. Therefore, this modulation method is not expected in practical applications.

![Figure 6-3 Two-mode modulation scheme.](image)

### 6.2.3 Two-Mode Modulation

When the trajectory of the operating point $P$ is located only on the boundaries $AB$ and $CB$ of the rectangle as shown in Fig. 6-3, i.e. either $d_1$ or $1-d_2$ is kept at 1, only one active switch is turned-ON/OFF in a single switching period. When the slope of the line $OP$ is smaller than 1, which indicates that the input voltage is higher than the output voltage, $1-d_2$ is kept at 1 while $d_1$ is controlled to regulate the output voltage and the
converter operates in buck mode; When the slope of the line \( OP \) is greater than 1, which indicates that the input voltage is lower than the output voltage, \( d_1 \) is kept at 1 while \( d_2 \) is controlled to regulate the output voltage and the converter operates in boost mode. Therefore, this modulation scheme is called two-mode modulation in this chapter. The two-mode modulation method is preferable in practical applications as it contributes to relative higher efficiency and generates smaller inductor current ripple and inductor current average value compared to the one-mode modulation scheme.

![Dead zone diagram](image)

**Figure 6-4 Dead zone.**

### 6.2.4 Origin of the Dead-Zone in Two-Mode Modulation

Although the two-mode modulation can obtain high efficiency and better inductor current performance, there is an unneglectable drawback hidden in this modulation method. Due to the practical unavoidable non-idealities, switching noise and other unpredictable disturbance of electronic components and the circuit layout, the duty cycle always has an upper limitation \( d_{\text{max}} \) and a lower limitation \( d_{\text{min}} \), therefore, \( d_1 \) and \( 1-d_2 \) can only achieve the values in the range \( EF \) and \( GH \) as shown in Fig. 6-4, which indicates that the voltage conversion ratio can only reach the values in the ranges \([M_{\text{min}}, M_{{\text{mid}1}}]\) and \([M_{{\text{mid}2}}, M_{\text{max}}]\) while the values in the ranges \([0, M_{\text{min}}]\), \([M_{\text{max}}, \infty]\), and \([M_{{\text{mid}1}}, M_{{\text{mid}2}}]\) are not achievable. The values in the ranges \([0, M_{\text{min}}]\) and \([M_{\text{max}}, \infty]\) are ignorable and can be avoided easily by designing the specification of the converter whereas the values in the range \([M_{{\text{mid}1}}, M_{{\text{mid}2}}]\) are essential for the converter as they need to be reached by the voltage conversion ratio when the input voltage approaches
the output voltage. Therefore, the range \([M_{\text{mid}1}, M_{\text{mid}2}]\) is defined as dead zone as shown in the shadowed area in Fig. 6-4.

It can be seen that there are no trajectories for the operating point \(P\) when the converter operates in the dead zone. This fact results in the performance that the operating point \(P\) tends to jump between the point \(F\) and point \(B\) when the converter operates in boost mode and between the point \(H\) and point \(B\) when the converter operates in buck mode, which indicates that the voltage conversion ratio \(M\) jumps from \(M_{\text{mid}1}\) to 1 or vice versa when the input voltage is higher than the output voltage and from 1 to \(M_{\text{mid}2}\) or vice versa when the input voltage is lower than the output voltage. This phenomenon leads to the discontinuity of the voltage conversion ratio \(M\) and brings some negative effects on the performance of the converter such as the increase of the output voltage ripple, the appearance of subharmonics in the output voltage, and even the unstable and uncontrollable operation of the converter.

### 6.3 Multi-Mode Modulation Methods

In order to eliminate the dead zone, extra trajectories are demanded for the operating point \(P\), which means that other operating modes are required to be inserted into the two-mode modulation scheme. Hence, multi-mode modulation schemes are required to be studied to implement the smooth mode transition between the buck mode and the boost mode. Basically, multi-mode modulation methods can be categorized into two types: three-mode modulation methods and four-mode modulation methods, which are to be analysed in detail in the following sub-sections.

#### 6.3.1 Three-mode Modulation

By inserting a straight line as the trajectory for the operating point \(P\) in the dead zone, three-mode modulation methods can be derived. Since the additional trajectory line can be adopted in different approaches, several three-mode modulation methods can be obtained. This section will describe three typical three-mode modulation schemes as examples.

1) Regulating both \(d_1\) and \(d_2\) in the dead zone
The first choice to add the additional straight trajectory for the operating point $P$ is to apply an oblique line $DI$, which is a part of the diagonal $AC$ as shown in Fig. 6-5. When the input voltage approaches the output voltage, the converter will operate in the buck-boost mode. In this case, both of the two active switches $S_1$ and $S_2$ are turned-ON/OFF in a single switching period. In this modulation method, the converter operates in buck mode when the input voltage is sufficiently higher than the output voltage, which implies that the voltage conversion ratio is in the range $[M_{\text{min}}, M_{\text{mid}}]$; in boost mode when the input voltage is sufficiently lower than the input voltage, which implies that the voltage conversion ratio is in the range $[M_{\text{mid}}, M_{\text{max}}]$; and in buck-boost mode when the input voltage is close to the output voltage, which implies that the voltage conversion ratio is in the range $[M_{\text{mid}}, M_{\text{mid}}]$. 

The relationship between the duty cycles $d_1$ and $d_2$ when the voltage conversion ratio is in the range $[M_{\text{mid}}, M_{\text{mid}}]$ under this modulation scheme can be expressed as,

$$d_1 = d_2.$$  \hspace{1cm} \text{(6-3)}

\textbf{II) Clamping $d_2$ and regulating $d_1$ in the dead zone}

The other choice to insert the straight additional trajectory for the operating point $P$ is to apply a vertical line $DI$ as shown in Fig. 6-6. When the input voltage approaches the output voltage, the duty cycle $d_2$ is clamped at a constant value $d_{2\text{fix}}$, which is slightly higher than the minimum value $d_{2\text{min}}$, while the duty cycle $d_1$ is controlled to regulate the output voltage. As this operating mode is similar to the buck mode, in which the
duty cycle $d_2$ is clamped at zero while the duty cycle $d_1$ is regulated to obtain the desired output voltage, it is defined as extend-buck mode in this chapter. In this modulation scheme, when the duty cycle $d_1$ reaches its maximum value in buck operating mode or the duty cycle $d_2$ reaches its minimum value in boost operating mode, the converter shifts to the extend-buck operating mode, the dead zone is therefore avoided.

The relationship between the duty cycles $d_1$ and $d_2$ when the voltage conversion ratio is in the range $[M_{\text{mid1}}, M_{\text{mid2}}]$ under this modulation scheme can be expressed as,

$$
\begin{align*}
  d_2 &= d_{2,\text{fix}} \\
  d_1 &= \frac{v_o}{v_i}(1-d_{2,\text{fix}}) \\
  d_{2,\text{fix}} &= 1-d_{1,\text{max}}(1-d_{2,\text{max}})
\end{align*}
$$

(6-4)

![Diagram](image)

Figure 6-6 Three-mode modulation scheme II.

III) Clamping $d_1$ and regulating $d_2$ in the dead zone

Another choice to add the additional straight trajectory is to apply a horizontal line $DI$ as shown in Fig. 6-7. When the input voltage is close to the output voltage, the duty cycle $d_1$ is clamped at a constant value $d_{1,\text{fix}}$, which is slightly lower than the maximum value $d_{1,\text{max}}$, while the duty cycle $d_2$ is controlled to regulate the output voltage. As this operating mode is similar to the boost mode, in which the duty cycle $d_1$ is clamped at one while the duty cycle $d_2$ is regulated to obtain the desired output voltage, it is defined as extend-boost mode in this paper. In this modulation scheme, when the duty cycle $d_1$ reaches its maximum value in buck operating mode or the duty cycle $d_2$ reaches its
minimum value in boost operating mode, the converter shifts to the extend-boost mode, the dead zone is hence eliminated.

![Figure 6-7 Three-mode modulation scheme III.](image)

The relationship of the duty cycles $d_1$ and $d_2$ when the voltage conversion ratio falls in $[M_{\text{mid1}}, M_{\text{mid2}}]$ under this modulation scheme can be expressed as,

$$
\begin{align*}
    d_1 &= d_{1\text{fix}} \\
    d_2 &= 1 - \frac{v_{\text{in}}}{v_o} d_{1\text{fix}} \\
    d_{1\text{fix}} &= d_{1\text{max}}(1 - d_{2\text{min}})
\end{align*}
$$

(6-5)

6.3.2 Four-Mode Modulation

By applying a polyline as the trajectory for the operating point $P$ in the dead zone, four-mode modulation schemes can be deduced. As the additional polyline trajectory can be adopted in different approaches, different four-mode modulation methods can be obtained. Two typical four-mode modulation methods are to be analysed as examples in this section.

1) Clamping $d_1$ at its maximum value and Clamping $d_2$ at its minimum value

Through inserting a convex polyline $DJI$ as the additional trajectory for the operating point $P$ as shown in Fig. 6-8, a four-mode modulation method can be obtained. Similar as three-mode modulation schemes, when the input voltage is sufficiently higher or lower than the input voltage, the converter operates in the buck and the boost mode respectively. When the input voltage is close to the output voltage, the converter will
operate in two different modes, which are the extend-buck mode and the extend-boost mode represented by the trajectories $IJ$ and $DJ$ respectively. When the input voltage is slightly higher than the output voltage, which means that the voltage conversion ratio is in the range $[M_{\text{mid}1}, 1]$, the operating point $P$ will move on the vertical trajectory line $IJ$ and the converter operates in extend-buck mode. In this operating mode, the duty cycle $d_2$ is clamped at its minimum value $d_{2\text{min}}$ while the duty cycle $d_1$ is controlled to regulate the output voltage. When the input voltage is slightly lower than the output voltage, which means that the voltage conversion ratio is in the range $[1, M_{\text{mid}2}]$, the operating point $P$ will move on the horizontal trajectory line $DJ$ and the converter operates in extend-boost mode. In this operating mode, the duty cycle $d_1$ is clamped at its maximum value $d_{1\text{max}}$ while the duty cycle $d_2$ is controlled to regulate the output voltage. Through inserting the extend-buck mode and the extend-boost operating mode, the elimination of the dead zone can be implemented.

The relationship between the duty cycles $d_1$ and $d_2$ when the voltage conversion ratio is in the range $[M_{\text{mid}1}, M_{\text{mid}2}]$ under this modulation scheme can be expressed as,

\[
\begin{cases}
    d_1 = \frac{v_o}{v_i}(1-d_{2\text{min}}), & d_2 = d_{2\text{min}} \\ 
    d_1 = d_{1\text{max}}, & d_2 = 1 - \frac{v_i}{v_o}d_{1\text{max}} \\
\end{cases} \quad M \in [M_{\text{mid}1}, 1] 
\]

(6-6)

**II) Clamping $d_1$ at a fixed value that is lower than its maximum value and Clamping $d_2$ at a fixed value that is higher than its minimum value**
By inserting a concave polyline $DJI$ as the additional trajectory for the operating point $P$ as shown in Fig. 6-9, another four-mode modulation method can be derived. When the input voltage is sufficiently higher or lower than the output voltage, the converter has the same operating principle as the previous described four-mode modulation method; while when the input voltage is close to the output voltage, the converter has different operating processes. When the input voltage is slightly higher than the output voltage, which means that the voltage conversion ratio is in the range $[M_{\text{mid}1}, 1]$, the operating point $P$ will move on the horizontal trajectory line $IJ$ and the converter operates in extend-boost mode. In this operating mode, the duty cycle $d_1$ is clamped at a constant value $d_{1\text{fix}}$, which is slightly smaller than its maximum value $d_{1\text{max}}$, and the duty cycle $d_2$ is controlled to regulate the output voltage. When the input voltage is slightly lower than the output voltage, which means that the voltage conversion ratio is in the range $[1, M_{\text{mid}2}]$, the operating point $P$ will move on the vertical trajectory line $DJ$ and the converter operates in extend-buck mode. In this operating mode, the duty cycle $d_2$ is clamped at a constant value $d_{2\text{fix}}$, which is slightly higher than its minimum value $d_{2\text{min}}$, and the duty cycle $d_1$ is controlled to regulate the output voltage. Therefore, when the voltage conversion ratio is located in the range $[M_{\text{mid}1}, M_{\text{mid}2}]$, extend-buck and extend-boost modes can be applied to implement the elimination of the dead zone and smooth transition between the buck mode and boost mode.

![Diagram of four-mode modulation scheme II.](image)

The relationship between the duty cycles $d_1$ and $d_2$ when the voltage conversion ratio is in the range $[M_{\text{mid}1}, M_{\text{mid}2}]$ under this modulation scheme can be expressed as,
\[
\begin{align*}
d_1 &= d_{1_{\text{fix}}}, d_2 = 1 - \frac{V_o}{V_{\text{in}}} d_{1_{\text{fix}}} & M \in [M_{\text{mid}1}, 1] \\
d_{1_{\text{fix}}} &= d_{\text{im}} (1 - d_{2_{\text{min}}}) \\
d_1 &= \frac{V_o}{V_{\text{in}}} (1 - d_{2_{\text{fix}}}), d_2 = d_{2_{\text{fix}}} & M \in [1, M_{\text{mid2}}] \\
d_{2_{\text{fix}}} &= 1 - d_{\text{im}} (1 - d_{2_{\text{min}}})
\end{align*}
\]

(6-7)

6.4 Study of the Inductor Current Performance under Different Modulation Schemes

It is known that the amount of the power loss determines the efficiency of the converter. For the non-inverting synchronous buck-boost converter, the core loss of the inductor and the conduction loss contribute to most of the total power losses [110]. It is investigated that the inductor core loss is related to the inductor current ripple [110] while the conduction loss is related to the inductor current root-mean-square value, which is similar to the average value when the current ripple is small [100]. Therefore, this section is to study the inductor current ripple and average value of the converter under the proposed different modulation schemes.

When the converter operates under one-mode modulation scheme, the inductor current ripple \( I_{\text{rip,1mode}} \) and the average value \( I_{\text{avg,1mode}} \) can be expressed as shown in (6-8) and (6-9) respectively over the entire input voltage range.

\[
I_{\text{rip,1mode}} = \frac{V_{\text{in}} V_o}{L f_s (V_o + V_{\text{in}})},
\]

(6-8)

\[
I_{\text{avg,1mode}} = \frac{V_o + V_{\text{in}}}{V_{\text{in}}} I_o.
\]

(6-9)

where, \( V_{\text{in}} \) is the input voltage, \( V_o \) is the output voltage, \( L \) is the inductance of the inductor, \( f_s \) is the switching frequency, and \( I_o \) is the output current.

When the converter operates under the two-mode modulation scheme, the inductor current ripple \( I_{\text{rip,2mode}} \) and the average value \( I_{\text{avg,2mode}} \) can be expressed as
\[
I_{\text{rip}, 2\text{mode}} = \begin{cases} 
\frac{V_i(V_o - V_i)}{L_f V_o} & V_i \leq V_o \\
\frac{V_i(V_o - V_i)}{L_f V_i} & V_i > V_o 
\end{cases}
\]

(6-10)

\[
I_{\text{avg}, 2\text{mode}} = \begin{cases} 
\frac{V_i}{I_o} & V_i \leq V_o \\
I_o & V_i > V_o 
\end{cases}
\]

(6-11)

When the converter operates under the three-mode modulation scheme I, the inductor current ripple \(I_{\text{rip}, 3\text{mode}1}\) and the average value \(I_{\text{avg}, 3\text{mode}1}\) can be expressed as

\[
I_{\text{rip}, 3\text{mode}1} = \begin{cases} 
\frac{V_i(V_o - V_i)}{L_f V_o} & V_i \leq V_{f,i1} \\
\frac{V_i(V_o - V_i)}{L_f (V_i + V_o)} & V_{f,i1} < V_i \leq V_{f,i2} \\
\frac{V_i(V_o - V_i)}{L_f V_i} & V_i > V_{f,i2} 
\end{cases}
\]

(6-12)

\[
I_{\text{avg}, 3\text{mode}1} = \begin{cases} 
\frac{V_i}{I_o} & V_i \leq V_{f,i1} \\
\frac{V_i + V_o}{V_i} I_o & V_{f,i1} < V_i \leq V_{f,i2} \\
I_o & V_i > V_{f,i2} 
\end{cases}
\]

(6-13)

where, \(V_{f,i1} = V_o / M_{\text{med2}}\) and \(V_{f,i2} = V_o / M_{\text{med1}}\).

When the converter operates under the three-mode modulation scheme II, the inductor current ripple \(I_{\text{rip}, 3\text{mode}2}\) and the average value \(I_{\text{avg}, 3\text{mode}2}\) can be expressed as

\[
I_{\text{rip}, 3\text{mode}2} = \begin{cases} 
\frac{V_i(V_o - V_i)}{L_f V_o} & V_i \leq V_{f,i1} \\
\frac{V_o d_{f,i2}}{V_o} & V_{f,i1} < V_i \leq V_o \\
\frac{V_i(V_o - V_i(1 - d_{f,i2}))}{L_f V_i} & V_o < V_i \leq V_{f,i2} \\
\frac{V_i(V_o - V_i)}{L_f V_i} & V_i > V_{f,i2} 
\end{cases}
\]

(6-14)
When the converter operates under the three-mode modulation scheme III, the inductor current ripple \( I_{\text{rip,3modeIII}} \) and the average value \( I_{\text{avg,3modeIII}} \) can be expressed as

\[
I_{\text{avg,3modeIII}} = \begin{cases} 
\frac{V_o}{V_{in}} I_o & V_{in} \leq V_{f1d} \\
\frac{1}{1-d_{2,fix}} I_o & V_{f1d} < V_{in} \leq V_o \\
\frac{1}{1-d_{2,fix}} I_o & V_o < V_{in} \leq V_{f2} \\
I_o & V_{in} > V_{f2} 
\end{cases}
\]

When the converter operates under the four-mode modulation scheme I, the inductor current ripple \( I_{\text{rip,4modeI}} \) and the average value \( I_{\text{avg,4modeI}} \) can be expressed as

\[
I_{\text{avg,4modeI}} = \begin{cases} 
\frac{V_o}{V_{in}} I_o & V_{in} \leq V_{f1d} \\
\frac{V_o(V_o - V_{in})}{L_f V_o} & V_{f1d} < V_{in} \leq V_o \\
\frac{V_o(V_o - V_{in}d_{1,fix})}{L_f V_o} & V_o < V_{in} \leq V_{f2} \\
\frac{V_o(1 - d_{1,fix})}{L_f} & V_{in} > V_{f2} 
\end{cases}
\]

\[
I_{\text{rip,4modeI}} = \begin{cases} 
\frac{V_o}{V_{in}} I_o & V_{in} \leq V_{f1d} \\
\frac{V_o(V_o - V_{in})}{L_f V_o} & V_{f1d} < V_{in} \leq V_o \\
\frac{V_o(V_o - V_{in}d_{max})}{L_f V_o} & V_o < V_{in} \leq V_{f2} \\
\frac{V_o}{V_{in}} I_o & V_{in} > V_{f2} 
\end{cases}
\]
When the converter operates under the four-mode modulation scheme II, the inductor current ripple $I_{\text{rip,4modeII}}$ and the average value $I_{\text{avg,4modeII}}$ can be expressed as

$$I_{\text{avg,4modeII}} = \begin{cases} V_o I_o & V_{\text{in}} \leq V_{\text{fix1}} \\ V_o d_{1\text{fix}} I_o & V_{\text{fix1}} < V_{\text{in}} \leq V_o \\ \frac{1}{1-d_{2\text{fix}}} I_o & V_{\text{in}} > V_{\text{fix2}} \end{cases} \tag{6-19}$$

$$I_{\text{rip,4modeII}} = \begin{cases} \frac{V_o(V_o - V_{\text{in}})}{L_f V_o} & V_{\text{in}} \leq V_{\text{fix1}} \\ \frac{V_o d_{2\text{fix}}}{L_f} & V_{\text{fix1}} < V_{\text{in}} \leq V_o \\ \frac{V_o}{L_f} (1-d_{1\text{fix}}) & V_{\text{in}} > V_{\text{fix2}} \\ \frac{V_o(V_o - V_{\text{in}})}{L_f} & V_{\text{in}} > V_{\text{fix2}} \end{cases} \tag{6-20}$$

$$I_{\text{avg,4modeII}} = \begin{cases} V_o I_o & V_{\text{in}} \leq V_{\text{fix1}} \\ \frac{1}{1-d_{2\text{fix}}} I_o & V_{\text{fix1}} < V_{\text{in}} \leq V_o \\ \frac{V_o}{V_o d_{1\text{fix}}} I_o & V_{\text{in}} > V_{\text{fix2}} \\ I_o & V_{\text{in}} > V_{\text{fix2}} \end{cases} \tag{6-21}$$

In order to clearly show the comparison among the inductor current ripples of the converter under different modulation schemes, the normalized current ripples are sketched in Fig. 6-10 by taking the maximum value of the current ripple under the one-mode modulation scheme $I_{\text{rip,1mode_max}}$, which can be obtained when the input voltage is at the highest value as shown in (6-22), as the base.

$$I_{\text{rip,1mode_max}} = \frac{V_{\text{in,max}} V_o}{L_f (V_o + V_{\text{in,max}})} \tag{6-22}$$

The parameters used to plot the figures are selected as $V_{\text{in}}=9 – 30$ V, $V_o=16.5$ V, $L=10$ µH, $P_o=36$ W, and $f_s=200$ kHz. Since it has been reported that the maximum and minimum limitations of the duty cycles are around 0.9 and 0.1, respectively [98, 105, 108], the limitations of the duty cycles used in this study are assumed as $d_{1\text{max}}=0.9$ and 0.1.
$d_{2\text{min}}=0.1$, then $d_{1\text{fix}}$ and $d_{2\text{fix}}$ can be calculated as $d_{1\text{fix}}=0.81$ and $d_{2\text{fix}}\approx 0.19$ according to the equations (6-4) and (6-5).

Fig. 6-10 shows that the inductor current ripple under the one-mode modulation scheme is the largest while the one under the two-mode modulation scheme is the smallest. The inductor current ripples under all three-mode and four-mode modulation schemes are the same as those under the two-mode modulation scheme when the input voltage is sufficiently higher or lower than the output voltage. When the voltage is slightly higher than the output voltage, the inductor current ripple under the four-mode modulation scheme I is smaller than the ones under other three/four-mode modulation schemes while the one under the three-mode modulation scheme I is larger than the ones under other three/four-mode modulation schemes. The inductor current ripples under the three-mode modulation scheme II and the four-mode modulation scheme II are the same, which is lower than the one under the three-mode modulation scheme III and higher than the four-mode modulation scheme I. When the voltage is slightly lower than the output voltage, the inductor current ripple under the four-mode modulation scheme I is still the smallest and the one under the three-mode modulation scheme I is still the largest among the ones under all three/four-mode modulation schemes. The inductor current ripples under the three-mode modulation scheme III and the four-mode modulation scheme II are the same, which is lower than the one under the three-mode modulation scheme II and higher than the four-mode modulation scheme I.

The comparison among the normalized average values of the inductor current of the converter under different modulation schemes is depicted in Fig. 6-11 by taking the maximum value of the inductor current average value under the one-mode modulation scheme $I_{\text{avg}_{-1\text{mode}}_{-\text{max}}}$ as the base. $I_{\text{avg}_{-1\text{mode}}_{-\text{max}}}$ can be expressed as,

$$I_{\text{avg}_{-1\text{mode}}_{-\text{max}}} = \frac{V_o + V_{\text{in}_{-\text{min}}}}{V_{\text{in}_{-\text{min}}}} I_o \cdot$$

(6-23)

Fig. 6-11 shows that the average value of the inductor current under different modulation schemes has the same trend as the inductor current ripples over the entire input voltage range.
Figure 6-10 Normalized inductor current ripples under different modulation schemes.

Figure 6-11 Normalized average value of the inductor current under different modulation schemes.

6.5 Implementation of Four-Mode Modulation I

As discussed in Section 6.4, the dead zone can be mitigated by inserting an extend-buck mode or/and an extend-boost mode.

In the extend-buck mode, the duty cycle $d_2$ is clamped at a constant value that is its minimum value or a value slightly higher than its minimum value, which means that the
active switch $S_2$ will be turned-ON for a fixed time interval in a switching period. The turned-ON time of the switch $S_2$ can be at the beginning, in the middle or the end of a switching period. In other words, this operating mode can be viewed as that the input voltage is boosted to a fixed relative higher value before it is bucked to the desired output voltage to ensure the duty cycle $d_1$ being in the reachable range.

When the converter shifts to operate in extend-boost mode, the duty cycle $d_1$ is clamped at a constant value that is its maximum value or a value slightly lower than its maximum value, which means that the active switch $S_1$ will be turned-OFF for a fixed time interval in a switching period. The switch $S_1$ can be turned OFF at the beginning, in the middle or the end of a switching period. In other words, this operating mode can be viewed as that the input voltage is bucked to a fixed relative lower value before it is boosted to the desired output voltage to ensure the duty cycle $d_2$ being in the reachable range.

Depending on the turned-ON time of the switch $S_2$ in the extend-buck mode and the turned-OFF time of the switch $S_1$ in the extend-boost operating mode, several control methods can be applied to implement the multi-mode modulation schemes.

As two examples, two implementations of the four-mode modulation scheme I will be presented in this section. Similar approaches can be applied to implement previously analysed other three/four-mode modulation schemes.

6.5.1 Turning ON the switch $S_2$ in the extend-buck mode and turning OFF the switch $S_1$ in the extend-boost mode in the middle of a switching period

In this implementation, the converter will operate in four modes, which are buck mode, boost mode, extend-buck mode and extend-boost mode. Some key waveforms among the components are shown in Fig. 6-12. When the converter operates in the buck mode and the boost mode, the waveforms are shown in Fig. 6-12(a) and Fig. 6-12(d), which are the same as the traditional buck converter and the traditional boost converter, therefore, the detailed operating processes will not be analysed in this section.
Figure 6-12 Some key waveforms of the converter in different operating mode of the implementation example A, (a) buck mode, (b) extend-buck mode, (c) extend-boost mode, (d) boost mode.

When the converter operates in extend-buck mode, there are four operating stages. The waveforms in the four operating stages are shown in Fig. 6-12(b). In operating stage 1, the equivalent circuit of the converter is shown in Fig. 6-13(a). The switch $S_1$ ($S_{1S}$) is turned OFF (ON) and the switch $S_2$ ($S_{2S}$) is turned OFF (ON) as well, and the inductor current is decreasing. The equivalent circuit of the converter in operating stage 2 is shown in Fig. 6-13(b). In this operating stage, the switch $S_1$ ($S_{1S}$) is turned ON (OFF) and the switch $S_2$ ($S_{2S}$) is still turned OFF (ON) till the middle of the switching period. Then the converter shifts to operate in operating stage 3, the equivalent circuit is shown in Fig. 6-13(c). The switches $S_1$ and $S_2$ are both turned ON while the switches $S_{1S}$ and $S_{2S}$ are turned OFF, and the inductor current is increasing. Operating stage 3 ends at the time $(0.5+d_{2\text{min}})T_s$ ($T_s$ is the switching period), which is the start of the operating
stage 4. The operation principle in the operating stage 4 is the same as that in the operating stage 2. This operating stage will last until the end of the switching period.

When the converter operates in the extend-boost mode, there are also four operating stages. The waveforms in the four operating stages are shown in Fig. 6-12(c). During the operating stage 1, the equivalent circuit of the converter is shown in Fig. 6-13(c). The switch $S_1$ ($S_{1S}$) is turned ON (OFF) and the switch $S_2$ ($S_{2S}$) is turned ON (OFF) as well, and the inductor current is increasing. The equivalent circuit of the converter in operating stage 2 is shown in Fig. 6-13(b). In this operating stage, the switch $S_1$ ($S_{1S}$) is
turned ON (OFF) and the switch \( S_2 \) (\( S_{2S} \)) is turned OFF (ON) till the middle of the switching period. Then the converter shifts to operate in the operating stage 3, the equivalent circuit is shown in Fig. 6-13(a). The switch \( S_1 \) (\( S_{1S} \)) is turned OFF (ON) and the switch \( S_2 \) (\( S_{2S} \)) is turned OFF (ON), and the inductor current is decreasing. This operating stage ends at the time \( (1.5-d_{1\text{max}})T_s \), which is the beginning of the operating stage 4. The operation principle in the operating stage 4 is the same as that in the operating stage 2. This operating stage will last till the end of the switching period.

### 6.5.2 Turning ON the switch \( S_2 \) in the extend-buck mode at the beginning and turning OFF the switch \( S_1 \) in the extend-boost mode both at the end of a switching period

The converter will operate in four modes including buck mode, boost mode, extend-buck mode and extend-boost in this implementation according to the relationship between the input voltage and the output voltage. Some key waveforms of the components are shown in Fig. 6-14. When the converter operates in buck mode and the boost mode, the waveforms are shown in Fig. 6-14(a) and Fig. 6-14(d), which are the same as buck and boost converters, respectively; therefore, the detailed operating processes will not be analysed in this section.

When the converter operates in the extend-buck mode, there are three operating stages. The waveforms in the three operating stages are shown in Fig. 6-14(b). In operating stage 1, the equivalent circuit of the converter is shown in Fig. 6-13(c). The switch \( S_1 \) and switch \( S_2 \) are both turned ON while the switch \( S_{1S} \) and \( S_{2S} \) are turned OFF and the inductor current is increasing. Operating stage 1 ends at the time \( d_{2\text{min}}T_s \), which is the start of the operating stage 2. In operating stage 2, the equivalent circuit of the converter is shown in Fig. 6-13(b). The switch \( S_1 \) (\( S_{1S} \)) is still turned ON (OFF) while the switch \( S_2 \) (\( S_{2S} \)) is turned OFF (ON) in this stage. In operating stage 3, both of the switches \( S_1 \) and \( S_2 \) are turned OFF and the inductor current is decreasing till the end of the switching period.

When the converter operates in the extend-boost mode, there are also three operating stages. The waveform in the three operating stages is shown in Fig. 6-14(c). In operating stage 1, the equivalent circuit of the converter is shown in Fig. 6-13(c). The
switches $S_1$ and $S_2$ are both turned ON and the inductor current is increasing. In operating stage 2, the equivalent circuit of the converter is shown in Fig. 6-13(b). The switch $S_1$ is still turned ON while the switch $S_2$ is turned OFF. This operating stage ends at the time $d_{1\text{max}}T_s$, which is the shifting time from stage 2 to stage 3. In operating stage 3, both of the switches $S_1$ and $S_2$ are turned OFF and the inductor current is decreasing till the end of the switching period.

![Diagram](a)

![Diagram](b)

![Diagram](c)

![Diagram](d)

Figure 6-14 Some main key waveforms of the converter in different operating mode of the implementation example B, (a) buck mode, (b) extend-buck mode, (c) extend-boost mode, (d) boost mode

### 6.6 Experimental results

To show the applicability of the proposed strategies under different conditions, two prototypes have been built and tested to verify the effectiveness of the two implementations presented in Section 6.5 accordingly. The experimental environments
of the two prototypes are the same and a simplified block diagram of the experimental environment is shown in Fig. 6-15. It should be claimed that different control methods like voltage mode control methods and current mode control methods can all be used as the control algorithm to implement the proposed modulation schemes in practical applications such as the battery charging or supplying systems and some control algorithm concepts have been studied in the literatures [95, 100-102, 105-106]. With the benefits of improved transient response, satisfied output immunity to the input variance, self-protection against over current and easiness for parallel operating of several converters, the current programmed control method is adopted in this thesis.

Table 6-1 Parameters of the components and specifications of the prototypes

<table>
<thead>
<tr>
<th>Components</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFETs S₁, S₁S, S₂, S₂S</td>
<td>SIR882DP-T1-GE3</td>
</tr>
<tr>
<td>Inductor L</td>
<td>10 µH</td>
</tr>
<tr>
<td>Input filter capacitor Cᵢ</td>
<td>2<em>47 µF Aluminium Electrolytic capacitors and 2</em>4.7 µF ceramic capacitors connected in parallel</td>
</tr>
<tr>
<td>Output capacitor Cₒ</td>
<td>2<em>220 µF Aluminium Electrolytic capacitors and 2</em>4.7 µF ceramic capacitors connected in parallel</td>
</tr>
<tr>
<td>Input voltage Vᵢn</td>
<td>9 – 30 V</td>
</tr>
<tr>
<td>Output voltage Vₒ</td>
<td>16.5 V</td>
</tr>
<tr>
<td>Rated power</td>
<td>36 W</td>
</tr>
<tr>
<td>Switching frequency fₛ</td>
<td>200 kHz</td>
</tr>
</tbody>
</table>

The components used in the two prototypes are listed in Table 6-1. A reconfigurable battery pack using the NCR18650PF Li-ion batteries is used to test the dynamical performance of the converter when the input voltage experience suddenly changes and a DC power supply is used for other tests. The differential probes of type THDP0200 and the probes of type TPP0250 are used for measuring the voltage information while the
current probes of type TCP0030A are used for measuring the current. All of the waveforms are recorded by the oscilloscope Tektronix MDO3024.

Figure 6-15 Simplified block diagram of the experimental environment

Fig. 6-16 shows the waveforms of the input voltage, the output voltage and the inductor current while Fig. 6-17 shows the switching sequences of the four switches of the implementation example A. The waveforms of the input voltage, the output voltage and the inductor current of the implementation example B are shown in Fig. 6-18 while the switching sequences of the four switches are shown in Fig. 6-19. It can be seen that the waveforms of the two prototypes are all corresponding well with the theoretical analysis.
Figure 6-16 Waveforms of the inductor current, the input voltage, and the output voltage of the implementation example A, (a) boost mode, (b) extend-boost mode, (c) extend-buck mode, (d) buck mode.
Figure 6-17 Waveforms of the driving signals of the implementation example A, (a) boost mode, (b) extend-boost mode, (c) extend-buck mode, (d) buck mode.
Figure 6-18 Waveforms of the inductor current, the input voltage, and the output voltage of the implementation example B, (a) boost mode, (b) extend-boost mode, (c) extend-buck mode, (d) buck mode.
In order to demonstrate the dynamical performance of the converter with the proposed modulation strategies, some tests with variation of the input voltage and load condition has been worked out for the two prototypes. The measured results from the implementation example A is shown in Fig. 6-20 and Fig. 6-21. Fig. 6-20 gives the waveforms of the output voltage when the load has suddenly changes under different input voltage conditions. It can be seen that the output voltage remains highly stable during the change of the load condition and the output voltage ripple increases slightly with the increase of the output power under all input voltage conditions. Note that the input voltage sees a slight change according to the change of the load condition, this is the effect caused by the internal resistance of the input source. The waveforms indicate that the load transient response of the converter with the proposed four-mode modulation scheme I is satisfactory.
Fig. 6-20 Waveforms of load change under different operating modes, (a) $V_{in}=10V$, (b) $V_{in}=16V$, (c) $V_{in}=17.5V$, (d) $V_{in}=24V$.

Fig. 6-21 shows the waveforms of the output voltage and output voltage ripples when the input voltage experiences smoothly and suddenly changes. It can be seen that the output voltage is stable during the transient period under all input voltage changing conditions. Hence, the satisfied input voltage transient response of the converter is verified. As similar transient performance has been obtained for the implementation example B, hence they are not presented in this paper. The experimental results well demonstrate the effectiveness of the four-mode modulation scheme I.

Fig. 6-22 sketches the power conversion efficiency of the implementation example A versus the input voltage under three different load conditions. It can be seen that the converter with the four-mode control method can obtain over 97% efficiency in the entire input voltage range under all load conditions. The power conversion efficiency of the implementation example B reaches over 96% in the experiment. The results
demonstrate that the non-inverting buck–boost converter can obtain satisfied efficiency with the proposed dead-zone elimination strategies.

![Waveforms](image)

(a)  

(b)  

(c)  

Figure 6-21 Waveforms of input voltage change under different load conditions, (a) input voltage increases smoothly, (b) input voltage decreases smoothly, (c) input voltage experiences suddenly change.

Figure 6-22 Efficiency of the implementation example A.
6.7 Summary

The origin of the dead zone hidden in the high-efficiency two-mode modulation scheme of the non-inverting synchronous buck-boost converter is demystified in this chapter. Based on this, a series of three-mode and four-mode modulation schemes are derived systematically to eliminate the dead zone. The inductor performance under different modulation schemes are analysed and compared as an evaluation for these modulation methods. Two implementation examples of the proposed four-mode modulation scheme I is presented and verified by experimental results in this chapter. This chapter can be an appropriate guidance for developing new control methods to implement smooth mode transition and high efficiency operation of the non-inverting synchronous buck-boost converter in practical applications such as the battery charging or supplying systems.
Chapter 7  Conclusions and Future Work

7.1  Conclusions

The traditional boost converter, traditional buck-boost converter, and non-inverting buck-boost converters are widely used in battery applications. However, there are still some limitations within these converters. This thesis aims to improve the input current ripple issues in the traditional boost converter, to extend the voltage conversion ratio of the traditional boost converter and the traditional buck-boost converter, and to reveal the origin and derive novel modulation methods for completely elimination of the dead zone existed in the non-inverting buck-boost converter when it is working in two-mode operation scheme.

Chapter 2 discussed some related existing research work, which includes the high gain boost converters, the input current ripple cancellation methods, the quadratic converters, and technologies to improve the performance of the non-inverting buck-boost converter.

Chapter 3 presented a novel high gain quadratic boost converter based on the combination of a voltage multiplier circuit and a traditional quadratic boost converter. Compared with the traditional quadratic boost converter, the proposed converter can obtain a much higher output voltage under the same duty cycle and input voltage, and can also reduce the voltage stresses in the power devices. Moreover, the serious input current ripple experienced by some other coupled-inductor based high gain converters has been released effectively. Consequently, the efficiency and the reliability can be improved by using semiconductors with low voltage level and high performance. The theoretical analysis of the proposed converter has been verified by the experimental results.

Chapter 4 proposed a \( \Delta-Y \) hybrid impedance network based boost converter to deal with the input current ripple issue for the traditional boost converter. The \( \Delta-Y \) hybrid impedance network is formed by the TBC’s main inductor, an additional coupled inductor, and an additional resonant inductor and capacitor pair. The proposed converter remains the TBC’s original structure and voltage conversion feature while effectively
reduce the input current ripple and the average current of the main inductor. The operation principle of the proposed converter has been explained and the mechanism of current ripple reduction has been analysed in detail. Experimental results are carried out to validate the effectiveness of the proposed converter.

Chapter 5 developed a single-switch quadratic buck-boost converter with non-pulsating input port current and non-pulsating output port current. The proposed converter has a wider voltage conversion ratio than that of the traditional buck-boost converter. The operating principle and steady-state performance of the proposed converter under continuous inductor current mode have been analysed in detail. The comparison between the proposed converter and the existing quadratic buck-boost converters has been conducted. Experimental results from a prototype built in the lab were recorded to verify the effectiveness and validity of the proposed quadratic buck-boost converter.

Chapter 6 analysed the relationship between the duty cycles of the active switches and the voltage conversion ratio of the non-inverting buck-boost converter from a novel perspective and the origin of the dead zone existed in the operation process of the converter operating in buck and boost mode has been demystified based on the analysis. A series of three-mode and four-mode modulation schemes are systematically derived to completely eliminate the dead zone. The ripple and average value of the inductor current under different modulation schemes are investigated to evaluate the performance of these modulation schemes. Two implementations of a four-mode modulation scheme were presented and experimentally tested as the examples for all modulation schemes to demonstrate the effectiveness of the proposed modulation schemes.

7.2 Future Work

Some possible extensions to the research conducted in this thesis can be summarised as follows.

1. The development of novel step-up converters with higher voltage conversion ratio and simple structure can be conducted for current and future applications.
2. A general rule or a unified topology to develop high gain step-up converters could be investigated for practical applications.

3. More detailed analysis including the discontinuous current mode operation of the converters proposed in this thesis could be completed in the future.

4. Novel input current ripple cancellation method could be studied and the applicability of the input current ripple cancellation methods for the output current ripple cancellation could be investigated.

5. Optimisation of the components parameter design for the non-inverting buck-boost converter can be conducted to obtain minimum output voltage ripple.
Bibliography


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