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Keywords
distributed, generation, limiter, current, link, dc, inverter, scheme, fault, ride

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A DC-Link Fault Current Limiter-Based Fault Ride-Through Scheme for Inverter-Based DGs

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***Abstract*— Due to increasing the penetration level of the inverter-based distributed generations (IBDGs) in power systems, their fault ride-through (FRT) capability has become one of the essential issues of new grid codes. This paper proposes a novel dc link fault current limiter (DLFCL) based FRT scheme to improve the FRT capability in IBDGs units. The DLFCL module has almost no effect on normal operation of IBDG unit. When a short-circuit fault occurs in power system, the DLFCL module effectively limits inverter output current and protects its switching devices. The employed DLFCL does not need any control, measurement and gate driving system. Also, it has simple configuration and it isn't mandatory to use superconductor inductor in its power circuit so, it has low initial cost. By using the proposed scheme, it is possible to provide continues operation of IBDG unit even at zero grid voltage. Analytical analysis is presented in detail. The effectiveness of proposed approach is approved through extensive simulation studies in PSCAD/EMTDC environment. An experimental setup is used to verify the main concept of the proposed approach.**

***Keywords*—Distributed generation; fault ride-through; voltage sourced inverter; dc link, fault current limiter.**

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I. INTRODUCTION

There are many technologies for distributed generations (DGs) beyond the conventional synchronous generators such as fuel cells, wind turbines, solar cells and micro turbines which use inverter for power exchange with the utility grid [1]. These types of DGs require voltage-source inverter (VSI) in most cases to interconnect with grid and are usually referred as inverter based distributed generations (IBDGs) [2].

Two main control strategies are proposed in literatures to control the interface-inverter in DG systems which are: Current Control Strategy (CCS) and Voltage Control Strategy (VCS) [3]-[5]. From the advantages of CCS is that, during fault condition, the output current of inverter can be effectively restricted to an acceptable level, consequently, the IBDG unit can ride-through networks faults. However, CCS has several drawbacks like reduction of main controller robustness and need to both voltage and current sensors. On the other hand, while VCS has good performance during normal operation, high level of fault current is its main drawback [4]. By increasing the penetration level (PL) and island operation of DG units in distribution systems, using of VCS to controls interface-inverter is more acceptable than CCS [6]. Furthermore, at high PL of the IBDG units in power system, their disconnection form utility during faults is not acceptable. Also, according to [7], the effect of IBDG units on network operation with 40% PL is not negligible.

Despite the IEEE standard 1547 which recommended that IBDGs units should be disconnected from the network when a fault occurs in the utility grid [8] in some new grid codes, the IBDGs units are forced to stay connected to the grid and ride-through network faults [9]-[10]. Regarding to above discussions different studies are conducted on current limitation strategies of VSIs during network faults.

Some control approaches for inverter-interfaced distributed energy resources are proposed in [11] and [12] to limit inverter fault current and improve their fault ride-through (FRT) capability. Reference [13], introduced an inverter fault current limitation strategy in a micro-grid at high PL of IBDG units. However, [13] did not present simulation and experimental results to approve its proposed technique. References [14]

and [15] investigated fault behavior of IBDGs units against various network faults and presented analytical and experimental results. A control scheme is proposed in [16] to improve ride-through capability of hybrid distributed energy resources including fuel cell/battery during power system faults. In [17], a control strategy proposed to enhance the voltage support ancillary service of IBDG unit to compliant the grid codes requirements. A fault protection scheme against the external short-circuit fault for the high-power three-phase inverters is proposed in [18] to provide high reliability for sensitive loads during transient faults. A control scheme is introduced in [19] to suppress the peak of three-phase PV inverters current during unsymmetrical faults. Reference [20] presented simulation and experimental results of a varistor based short circuit fault protection scheme for series active power filters.

An effective method to control the fault current level is using fault current limiters (FCLs). Several types of FCLs are proposed to improve the power system performance in [21]-[24]. Also, as [25], it is expected, in the future, FCLs might be coupled with DGs units and sold as an important part of these generation plants.

This study proposes a novel dc link fault current limiter (DLFCL) based FRT scheme to improve the FRT capability in IBDG units. The DLFCL module has not effect on IBDG system performance during normal operation of utility grid but, it limits the inverter current in fault condition. In this way, the IBDG system can stay connect to utility during fault condition. Moreover, the proposed DLFCL could make use of non-superconducting inductor to decrease initial cost of superconducting inductor as well as the cost and volume of cryogenic system. Besides, according to [26], the problems of latch-up and wind-up arise when the inverter control strategy changes from normal, to fault mode operation, during fault condition. However, in the proposed scheme, interface-inverter is controlled as a controlled voltage source in normal condition as well as fault condition. Also, by present scheme, the FRT is possible even at zero grid voltage as recommended by E.ON grid code [10].

The rest of this paper is organized as follows: Section II deals with basis of proposed scheme. Section III explains performance evaluation of proposed FRT approach. Section V and IV includes the simulation studies and experimental results, respectively. Finally, section VI provides concludes of paper.

II. Proposed Fault Ride Through Configuration

Fig .1 shows the power circuit topology of proposed FRT configuration for an IBDG unit. Based on [2], the model of IBDG unit for the purpose of fault analysis can be made up under the assumption that in sub-transmission systems the dc input voltage of the interface VSI is regulated and essentially fixed in the time frame 0-1.0 s. Nevertheless, the V_{DC} that is shown in Fig. 1 is considered as average of DC voltage during fault to simplify the analytical analysis. To enhance FRT capability of IBDG unit, application of a diode-bridge DLFCL module is proposed. The Non superconducting DLFCL module is composed of a diode-bridge and a non-superconductor (copper coil) that is modeled by a resistor r_d and an inductor L_d in Fig. 1. In case of using superconductor inductor, r_d will be equal to zero. A two-level VSI is used for DC to AC power conversion. The DLFCL module is connected in series with V_{DC} as shown in Fig. 1. Also, total resistance and inductance between high voltage side of grid-connected transformer and inverter output terminals are modeled by r_s and L_s in Fig. 1, respectively. The utility grid is modeled by an infinitely stiff AC system; so it is represented by an ideal sinusoidal three-phase voltage source with a constant frequency (V_{an}, V_{bn} and V_{cn} in Fig. 1), where ω and V_ϕ stand for its angular frequency and effective voltage value in each phase, respectively.

In proposed scheme, just one single set of FCL module is required in DC side of inverter. This new idea, in comparison with current limiting in AC side of inverter which needs three similar sets of FCL modules results in considerable reduction of cost. The present FRT method does not need any control, measurement and gate deriving system. The proposed FRT solution has the potential of easily implementation by commercial inverter manufacturer companies with least design efforts and engineering cost. By choosing

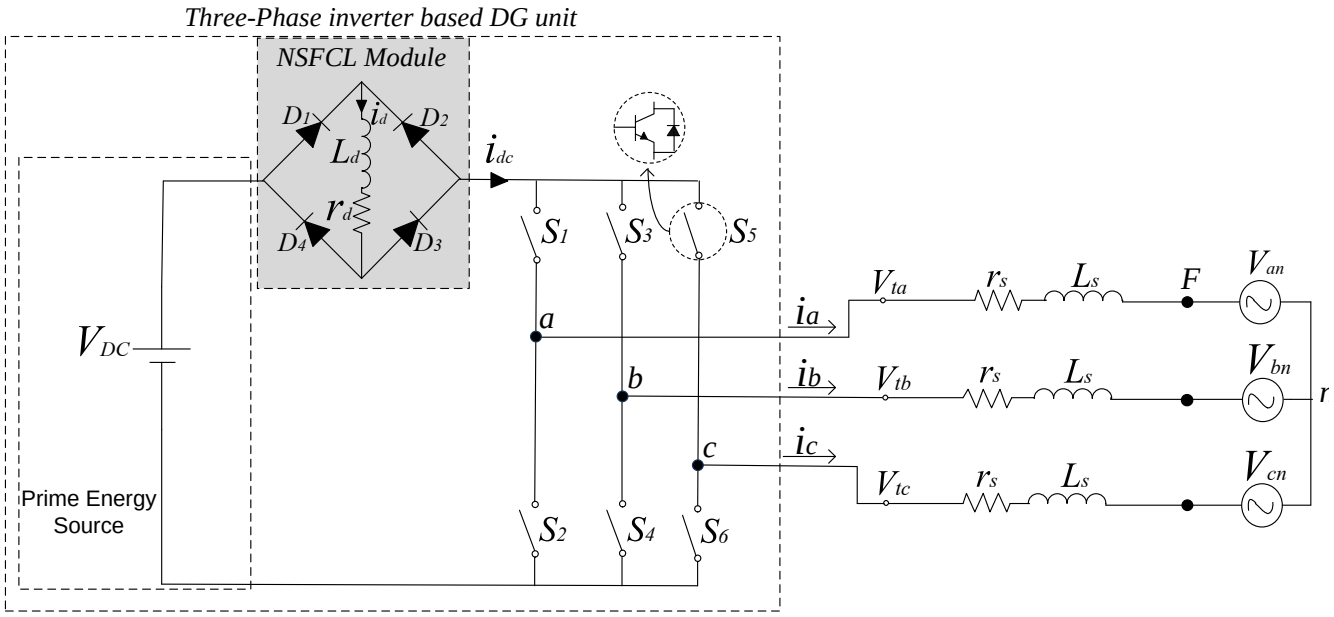

Fig. 1. Power circuit topology of the proposed fault ride-through configuration for an inverter based distributed generation.

an appropriate value for L_d in Fig. 1, it is possible to achieve a nearly dc current for dc reactor at steady state. Therefore, the dc reactor has no significant role in normal operation of inverter but, if a short circuit occurs in power system, the dc reactor can effectively suppresses severe *di/dt* initiated in the first moments of fault and it can decreases inverter fault current successfully over the fault duration.

III. Performance Evaluation of Proposed FRT Scheme

A. Analytical Analysis

In order to analysis the operation of VSI along with DLFCL module, it is assumed that AC line currents (i_a, i_b and i_c) of inverter are pure sinusoidal and inverter is controlled by VCS. In the analytical analysis, each semiconductor device of inverter and DLFCL module is modeled by series connection of its voltage drop (V_d) and resistance (r_{on}) in on state. The switching signals of semiconductor devices are generated by sinusoidal PWM strategy. So, the dc link current (i_{dc}) can be expressed in the basis of AC line currents and switching states as follow [27]-[28]:

$$i_{dc} = S_a i_a + S_b i_b + S_c i_c = 3[I_l S_{abc} \cos(\Theta - \phi)]/2 \qquad (1)$$

Where, S_a, S_b and S_c are the switching states of the phases *a*, *b* and *c*, respectively. Also, in (1), I_l denotes peak value of AC line current, ϕ represents the power factor angle and Θ incorporates the phase angle and frequency information [27]-[28].

Since, in carrier based PWM inverters, the carrier frequency is very high in comparison with the fundamental output frequency, it is expected to assume that the value of modulating signal over one carrier period is almost constant [3], [27]. In this section, the performance of proposed scheme is explained during one carrier period. The analytical analysis is performed in three modes of operation as follows.

A.1. Mode 1: Pre-fault operation

In this study, for a better understanding of the performance of proposed FRT scheme, the charging and discharging operating condition of dc reactor in non-superconducting DLFCL module is analyzed. Fig. 2(a) shows the dc link current i_{dc}, dc reactor current i_d and switching sequence of interface-inverter during normal operation. As is shown, by changing the switching state, i_{dc} changes instantaneously. Also, during one carrier period, i_d is a rectified but periodic current. In time interval T'_0, switching state is (000) and dc reactor current is more than dc link current ($i_{dc}=0$). Fig. 2(b) shows the equivalent circuit during time interval T'_0. According to equivalent circuit, over the time interval T'_0, the dc reactor is in discharging mode. During discharging mode all of diodes of DLFCL module are in on-state and i_d freewheels through D_2-D_3 and D_1-D_4. So, differential equation of dc reactor current can be expressed as follow:

$$\left(r_d + 2r_{on}\right) i_d(t) + L_d \, di_d(t)/dt + 2V_d = 0 \qquad (2)$$

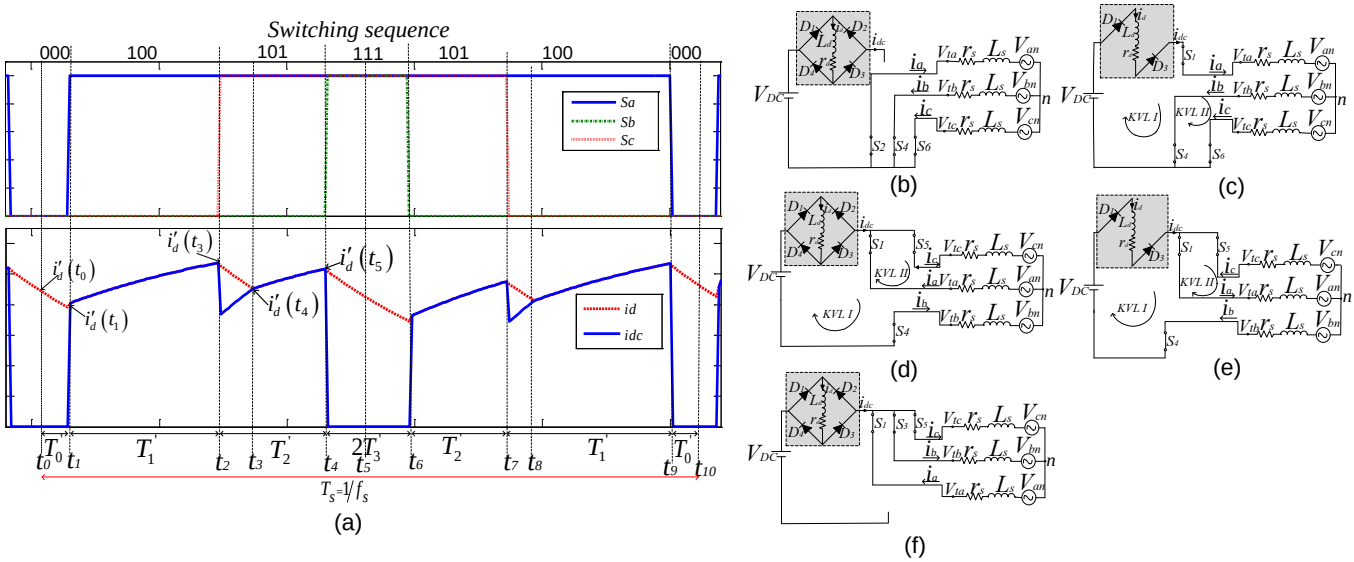

Fig. 2. (a) PWM output sequence from VSI and measured dc link (i_{dc}) and dc reactor (i_d) currents during normal operation. (b)-(f) shows the equivalent circuits of operating intervals during normal operation: (b) switching state (000), (c) switching state (100), (d) switching state (101), (e) switching state (101), and (f) switching state (111).

Where r_d, L_d, r_{on} and V_d stands for dc reactor resistance, dc reactor inductance, on state resistance and forward voltage drop across each semiconductor device, respectively. Solution (2), leads to (3) which represents the dc reactor current formula during discharging mode in normal operation condition:

$$i_d(t) = e^{-(t-t_0)(r_d+2r_{on})/L_d}\left\{i_1' + (2V_d)/r_d+2r_{on}\right\} - (2V_d)/r_d+2r_{on} \qquad (3)$$

Where, $i_1'=i_d(t_0)$.

At $t=t_1$, the switching state changes to (100). Fig. 2(c) shows the equivalent circuit for t_1 to t_2. As equivalent circuit reveals, i_d is equal with i_{dc} and dc reactor is in charging mode. By applying Kirchhoff Voltage Law (KVL) in circuit loops of Fig. 2(c), the dc reactor current differential equation can be expressed as (4):

$$(3/2L_S+L_d)\,di(t)/dt + \left(r_d + 7/2\,r_{on} + 3/2\,r_s\right)i(t) = V_{DC} - 4V_d - 3/2V_\phi\cos(\omega t) \qquad (4)$$

Equation (5) is derived by using (4) and shows the dc reactor current formula in charging mode during normal operation.

$$i(t) = Ae^{-(t-t_1)/\tau_1} + B\cos(\omega t-\theta) + K \qquad (5)$$

Where,

$$\begin{cases} A = i_2' - \dfrac{3V_\phi}{2\sqrt{r_{c1}^2 + \left((3/2\,L_s + L_d)\omega\right)^2}} - \dfrac{V_{DC} - 4V_d}{r_{C1}}, K = \dfrac{V_{DC} - 4V_d}{r_{C1}}, \theta = \tan^{-1}\left(\dfrac{3L\omega}{2r_{c1}}\right), \tau_1 = \dfrac{3L_s}{2r_{c1}} \\ B = \dfrac{3V_\phi}{2\sqrt{r_{c1}^2 + \left((3/2\,L_s + L_d)\omega\right)^2}}, i(t) = i_d(t) = i_{dc}(t), i_2' = i(t_1), r_{c1} = r_d + \dfrac{7}{2}r_{on} + \dfrac{3}{2}r_s. \end{cases}$$

At $t=t_2$, switching state changes to (101) and i_{dc} changes instantaneously. So, during time interval t_2 to t_3, the dc reactor current is more than dc link current and the dc reactor is in discharging mode (Fig. 2(d)). At $t=t_3$, switching state is not changed but the dc reactor current is equal with the dc link current and charging mode begins and continues till t_4, (Fig. 2(e)).

At $t=t_4$, switching state changes to (111) and the dc link current instantaneously reduced to zero. So the dc reactor is in discharging mode till t_5 (Fig. 2(f)). It should be noted that, the time interval between t_0 to t_5 is half of carrier period so, the above mentioned analysis can be implemented for the rest of this period until t_{10}.

A.2. Mode 2: During fault condition

For analysis of fault condition, a three phase Y-connected short-circuit fault with impedance $Z_f = r_f + jL_f\omega$ is applied at point F, as shown in Fig. 1, at $t=t_{10}$. Fig. 3(a) shows the dc link current i_{dc}, the dc reactor current i_d and the switching sequence of inverter during fault condition. During time interval t_{10} to t_{11} switching state is (000). Fig. 3(b) shows the equivalent circuit during time interval T_0. As the equivalent circuit shows, i_{dc} is equal with zero and the dc reactor is in discharging mode. The following differential equation can be expressed for dc reactor current:

$$\left(r_d + 2r_{on}\right) i_d(t) + L_d\, di_d(t)/dt + 2V_d = 0 \qquad (6)$$

Equation (7) is derived by using (6) and shows the dc reactor current formula during discharging mode:

$$i_d(t) = e^{-(t-t_{10})(r_d + 2r_{on})/L_d}\left\{i_1 + (2V_d)/r_d + 2r_{on}\right\} - (2V_d)/r_d + 2r_{on} \qquad (7)$$

Where $i_d(t_{10})=i_1$.

At $t=t_{11}$ switching state changes to (100). Fig. 3(c) shows the equivalent circuit during time interval t_{11} to t_{12}. According to equivalent circuit, over the time interval T_1, i_{dc} is equal with i_d and the following differential equation can be expressed:

$$(L_d + 3/2\, L_e)\, di(t)/dt + \left(r_d + 7/2\, r_{on} + 3/2\, r_e\right) i(t) = V_{DC} - 4V_d \qquad (8)$$

Where, $L_e=L_s+L_f$, $r_e=r_s+r_f$. The following equation is derived by using (8) and shows the dc reactor and dc link current formula in charging mode and during fault condition:

$$i(t) = e^{-(t-t_{11})/\tau_1} \left\{ i_2 - (V_{DC} - 4V_d)/r_{c1} \right\} + (V_{DC} - 4V_d)/r_{c1} \qquad (9)$$

Where $i(t)=i_d(t)=i_{dc}(t)$, $i_2=i_d(t_{11})$, $\tau_2=(3/2L_e+L_d)/r_{c2}$, $r_{c2}=r_d+7/2r_{on}+3/2r_e$.

At $t=t_{12}$, switching state changes to (101). Fig. 3(d) shows the equivalent circuit during time interval t_{12} to t_{13}. During this time interval, the dc reactor current is more than the dc link current and dc reactor begins to discharge through diodes D_2-D_3 and D_1-D_4. So, the dc reactor current formula is as (10):

$$i_d(t) = e^{-(t-t_{12})(r_d + 2r_{on})/L_d} \left\{ i_3 + (2V_d)/r_d + 2r_{on} \right\} - (2V_d)/r_d + 2r_{on} \qquad (10)$$

Where, $i_d(t_{12})=i_3$.

In addition, according to Fig. 3(d), it is possible to write the dc link current differential equation as:

$$3/2\, L_e\, di_{dc}(t)/dt + 3/2\, (r_e + r_{on}) i_{dc}(t) = V_{DC} - V_d \qquad (11)$$

Solution (11) leads to (12) that represent the dc link current formula during time interval t_{12} to t_{13} during fault condition:

$$i_{dc}(t) = e^{-(t-t_{12})/\tau_3} \left\{ i_3 - (V_{DC} - V_d)/r_{c2} \right\} + (V_{DC} - V_d)/r_{c2} \qquad (12)$$

Where, $i_3=i_{dc}(t_{12})$, $\tau_3=L_e/(r_e+r_{on})$.

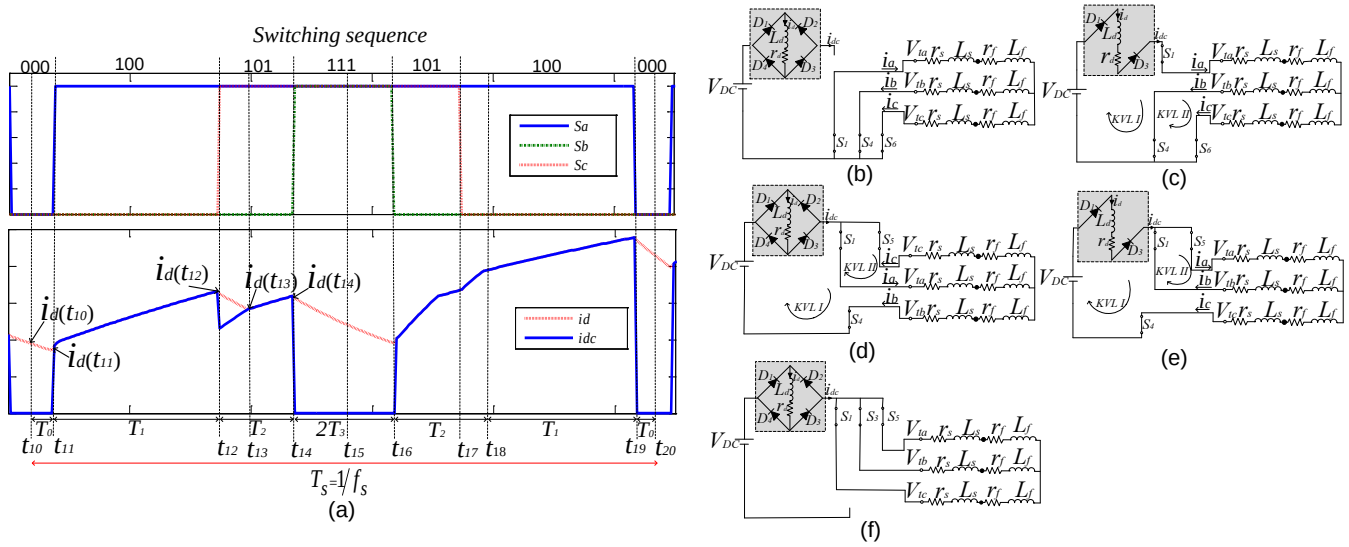

Fig. 3. (a) PWM output sequence from VSI and measured dc link current (i_{dc}) and dc reactor current (i_d) during fault condition. (b)- (f) shows the equivalent circuits of operating intervals during fault condition: (b) switching state (000), (c) switching state (100), (d) switching state (101), (e) switching state (101), and (f) the switching state (111).

At $t=t_{13}$, the dc reactor current is equal with dc link current. Therefore, the dc reactor is in charging mode till $t=t_{14}$ while switching state is (101). Fig. 3(e) shows the equivalent circuit during time interval t_{13} to t_{14}. According to the equivalent circuit, the following differential equation can be obtained:

$$(L_d + 3L_e/2)\, di(t)/dt + r_{c3} i(t) = V_{DC} - 3V_d \qquad (13)$$

Equation (14) is derived based on the (13) as follows:

$$i(t) = e^{-(t-t_{13})/\tau_4} \left\{ i_4 - \left(V_{DC} - 3V_d\right)/r_{c3} \right\} + \left(V_{DC} - 3V_d\right)/r_{c3} \qquad (14)$$

Where $i(t)=i_d(t)=i_{dc}(t)$, $i_4=i_d(t_{13})$, $\tau_4=\tau_2$, $r_{c3}=r_{c2}$.

At $t=t_{14}$, switching state changes to (111) and the dc link current instantaneously reduces to zero. Therefore, the dc reactor is in discharging mode. Fig. 3(f) shows the equivalent circuit during time interval t_{14} to t_{15}. According to the equivalent circuit, the dc reactor current can be obtained as (15):

$$i_d(t) = e^{-(t-t_{14})(r_d+2r_{on})/L_d} \left\{ i_5 + (2V_d)/r_d + 2r_{on} \right\} - (2V_d)/r_d + 2r_{on} \qquad (15)$$

Where $i_d(t_{14})=i_5$.

After $t=t_{15}$, circuit will have the same periodic operation according to the inverter switching state until protection system operation and clearing the fault.

A.3. Mode3: After clearance of fault

In this mode, the dc reactor current decreases because of its resistance and forward voltage drop on diodes. So, DLFCL will be short circuit. Fig. 4 shows that the dc reactor current discharges to its pre-fault value after some millisecond that is equal with peak value of dc link current. Now, the DLFCL module automatically becomes ready to limit any possible upcoming short circuit faults.

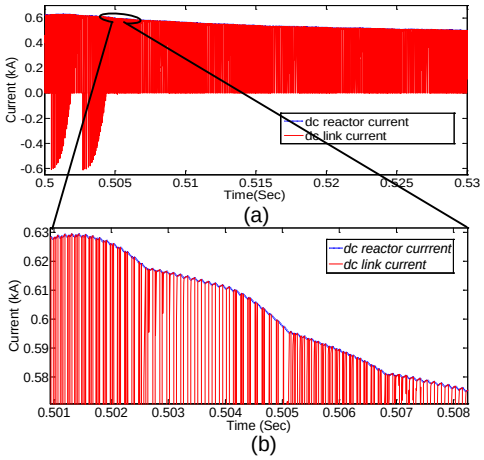

Fig. 4. DC reactor and DC link current after fault, (b) is enlarged of (a).

B. Design Consideration of DLFCL

B.1. DC reactor inductance calculation

To protect inverter semiconductor devices during short circuit condition, it is required to calculate the desired value of L_d. For this purpose, the dc reactor current charging formula in time interval t_{11} to t_{12} is used. Since time interval T_0 in Fig. 3(a) is very small percentage of one carrier period [27], this interval can be considered equal with zero. Now, as t_c considered as operating time of protection system and corresponding current represent by i_c, the following equation can be expressed according to (9):

$$i_c = e^{-(t_c - t_{11})/\tau_1}\left\{i_2 - (V_{DC} - 4V_d)/r_{C1}\right\} + (V_{DC} - 4V_d)/r_{C1} \qquad (16)$$

According to (16), it is possible to calculate the desired value of L_d as follows

$$L_d = \left(r_{c2}(t_c - t_1)/\ln\{B/(i_c - A)\}\right) - 3L_e/2 \qquad (17)$$

Where $B=i_2-(V_{DC}-4V_d)/r_{c1}$, $A=(V_{DC}-4V_d)/r_{c1}$.

B.2. Power losses assessment

As shown in section III-A, during normal operation, the current of dc reactor is an almost ripple-free dc current with amplitude equal to peak of dc link current. So, (18) can be writing as follows:

$$i_r \cong 0 \Rightarrow I_{DC} \cong I_{\max} \qquad (18)$$

Where, i_r, I_{DC} and I_{max} stand for ripple-current in dc reactor, the average current in dc reactor and peak value of dc link current in steady state, respectively. So, the total power loss of non-superconducting FCL (NSFCL) module (P_{Total}) is sum of DC reactor power loss (P_{DC}) and power loss of diode bridge (P_{Bridge}) and can be calculated as follows:

$$\begin{cases} P_{DC} \cong r_d I_{DC}^2 = r_d I_{\max}^2 \\ P_{Bridge} = 2V_d \times I_{DC} \\ P_{Total} = P_{DC} + P_{Bridge} = I_{DC}\left[r_d I_{DC} + 2V_d\right] \end{cases} \qquad (19)$$

Also, in absence of non-superconducting FCL module in series with dc link and in the case that the switching losses of interface inverter is neglected, (20) can be expressed for an inverter [30]:

$$\begin{cases} P_{ac\_inv} = v_a i_a + v_b i_b + v_c i_c \\ P_{DC\_inv} = V_{DC} i_{dc} \\ P_{ac\_inv} = P_{DC\_inv} \end{cases} \qquad (20)$$

Now, as the set of NSFCL module is connected in series with dc link of the inverter, AC side power can be expressed as follow:

$$P_{ac\_inv} = P_{DC\_inv} - P_{Total} \qquad (21)$$

For example, consider an IBDG unit with rated capacity of 6 MW, output phase voltage V_{abc_rms}=4kV , *P.F*=0.9 and dc link current approximately is i_{p_rms}=600(A). By installation of a NSFCL module in series with dc link with parameter of r_d=*0.01*(Ohm), V_d=3 (*V*) the power loss is P_{Total}=7200(W). The ratio of total power loss to active power of generated by IBDG unit is defined by K and can be derived as follows:

$$K = P_{Total} / P_{ac\_inverter} = I_{DC}\left[r_d I_{DC} + 2V_d\right] / P_{ac\_inverter} = 0.001 \qquad (22)$$

As another case, an IBDG unit is considered with rated apparent power of 100 KVA, output phase voltage V_{abc_rms}=500 V, $P.F$=0.6 and dc link current i_{p_rms}=20(A). By installation a NSFCL module with r_d=*0.005*(Ohm), V_d=2 (*V*) in series with dc link, the value of K for this system can be calculated as follows:

$$K = P_{Total} / P_{ac\_inverter} = 20\left[(0.005\times 20)+(4)\right] / 60kW = 0.0013 \quad (23)$$

This shows that in the presence of NSFCL module in dc link of interface-inverter, total power dissipation is very small percentage of overall rated power of IBDG unit and it can be acceptable for most practical applications. By using superconductor type inductor in dc link of diode bridge, it is possible to cancel out the power loss of inductor in the expense of higher initial cost and higher weight and volume of cryogenic system. Obviously, it is possible to use a parallel circuit breaker with FCL to bypass it during steady state and eliminate the power dissipation of FCL module during normal operation of IBDG unit.

B.3. *Voltage drop compensation*

Due to using diode-bridge and non-superconducting coil there is a voltage drop on the NSFCL module. It is possible to compensate the voltage drop by using a dc voltage source in series with dc reactor (as shown in Fig. 5) [21], [23]. If current through dc reactor is supposed to be a ripple-free dc current equal to I_{DC} the magnitude of dc voltage source can be calculated as follows:

$$V_{dc} = r_d I_{DC} + 2V_d \quad (24)$$

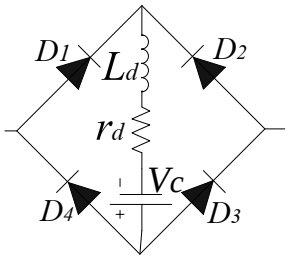

Fig. 5. NSFCL module with a dc voltage source.

IV. Simulation Results

Single line diagram of test system is shown in Fig. 6. The primary source of the IBDG unit is represented by a 5-kV DC voltage source. As shown in this figure, the primary source is interconnected to the utility grid through a two level VSI, a 4-kV/34.5kV step-up transformer (with the same power rating of corresponding IBDG unit) and a double-line transmission line. The utility grid is represented by a three phase AC voltage source with equivalent impedance of Z_g. The inverter operates through the simulation by VCS that is introduced in [2]. The IBDG unit simulation parameters can be found in [2], and network data are given in [29]. The PSCAD/EMTDC is implemented to simulate various fault conditions. To demonstrate the effectiveness of proposed FRT scheme extensive simulation studies are carried out under different fault conditions. The fault scenarios which are simulated include LLLG, LL and LG fault. Among the different grid codes which are in use by different grids operators in the worldwide, the E. ON grid code has severe FRT requirements [9]. According to the E. ON, if the voltage at point of common coupling drops to zero for 0.15 s, the DG unit must not disconnect from the grid. So, in the entire conducted simulations, fault clearing time is considered to be 0.15 s. Corresponding results provided in the following subsections.

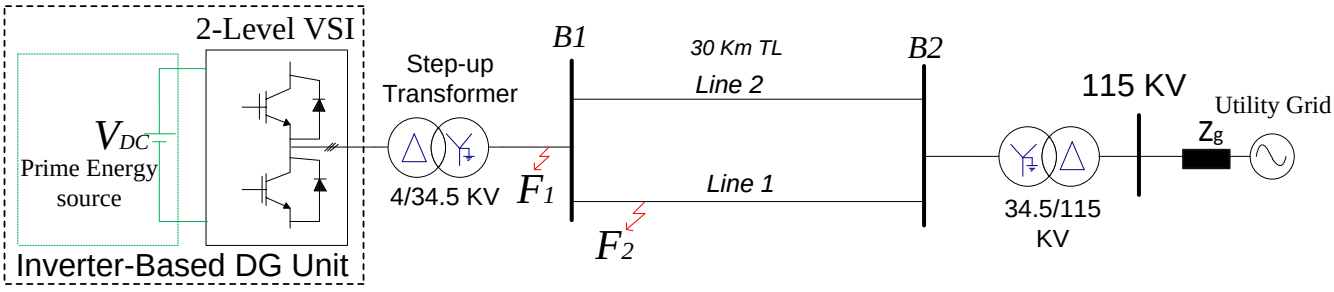

Fig. 6. Single line diagram of the under study test system.

A. Symmetrical fault

In this scenario, a bolted temporary LLLG fault is applied at point F1, as shown in Fig. 6, at *t=0.8* sec, with clearing time 0.15 s, as a worst scenario to causes a sever voltage dip (100%) at IBDG unit terminals. At first, the simulation is carried out while the FCL module is not connected in series with dc link of

inverter. The obtained results are shown in Fig. 7(a), (c) and (e). As shown in Fig. 7(a), once the fault occurs, voltage at IBDG terminal drops to zero. In this condition, the IBDG unit's output current increases suddenly. The peak value of IBDG unit's output current at the first moment of the fault reaches to around 4pu as shown in Fig. 7(c). A 2-level VSI with 6 power electronic switches (which are very vulnerable

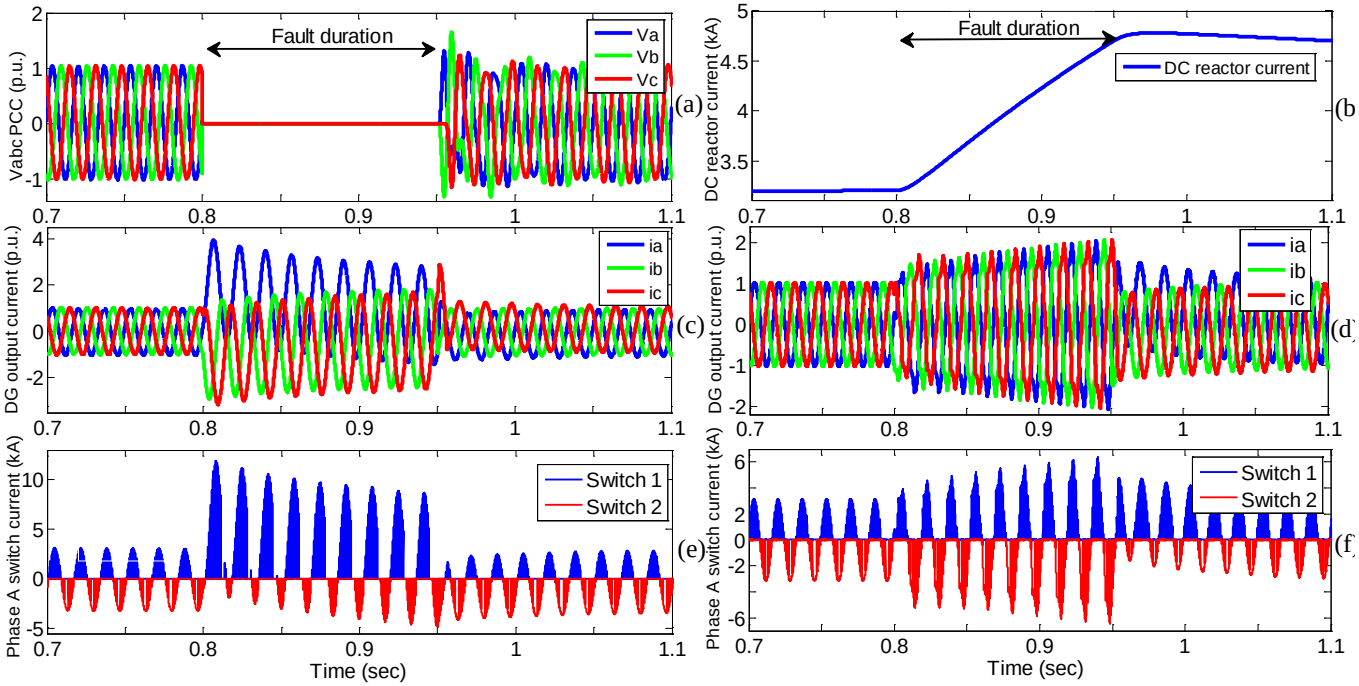

Fig. 7. Simulation results for an LLLG fault at point F1. (a) three-phase voltages at point F1. (b) DC reactor current. Three-phase output current of IBDG unit: (c) without DLFCL (d) with DLFCL. Phase A switch current of inverter: (e) without DLFCL (f) with DLFCL.

against short circuit condition) is used for DC to AC power conversion. The current through switches of phase A (S_1 and S_2 in Fig. 1) are shown in Fig. 7(e). As this figure shows, these over-currents reached about 4 times the nominal value and tend to damage semiconductors and/or trip out of IBDG unit in practical cases.

Now, to demonstrate the effectiveness of proposed FRT method, a bolted temporary LLLG fault with the same fault characteristics of the previous study is applied at point F1, in Fig. 6 while the FCL module is connected in series with dc link of the inverter. Corresponding results are shown in Fig. 7(b), (d) and (f). The dc reactor current is shown in figure 8(b). As this figure shows, during the fault period the dc reactor

current increases almost linearly. However, during the entire timeframe of fault (150 *ms*), the DLFCL module is capable to limit three phase output current of IBDG unit to less than to twice of nominal current, as shown in Fig. 7(d). According to Fig. 7(f), the current through the power electronic switches of phase A effectively is limited to twice of nominal value. So, the semiconductors operate in safe area operation during fault condition because of DLFCL module.

On the other hand, the time interval between the fault initiation and semiconductors failure is very smaller [31] than the time duration that is required to active the respective protection devices and disconnecting the IBDG unit from the utility. So, the severe *di*/*dt* which is initiated at the initial instants of the short circuit can damage the semiconductors. The rate of change of current through one of the inverter switches at the first moment of fault for both simulation conditions, with and without FCL in dc-link of the inverter, are compared with each other and are shown in Fig. 8. This figure shows that the presence of DLFCL module can suppress the severe *di*/*dt* at the initial instants of fault effectively.

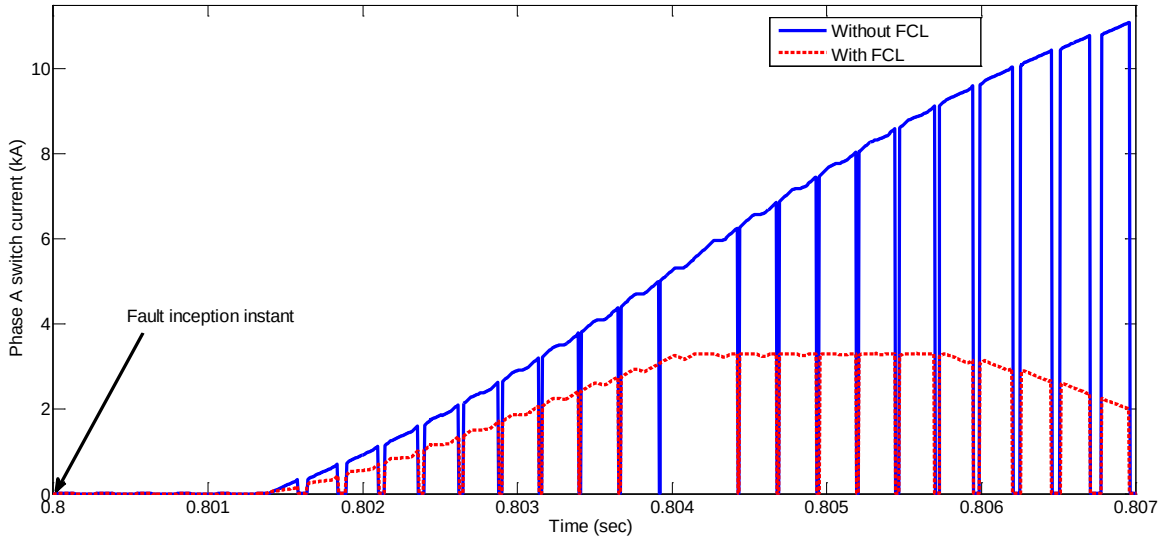

Fig. 8. The effectiveness of the proposed FRT scheme in suppressing the initial rate of change of current through one of the inverter power electronic switches after fault.

In order to establish relations between simulations results and analytical analysis, the time axis of dc reactor current in Fig. 7(c) is enlarged for three cases: before, during and after the fault and corresponding results are shown in Fig. 9. As illustrated in Fig. 9(a), before the fault dc reactor current is an almost ripple-

free dc current. After fault occurrence, the DLFCL automatically inserted in series with dc link of inverter consequently increases fault path impedance. So, the dc reactor current being to increase until fault is cleared (Fig. 9(b)). After fault clearance, the dc reactor current discharges to its pre-fault value after some milliseconds (Fig. 9(c)). So, the simulation results presented in Fig. 9 approved analytical analysis in part III (compare Fig. 9 with Fig. 2 and 3).

According to this analysis, by implementation of proposed FRT approach, the IBDG unit can stay connected to the utility grid during worst case short circuit faults so, it compliance the new grid codes requirements.

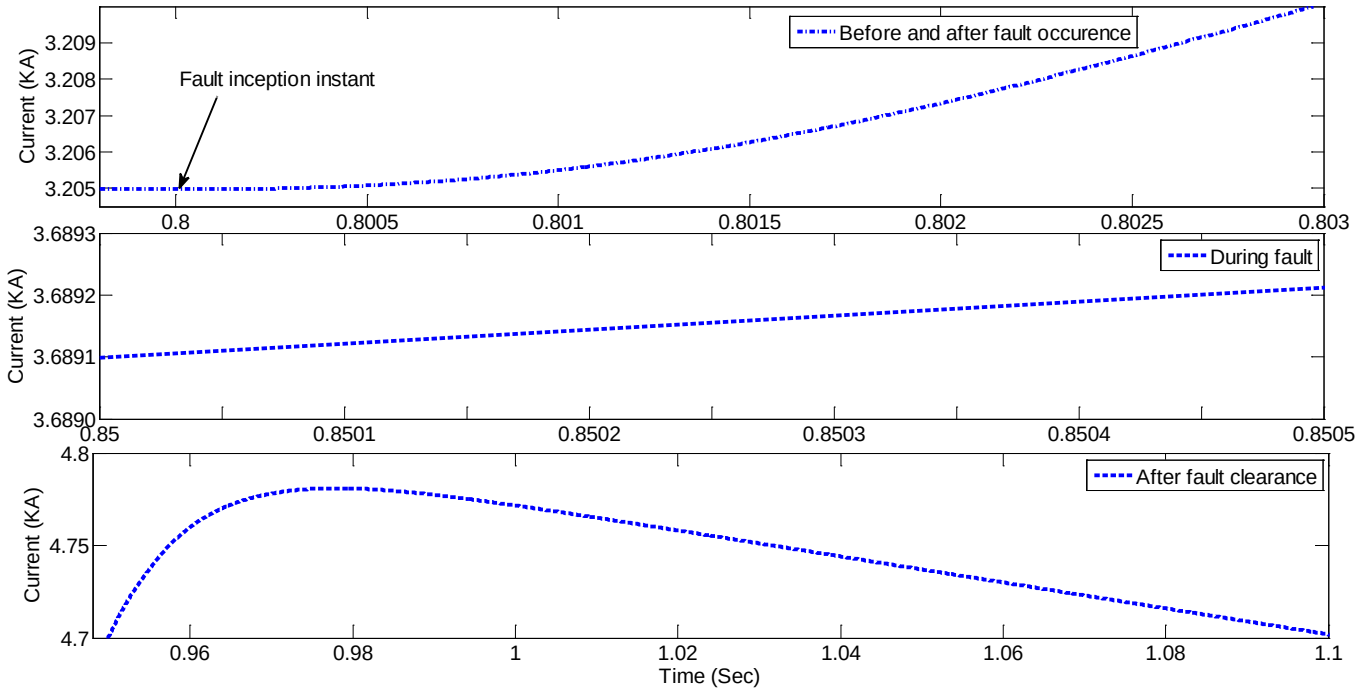

Fig. 9. The effectiveness of the proposed FRT scheme in suppressing the initial rate of change of current through one of the inverter power electronic switches after fault inception.

B. Asymmetrical faults

In this section, the performance of proposed approach is validated during asymmetrical grid faults. For this purpose two cases of asymmetrical fault including a LL fault between phases b and c, and a LG fault

on phase a are considered and are applied at point F1 in Fig. 6 at *t=0.8 s* with clearing time of 0.15 *s*. Simulation results including three phase output currents and current through switches of phase A when proposed FRT scheme is applied during LL and LG fault are shown in Fig. 10(a)-(d). It can be seen that for both fault situations, during the voltage dip, the output current of IBDG unit and current through the semiconductors effectively are limited to twice of nominal value in fault interval.

C. Repeated Transient Faults

Repeated transient faults (*i.e* lightning, storm, *etc.*) introduced major problems in overhead lines. The intent of this section is to highlight the performance of the proposed FRT scheme against repeated transient short circuit faults. For this purpose, at *t*=0.6 *s*, a repeated transient LG fault is applied at the end of the line 1 at point F2 in Fig. 6. Corresponding results provided in Fig. 11. As this figure shows, the proposed scheme can successfully limit the fault current of IBDG unit during such circumstances.

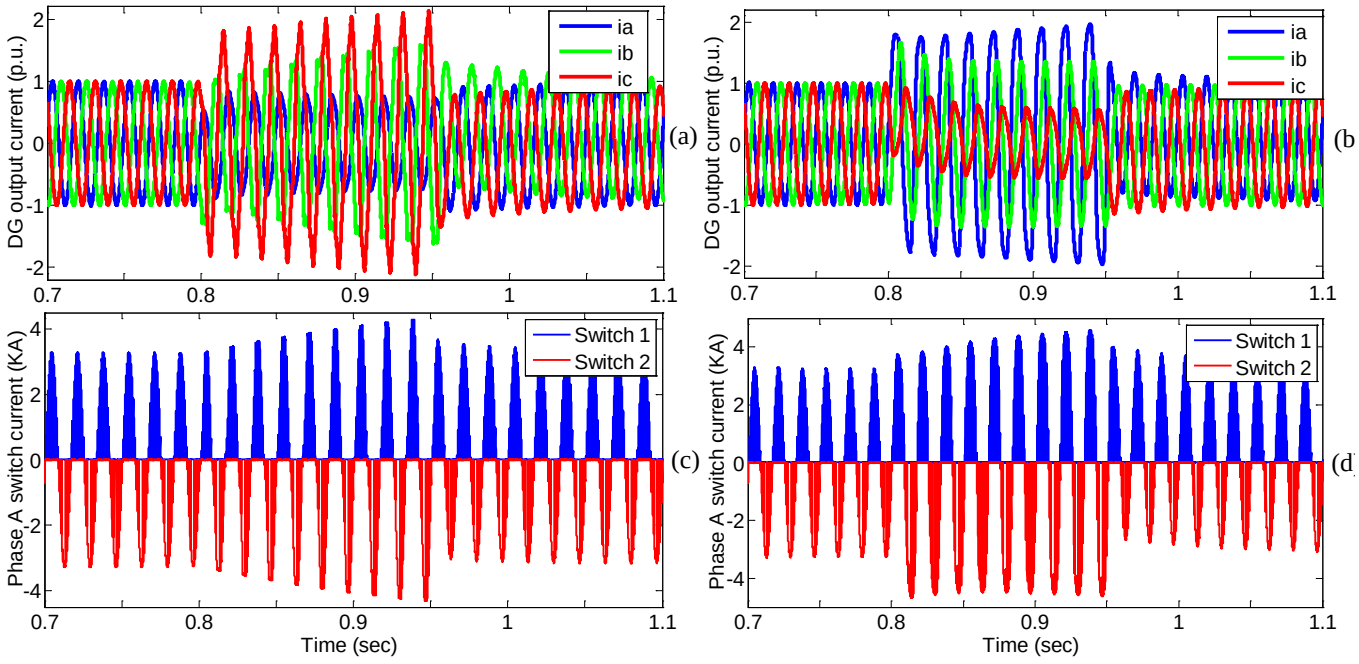

Fig. 10. Performance of the proposed FRT scheme during asymmetrical grid faults at point F1. Three-phase output current of IBDG unit during: (a) LL fault (b) LG fault. Phase A switch current of inverter during: (c) LL fault (d) LG fault.

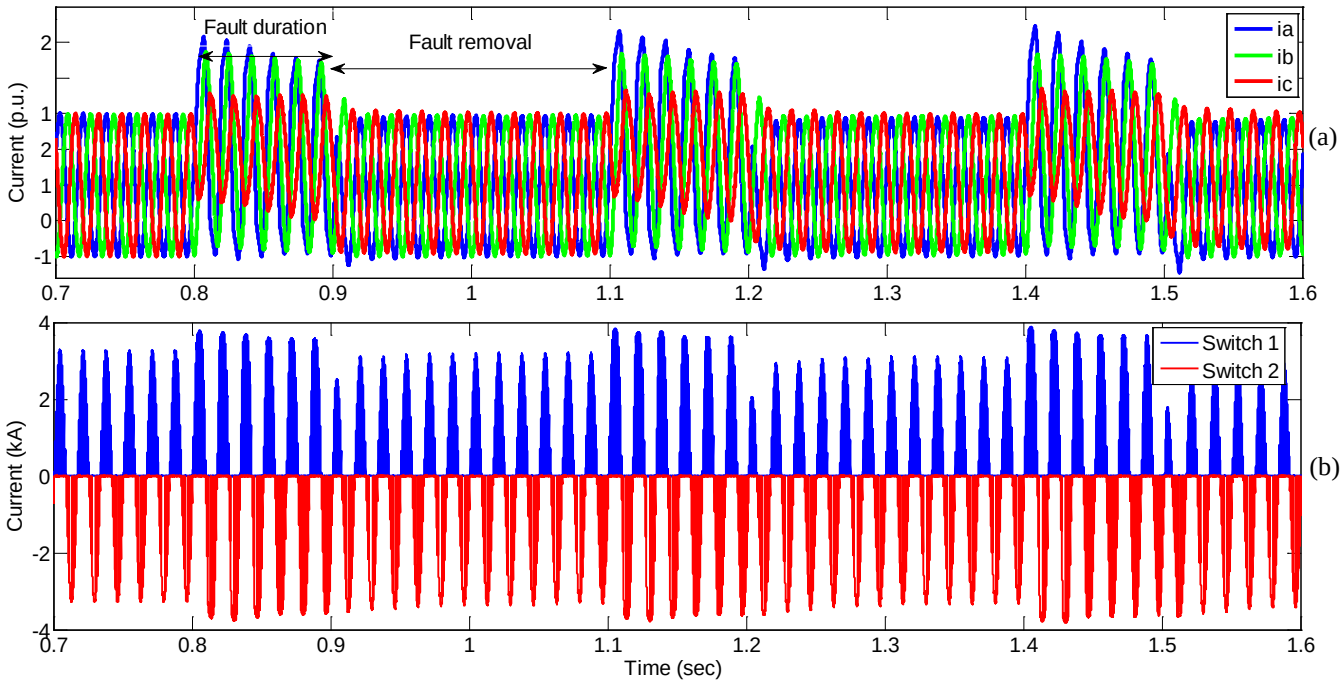

Fig. 11. Performance of the proposed FRT scheme during repeated transient faults at point F2. (a) Three-phase output current of IBDG unit. (b) Phase A switch current of inverter.

V. Experimental Results

Fig. 12 shows the single line diagram of experimental setup. A controllable DC source is connected in series with the proposed diode-bridge FCL and energises a Power Bright model ERP 400-12, 11-46 V dc to 220 V, 50 Hz ac inverter. The waveforms are captured using an Agilent Infiniivision (Model: DSO7034 A) oscilloscope. Fig. 13 shows experimental results without and with application of proposed FCL. To model a fault situation, the voltage of DC Source was programmable and increased stepwise from 16 to 22 (V). By this way, the dc link current abruptly increases which could modelling a fault condition. The results show that application of FCL has resulted in smoother current waveform in DC link (Idc) and output voltage from controllable DC source before and after fault modelling condition. The average current in DC link (Idc) after fault has decreased from 3.2 to 1.8 (A) by using DLFCL.

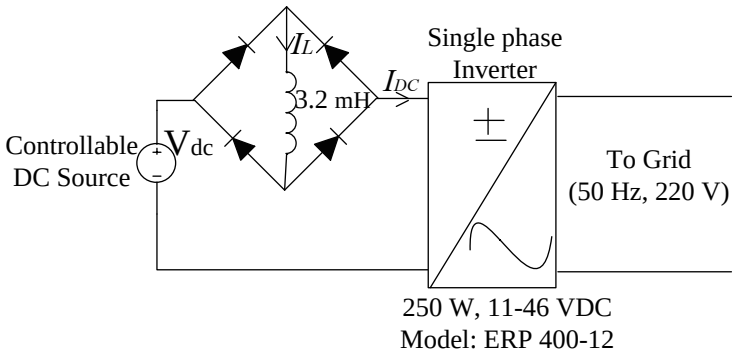

Fig. 12. The single line diagram of experimental setup.

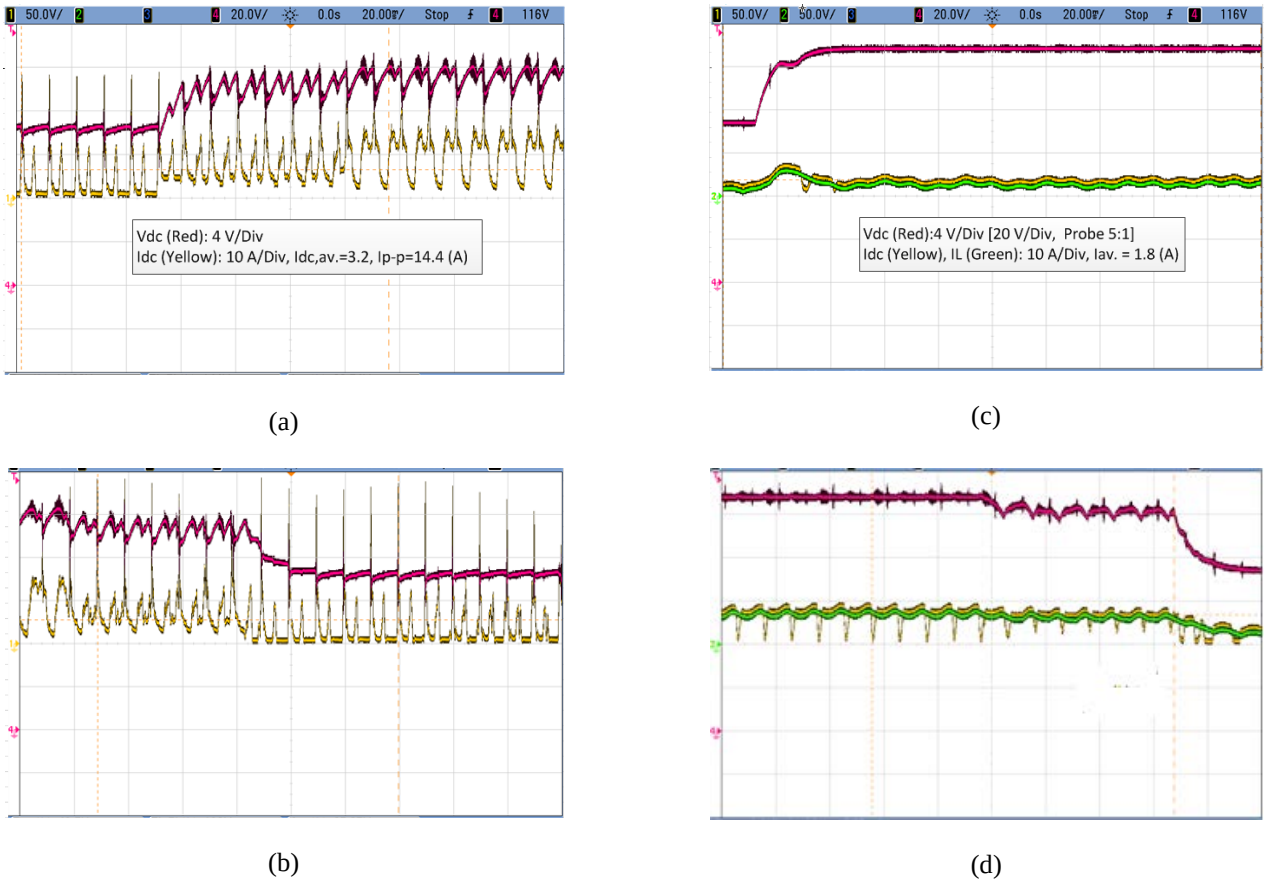

Fig. 13. Experimental results for DC link voltage change. Without FCL: (a) voltage raise, (b) voltage drop. With FCL: (c) voltage rise, (d) voltage drop.

VI. Conclusion

In this paper, a novel dc link FCL based FRT scheme proposed to improve the FRT capability in IBDGs units. The proposed approach provides several benefits which are listed below:

- The proposed scheme employs just one single set of FCL module in DC side of inverter. Therefore, it is more efficient than conventional approaches which need three similar sets of FCL modules at AC side of inverter.
- Since the DLFCL has simple configuration and does not need any control, measurement and gate deriving system. The proposed FRT solution can be simply implemented on VSI with least engineering cost.
- Compare with the other FRT methods, the proposed scheme is not affected by the deep of voltage dip. Moreover, by the present method continues operation can be realized for IBDG at zero grid voltage.
- Interface-inverter is controlled as a controlled voltage source in normal condition as well as fault condition. Moreover, no need to make use of superconductor inductor in DLFCL module leads to low initial cost of the proposed scheme.
- The proposed scheme has a reliable performance during various fault conditions. It has been evaluated under LLLG, LL, and LG short-circuit faults in PSCAD/EMTDC environment. Moreover, its efficiency is approved by a prototype setup.

So, the present scheme can be considered as an efficient method for fault current limitation of VSIs.

VII. REFERENCES

[1] W. Kramer, S. Chakraborty, B. Kroposki and H. Thomas.,Advanced power electronic interfaces for distributed energy systems part 1: systems and topologies, *National Renewable Energy Laboratory*, Golden, CO, NREL/TP-582-42672, 2008.

[2] Natthaphob Nimpitiwan, Gerald Thomas Heydt, Raja Ayyanar and Siddharth Suryanarayanan, Fault current contribution from synchronous machine and inverter based distributed generations, IEEE Transactions on Power Delivery 22 (2007) 634-641.

[3] A. Yazdani and R. Iravani. Voltage-sourced converters in power systems: modeling, control, and applications. Hoboken, NJ:Wiley, 2010.

[4] Amir H. Etmadi and Reza Iravani, Overcurrent and overload protection of directly voltage-controlled distributed resources in a microgrid, IEEE Transactions on Industrial Electronic 60 (2013) 5629-5638.

[5] Jeffrey M. Bloemink, and M. Reza Iravani, Control of a Multiple Source Microgrid With Built-in Islanding Detection and Current Limiting, IEEE Transactions on Power Delivery 27 (2012) 2122-2132.

[6] Fang Gao, and M. Reza Iravani, A control strategy for a distributed generation unit in grid-connected and autonomous modes of operation, IEEE Transactions on power Delivery 23 (2008) 850-859.

[7] J. Keller and B. Kroposki,"Understanding fault characteristics of inverter-based distributed energy resources, National Renewable Energy Laboratory, Golden, NREL/TP, 2010, 550-698.

[8] IEEE 1547-2003, IEEE Standard for Interconnecting Distributed Resources with Electric Power System, 2003.

[9] "E.ON Netz grid code—High and extra high voltage," E.ON Netz GmbH. Bayreuth, Germany [Online]. Available://www.eonnetz.com/Ressources/downloads/enenarhseng1.pdf.

[10] Technical guideline—Generating plants connected to the medium voltage network, Bundesverband der Energie-und Wasserwirtschaft e.V.(BDEW), Berlin, Germany, 2008.

[11] Junbum Kwon, Sunjae Yoon, Hyungjin Kim,and Sewan Choi, Fault ride-through control with voltage compensation capability for utility interactive inverter with critical load, in Proc. IEEE Power Electronics Conf., 2011, pp.3041-3047.

[12] Gazi Md. Saeedul Islam, Ahmed Al-Durra, S. M. Muyeen, and Junji Tamura, Low voltage ride-through capability enhancement of grid connected large scale photovoltaic system, in Proc. IEEE industrial electronic society Conference, 2011, PP. 884-889.

[13] Tom Loix, Thomas Wijnhoven, Geert Deconinck, Protection of micro-grids with a high penetration of inverter-coupled energy sources, in Proc. IEEE PES/CIGRE Symposium., 2009, pp.1-6.

[14] C. Plet, M. Graovac, T. Green, and R. Iravani, Fault response of grid connected inverter dominated networks, in Proc. IEEE Power and Energy Society General Meeting Conf,2010, pp. 1–8.

[15] Cornelis A. Plet, Maria Brucoli, John D.F. McDonald and Timothy C. Green, Fault models of inverter-interfaced distributed generators: experimental verification and application to fault analysis, in Proc. IEEE Power and Energy Society General Meeting Conf, 2011, pp. 1–8.

[16] Amin Hajizadeh, and Masoud Aliakbar Golkar, Control of hybrid fuel cell/battery distributed power generation system with voltage sag ride-through capability, 2nd IEEE International Conference on Power and Energy (PECon 08), December 1-3, 2008, Johor Baharu, Malaysia.

[17] JAntonio Camacho, Miguel Castilla, Jaume Mire, Juan C. Vasquez, and Eduardo Alarcon-Gallo, Flexible voltage support control for three-phase distributed generation inverters under grid fault, IEEE Transactions on Industrial Electronic 60 (2013) 1429–1441.

[18] Xuejun Pei, Yong Kang, Short-circuit fault protection strategy for high-power three-phase three-wire inverter, IEEE Transactions on Industrial Informatics 8 (2012) 545-553.

[19] Jaume Miret, Miguel Castilla, Antonio Camacho, Lu´ıs Garc´ıa de Vicu˜na, and Jos´e Matas, Control scheme for photovoltaic three-phase inverter to minimize peak currents during unbalanced grid-voltage sags, IEEE Transactions on Power Electronic 27 (2012) 4262-4271.

[20] Luis A. Mor´an, Ivar Pastorini, Juan Dixon, and Rogel Wallace, A fault protection scheme for series active power filters, IEEE Transactions on Power Electronic 14 (1999) 928-938.

[21] Mehrdad, Tarafdar Hagh, Mehdi Abapour, Nonsuperconducting fault current limiter with controlling the magnitude of fault currents, IEEE Transactions on Power Electronic 24 (2009) 613-619.

[22] M. Jafari, S. B. Naderi, M. Tarafdar Hagh, M. Abapour, and S. H. Hosseini, Voltage sag compensation of point of common coupling (PCC) using fault current limiter, IEEE Transactions on Power Delivery 26 (2011) 2638-2646.

[23] M. T. Hagh and M. Abapour, Nonsuperconducting fault current limiters, European Transactions on Electrical Power 19 (2008) 669-682.

[24] M. Abapour, S. H. Hosseini, and M. T. Hagh, Power quality improvement by use of a new topology of fault current limiter, in Proc. ECTICON, 2007, pp. 305–308.

[25] Taha Selim Ustun, Cagil Ozansoy, and Aladin Zayegh, A central microgrid protection system for networks with fault current limiters, in Proc.10th Int. Conf. Environment and Electrical Engineering (EEEIC), 2011, pp.1–4.

[26] Nathaniel Bottrell, Student, and Timothy C. Green, Comparison of current limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up, IEEE Transactions on Power Electronic 29 (2014) 3786–3797.

[27] Ali Keyhani and Muhammad Marwali. Smart Power Grids. Berlin: Springer, 2011, chap. 9.

[28] Ahmad F. Zobaa and Ramesh C. Bansal. Handbook of Renewable Energy Technology. London: World Scientific Publishing Co. Pte. Ltd, 2011, chap. 6.

[29] A.H. Kasem, E.F. El-Saadany, H.H. El-Tamaly, and M.A.A. Wahab, An improved fault ride-through strategy for doubly fed induction generator-based wind turbines, IET Renewable Power Generation 2 (2008) 201–214.

[30] Zhixin Miao, Alexander Domijan, Jr, and Lingling, Investigation of microgrids with both inverter-interfaced and direct ac-connected distributed energy resources, IEEE Trans on Power Delivery 26 (2011) 1634–1642.

[31] Bin Lu, and Santosh K. Sharma, A literature review of IGBT fault diagnostic and protection methods for power inverters, IEEE Transactions on Industrial Application 45 (2009) 1770–1777.