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Frequency-domain turbo equalisation with iterative impulsive noise mitigation for single-carrier power line communications

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Frequency-Domain Turbo Equalisation with Iterative Impulsive Noise Mitigation for Single-Carrier Power Line Communications

A thesis submitted in fulfilment of the requirements for award of the degree

Master of Engineering by Research

from

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by

Ying Liu

School of Electrical, Computer and Telecommunications Engineering

March 2015

Certification

I, Ying Liu, hereby declare that this thesis, submitted in partial fulfilment of the requirements for the award of Master of Engineering by Research, in the School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, is wholly my own work unless otherwise referenced or acknowledged. The document has not been submitted for qualifications at any other academic institution.

Signature: _____

Ying Liu

31 March 2015

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List of Abbreviations

8-PSK	8 phase-shift keying
APP	A posteriori probability
AWGN	Additive white Gaussian noise
BER	Bit-error rate
BPL	Broadband power line communications
BPSK	Binary phase-shift keying
EMC	Electromagnetic compatibility
FFT	Fast Fourier transformation
i.i.d	Independent and identically distributed
IFFT	Inverse fast Fourier transformation
IN	Impulsive noise
IN-EC	Impulsive noise estimation and cancellation
ISI	Inter-symbol interference
LMMSE	Linear minimum mean square error
LS	Least square
MAP	Maximum a posteriori probability
OFDM	Orthogonal Frequency Division Multiplexing
PAPR	Peak-to-average power ratio
PDF	Probability density function
PLC	Power line communications
QPSK	Quadrature phase-shift keying
SC-FDE	Single carrier modulation with frequency domain equalisation
SC-FDTE	Single carrier modulation with frequency domain turbo equalisation
SIR	Signal-to-impulsive noise ratio
SNR	Signal-to-noise ratio

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Abstract

Power line communications (PLC) operates by transmitting modulated data signal through the electrical power transmission and distribution cables. Nowadays, PLC has been recognised as a promising alternative communication technology due to the universal existence of power lines, which saves human and material resources from establishing additional communication infrastructures. However, power lines were originally devised to deliver electrical power rather than signal data. Thus, signal transmitted through PLC channel suffers from severe inter-symbol interference (ISI) and strong impulsive noise (IN), degrading the reliability of data transmission. Except for ISI and IN, in order to avoid interference to other communication systems, electromagnetic compatibility constraints regulate a limit to the signal power transmitted in the power line systems.

To date, multicarrier modulation, e.g., orthogonal frequency division multiplexing (OFDM), based PLC systems have been advocated to combat ISI. Besides, several IN mitigation approaches have been introduced to OFDM to eliminate the detrimental impact of IN. However, the inherent large peak-to-average power ratio (PAPR) of the OFDM signals makes IN detection difficult, and the OFDM based PLC system may not be the best choice under hostile PLC channels.

In comparison with OFDM, this thesis proposes to use single carrier modulation due to its low PAPR. Specifically, a novel iterative receiver, i.e., single carrier modulation with frequency-domain turbo equalisation (SC-FDTE) coupled with an iterative IN estimation and cancellation (IN-EC) module, is developed for PLC. The frequency domain equaliser is implemented based on linear minimum mean square error (LMMSE) algorithm, which significantly reduces computational complexity compared with the time-domain equalisation. Moreover, powerful turbo (iterative) equalisation is used to handle severe ISI. The iterative IN-EC module is designed to combat the impact of IN, which includes the components of IN location detection, IN estimation and IN cancellation. For the IN location detection component, two IN detection methods are developed to be implemented: the sorting based method and the thresholding based method. After IN estimation and cancellation, the IN-EC provides an 'IN free' (residual IN may still exist) received signal to the equaliser. It is worth highlighting that the novel receiver facilitates an iterative operation between the equaliser and the IN-EC. Hence, both of the equaliser and IN-EC are able to enhance their performance iteratively, thereby leading to a significant improvement in system performance.

Simulation results demonstrate that, compared with the conventional non-iterative OFDM and single-carrier frequency-domain equalisation (SC-FDE) based PLC systems, which both combined with non-iterative IN mitigation approaches, PLC system with the proposed iterative receiver can achieve a remarkable performance gain, i.e., 20 dB as shown in Chapter 3, under a typical 4-path reference PLC channel at a bit error rate of 10^{-5} .

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Chapter 1 Introduction

Power Line Communications (PLC) allows transmitting data signal through the electrical power transmission and distribution cables, aka, power lines [1, 2]. It is also known as Power Line Carrier, Power Line Telecommunications or Power Line Networking [2]. This thesis refers to the term 'Power Line Communications (PLC)'.

Electrical power lines are usually classified into the high ($>100\text{kV}$), medium ($1 \sim 100\text{kV}$) and low ($< 1\text{kV}$) voltage networks, with respectively increasing communications difficulties [2]. Therefore, PLC technology consists of the corresponding high, medium and low voltage PLC. The main thrust of the developments in PLC has been focusing on the low voltage network, which has the geographically widest spread [3]. The two-fold markets of the low voltage PLC shown in

Fig. 1.1 and Fig. 1.2 are: to the home, or 'last-mile' access; and in the home, or 'last-inch' access [3-5]. From Fig. 1.1, it can be seen that the 'last-mile' PLC delivers signal through the local low voltage power line cables between different residences. For example, the information of meter reading and security cameras can be transmitted to the community public security center through this 'last-mile' PLC system. In the 'last-inch' PLC network, which is shown in Fig. 1.2, information signal is able to be delivered among different rooms via the in-home power cables. Therefore, various appliances are connected whilst accessible to the global internet, which is a significant first step for future smart home projects.

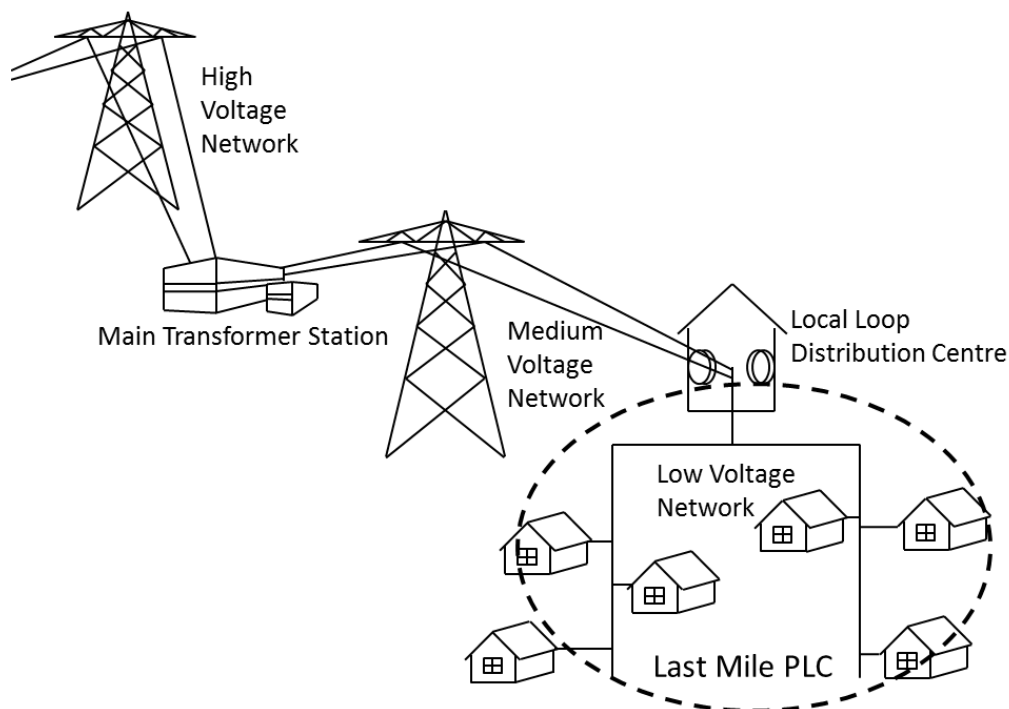


Figure 1.1 'Last-mile' PLC network.

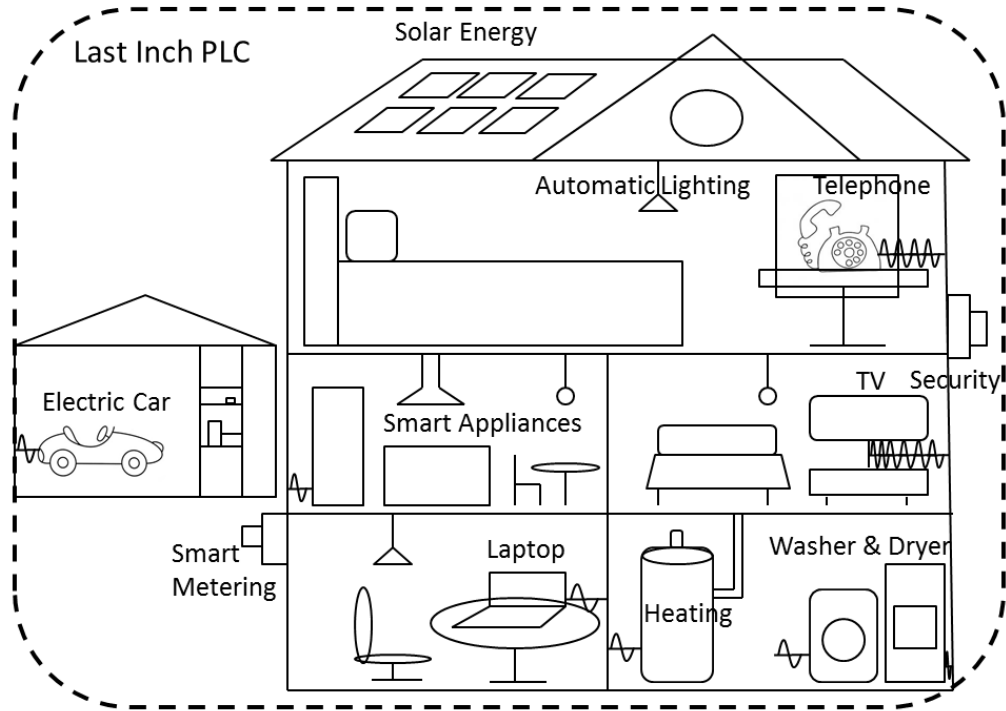


Figure 1.2 'Last-inch' PLC network.

1.1 Background

Early works of PLC can be traced back to the beginning of the twentieth century, with applications involving analog voice communications over high voltage long distance power lines [2]. Other applications during this period are remote monitoring and power line equipment protection [2-4]. In the middle age of the twentieth century, the applications in high voltage PLC became matured and researchers transferred their attention to medium voltage and low voltage PLC networks. In this period, digital communications techniques were introduced to PLC to support smart tele-metering and tele-controlling [4]. However, the development of early PLC was only established

on the applications embracing the national power plants. Besides, the data transmission rate was very low, e.g., few hundreds bits per second [4].

In the past few decades, novel applications except for the grid binding ones were developed. The broadband PLC (BPL) technology was first proposed in 1997 [2]. BPL system aimed to realize high-speed communications for low voltage outdoor systems and indoor systems, e.g., high-speed internet, video on demand, video monitoring and digital home automation. Moreover, BPL technology can be applied to the existing wireline (cable) and wireless (WiFi/optical) communications, which makes data transmission further convenient for users. Another important driver for PLC technology is the load management for Smart Grid [1, 2], i.e., the selectivity of switching off free device such as water heater at time of peak demand. This load management application helps electric suppliers to balance the demands in the power system and acts as saving incentives for house owners. In the future, powerful PLC technologies are desired for various applications ranging from transportation platforms (vehicle) applications [6] to home/community automation [7]. As an example for PLC in-vehicle application, consider a vehicle with tractor-trailer, information from the trailer (brake heating, tire pressure, internal temperatures, etc.) could be transmitted via the electric wires to the driver to alert him any specific conditions within the trailer. This could improve road safety.

1.1.1 Advantages of PLC

Nowadays, PLC draws itself an attraction as the alternative medium for modern

communications due to its marked superiorities. Firstly, electric power lines are already settled in essentially all buildings and residences. The universal existence of power line facilities naturally exhibits a convenient and simple communications approach for analog and data signal [1, 2]. In addition, it saves human and material resources from building additional transmission infrastructures. The second advantage of PLC is the ubiquitous power points inside modern constructions, which makes electric appliances easily connected to the broadband internet. At the same time, data transmissions between various electrical devices become convenient. Except for the aforementioned advantages, compared with PLC, the extensively used Asymmetrical Digital Subscriber Lines technology suffers from the drawback of small number of connection points. Besides, the wireless communications technology is affected by terrible congestion and interference in the unlicensed bands [5].

1.1.2 Challenging Issues of PLC

However, like all other technologies, PLC also faces its own set of obstacles. The power line system was designed to carry large current under high voltages alternating at 50 or 60 Hertz. Thus, it differs in topology, structure, and physical properties from conventional 'point-to-point' medias such as twisted pair, coaxial, or fiber-optic cables [5]. Therefore, the wirings in place to supply electrical power to, and within, homes and offices lead to a harsh, noisy and nonlinear environment for data transmissions. Specifically, the main challenges in PLC are multipath propagation and impulsive noise (IN), which significantly degrade the reliability of data communications [1-5]. Another

challenging issue in PLC is the electromagnetic compatibility, especially for BPL in-home technology. The following subsections present the details of these challenges.

1.1.2.1 Multipath Propagation

Multipath propagation phenomenon is caused by the specific topology of power line. It has a 'tree like' topology with multiple branches between the transmitter and the receiver. Therefore, signal symbols transmitted in power line suffer from reflections at these branches, which lead to asynchronous arrivals of different signal symbols at the receiver. As a result, PLC exhibits multipath propagation similar as the wireless communications [2-5], which yields severe ISI for data transmission. Details of the mathematical models of the power line channel are discussed in Chapter 2.

1.1.2.2 Impulsive Noise

Another challenging issue in PLC is the presence of strong, time-varying and non-white noise. Such noise is generated by electrical devices connected to the power line, and by external noise and interference coupled to the power grid via radiation or conduction. From past works [1-3, 8, 9], the noise in power line can be classified into two categories: background noise and IN. The IN is time-varying with random occurrence and duration from microseconds to milliseconds. Its amplitude is relatively large, which may exceed the background noise by more than 50 dB. Therefore, Due to the existence of IN, data symbols transmitted in PLC channel are affected by bit or burst errors, which severely degrade the BER performance of the whole communications system. Mathematical

models of the IN are shown in Chapter 2.

1.1.2.3 Electromagnetic Compatibility

Electromagnetic interference refers to a phenomenon that occurs when an electronic device is affected by an external source due to either electromagnetic induction or electromagnetic radiation [2, 10, 11]. The power lines may emit severe electromagnetic interference due to large power signal transmitted inside, which impacts the operations of other radio receivers. Therefore, power spectrum density limits have been proposed as the EMC constraints for PLC system, in order to adjust the operations of other radio frequency based communication systems [2, 10, 12].

1.2 Research Motivations

To date, multicarrier modulation, e.g., OFDM, based PLC system has been advocated to address the multipath channel condition. Besides, several IN mitigation approaches have been introduced to OFDM to eliminate the detrimental impact of IN [13-17]. However, OFDM signal has a large PAPR due to the superposition of signals from several sub-carriers. As a result, OFDM signal symbols with large amplitudes may be incorrectly identified as IN in the IN mitigation module, which makes IN detection difficult. In addition, the OFDM based PLC system delivers bad performance under hostile PLC channels [18, 19]. On the other hand, time-domain equalisation achieves optimal signal detection for ISI channel [20]. However, the large number of channel

taps makes the computational complexity a major concern. Due to the low complexity and low PAPR, other works focus on the single-carrier frequency-domain equalization (SC-FDE) based PLC system [19, 21]. However, these works neglect the IN in PLC channel and the non-iterative frequency domain equalisation is not a powerful approach to combat ISI.

The objective of this thesis is to combat both ISI and IN in PLC. Moreover, it aims to achieve a distinct BER performance under low SNR to meet the EMC constraints. In comparison with OFDM, this thesis proposes to use single carrier modulation due to the low PAPR. In addition, a powerful iterative receiver is developed for PLC, which combines frequency domain turbo equalisation with an iterative IN estimation and cancellation (IN-EC) module.

1.3 Research Contributions

Compared with other conventional strategies for PLC, this thesis makes the following contributions:

1. A novel iterative receiver is designed for PLC, which enables iterative ISI and IN eliminations. The basis of the proposed receiver is the frequency domain turbo equalisation, which can improve signal detection iteratively using the soft message passing loop between the equaliser and the decoder. In addition, an iterative IN mitigation module named IN-EC is coupled with the turbo

equalisation in order to achieve a new iterative operation between the equaliser and the IN-EC. Therefore, by using these two soft message flowing loops, both of the equaliser and the IN-EC are able to enhance their performance iteratively. Consequently, the system performance can be significantly improved. Detailed algorithms and simulation results of the proposed iterative receiver for PLC are shown in Chapter 3.

2. This thesis proposes the novel IN mitigation module, i.e., the iterative IN-EC. It consists of three components: IN location detection, IN estimation and IN cancellation. By considering the fact that the 'interference' of data signal may cause incorrect IN detection from the received signal, the IN-EC first attempts to do signal cancellation from the received signal before the IN location detection. In addition, two IN location detection methods, namely, the sorting based method and the thresholding based method, are designed to be implemented in the IN-EC to localise IN from the residual signal. The sorting based method sorts the amplitude of residual signals in decreasing order, and assumes the signal symbols with large amplitudes containing IN. on the other hand, in the thresholding based method, a novel optimal threshold determination is proposed according to the signal detection theory. Details of the proposed IN-EC algorithm as well as the two IN localisation methods are presented in Chapter 3.

1.4 Thesis Organization

The rest of this thesis is structured as follows:

Chapter 2 reviews the past works. Firstly, mathematical models of the PLC channel as well as IN models are introduced. After that, this chapter discusses previous approaches to mitigate ISI, namely, the time-domain equalization and OFDM. The wireless communications approach, i.e., SC-FDE, is also reviewed because PLC channel has similar multipath propagation characteristic with wireless communications. In addition, Chapter 2 compares the conventional IN mitigation approaches, i.e., the receiver front-end IN mitigation scheme and the equaliser back-end IN mitigation scheme. At the end of Chapter 2, the outstanding issues in previous PLC research are concluded.

Chapter 3 shows the structure and algorithm of the proposed receiver for PLC. Firstly, the received signal model is presented. This chapter then discusses the algorithm of frequency-domain turbo equalisation, where the turbo equaliser is based on LMMSE algorithm. After that, the detailed procedure of the novel IN mitigation module is introduced. Finally, Chapter 3 presents simulation results and analysis.

Chapter 4 concludes this thesis and puts forward future works.

Chapter 2 Literature Review

2.1 PLC Channel Models

Recall that, PLC channel is frequency selective due to the multipath propagation (see Chapter 1). Generally, its channel response is affected by the cable layout, the types of appliances and the selection of sockets connecting electrical devices. In previous literature on the PLC channel models, two types of approaches are widely used to obtain the PLC channel's frequency response, which are the bottom-up approach and the top-down approach.

The bottom-up approach is based on characterising the power line's physical structures, such as lines, branches and loads [22-26]. Moreover, the parameters of the PLC channel based on the bottom-up approach can be obtained by calculating the

properties of these physical structures. In 2004, Meng et al. [22] proposed a power line channel model based on the transmission line theory, in which, the power line is modelled as a two conductor transmission line. Later, Galli and Banwell [23] proposed a more accurate power line channel model based on multi-conductor transmission line theory and modal decomposition. Briefly, PLC channel models with deterministic parameters can be established using the bottom-up approach. These models clearly present the relationship between the power line network's physical behavior and the model parameters, which is accurate and flexible. In addition, PLC channel models based on the bottom-up approach do not require the measurement of a real PLC channel frequency response. However, they rely on the detailed knowledge of the PLC network, which is usually impossible to obtain exactly in practice, to set up transmission matrices and scattering matrices. In addition, the computational complexity required to calculate the model parameters grows with the number of discontinuities, which may be extremely high for some in-home PLC scenarios due to numerous sockets and applications [27].

As opposite to the bottom-up approach, top-down approach considers the PLC channel as a black box [27, 28], in which, the multipath propagation can be expressed using a parametric echo model. In the top-down approach, measured frequency response of a real PLC channel is required and the model parameters can be derived from fitting the results of measured frequency response. In 1999, Philipps [28] proposed a time-domain echo model where the signals are received via N paths. Each

path can be represented by a time delayed impulsive response and a phase shift. Later, an adapted frequency-domain model was proposed by Zimmermann and Dostert [27]. This model not only considered the multipath propagation, but also introduced the signal attenuation due to the length of the propagation path. In the past decade, Zimmermann and Dostert's multipath model has been verified in numerous experiments, showing excellent agreement with measured values. Furthermore, Tonello [29] proposed statistical distributions for the parameters in Zimmermann and Dostert's multipath model to obtain a random channel generator. As compared with the bottom-up approach, top-down approach requires less computational resources and is easier implemented with computer simulation. However, the accuracy of the channel model parameters based on the top-down approach is restricted by measurements.

Note that, the main objective of this thesis is to design a receiver for PLC system with effective ISI and IN mitigation approaches to improve data transmission reliability. Therefore, the easily implemented top-down approach based Zimmermann and Dostert's [27] multipath power line channel model is used in this thesis to generate the PLC channel matrix. This is because it provides a good trade-off between the computational complexity and the straightforward expression of the PLC channel's multipath effect. The remaining of this section shows the details of Zimmermann and Dostert's model.

The frequency response of Zimmermann and Dostert's [27] N -path PLC channel is

derived by combining the weighting factor g_i , the attenuation portion $e^{-(a_0+a_1 \cdot f^k) \cdot d_i}$ and the delay portion $e^{-j2\pi f \tau_i}$. The simplified model of the channel frequency response is given by:

$$H(f) = \sum_{i=1}^N \underbrace{g_i}_{\text{weighting factor}} \cdot \underbrace{e^{-(a_0+a_1 \cdot f^k) \cdot d_i}}_{\text{attenuation portion}} \cdot \underbrace{e^{-j2\pi f \tau_i}}_{\text{delay portion}} \quad (2.1)$$

Each path has a weighting factor g_i , which is assumed between zero and one. This is because the load of a parallel connection of two or more cables leading to the resultant impedance lowers than the original feeding cable's impedance. In Equation (2.1), the attenuation is the function of the frequency and the length of each path, which yields:

$$A(f, d_i) = e^{-(a_0+a_1 \cdot f^k) \cdot d_i}, \quad (2.2)$$

where a_0 and a_1 represent the attenuation parameters, k is the exponent of the attenuation factor and d_i represents the length of the i th path. Typically, the parameters a_0 , a_1 and k are derived from the measured transfer function. In addition, the delay τ_i in Equation (2.1) is calculated as follows:

$$\tau_i = \frac{d_i \sqrt{\epsilon_r}}{c_0}, \quad (2.3)$$

where ϵ_r denotes the dielectric constant of the insulating material, and c_0 is the

speed of light.

Given the fact that the received signal is the superposition of signals transmitted through different paths. A path with longer length provides a smaller weighting factor and a higher attenuation to the transmitted signal. Therefore, signal transmitted through a longer path contributes less to the overall signal at the receiver. In practise, researchers only consider the dominant reflections, typically $N = 3 \sim 5$. In this thesis, the parameters of a 4-path reference PLC channel [27] are used to constitute the PLC matrix. Detailed simulation of the PLC channel will be presented in Chapter 3.

2.2 PLC Noise Models

Given that the noise in power line can be classified into two categories: background noise, \mathbf{w} , and IN, \mathbf{i} [8, 9]. The total additive noise is the sum of the background noise and the IN as follows:

$$\mathbf{n} = \mathbf{w} + \mathbf{i}. \quad (2.4)$$

Background noise in the PLC channel experiences small deviations with time and is usually modelled as additive complex white Gaussian noise with a PDF of $w_k \sim CN(0, \sigma_w^2)$ [5, 8, 9, 30]. On the other hand, IN in the PLC channel is a non-stationary, binary-state sequence of impulses with random amplitudes and random occurrence. Therefore, an IN sequence is usually modelled as the product of a

binary-state random sequence and a Gaussian noise process [13, 17, 30-35]. A well-known noise model for the PLC channel is the Middleton's class A model [34, 36], in which the PDF of the total additive noise is given by:

$$p(n) = \sum_{k=0}^{\infty} P_k \cdot \frac{1}{\sqrt{2\pi} \cdot \sigma_k} \cdot \exp\left(\frac{-n^2}{2 \cdot \sigma_k^2}\right) \quad (2.5)$$

$$P_k = \frac{e^{-A} \cdot A^k}{k!} \quad (2.6)$$

$$\sigma_k^2 = \sigma_i^2 \cdot \frac{k}{A} + \sigma_w^2, \quad (2.7)$$

where σ_i^2 and σ_w^2 represent the variances of IN and background noise respectively, A denotes the impulse index. The Middleton's class A noise model can be considered as the superposition of an infinite number of parallel Gaussian processes, each with different variances and generated with the Poisson distribution P_k . Thus, this model is also called the Poisson-Gaussian mixture noise model.

The authors in [30] propose an IN model called Bernoulli-Gaussian model, which provides a straightforward physical characteristic of IN with a simple mathematical representation. The Bernoulli-Gaussian is the product of a real Bernoulli process and a complex Gaussian process as follows:

$$i_k = b_k g_k, \quad k = 0, 1, \dots, K-1, \quad (2.8)$$

where $\{b_k\}$ denotes an i.i.d sequence of zeroes and ones with the probability when $b_k = 1$ is p . g_k is a complex white Gaussian process with mean zero and variance σ_i^2 . For a better understanding, the Bernoulli–Gaussian IN can be taken as a physically scenario that each signal symbol being hit independently by an impulse. This impulse has a form corresponding to a complex white Gaussian process with an occurrence probability of p . Furthermore, in the Bernoulli–Gaussian model, the fraction of the variances between the IN and the background noise is represented as $\mu = \sigma_i^2/\sigma_w^2$.

Other works, i.e., [8, 31], use a two-state hidden Markov model to indicate the binary-state sequence in IN models. The on and off states in the Markov loop represent the cases when IN occurs or does not occur.

2.3 ISI Mitigation

As discussed in Chapter 1, a major challenging issue in the research of PLC is the ISI caused by multipath propagation. Generally, two widely used approaches have been proposed to effectively cope with the ISI: time-domain equalisation and OFDM. In the time-domain equalisation, optimal signal detection can be achieved to enable perfect estimates of the transmitted signal symbols. However, the heavily dispersive power line channel leads to large computational complexity, which is a major concern [20]. On the contrary, OFDM-based PLC system has been advocated to cope with the significantly delayed PLC channel by using the low complexity frequency-domain equaliser [14-16,

33, 37-40]. However, the inherent large PAPR of OFDM symbols make IN detection difficult, especially under high SIR conditions [18, 41-43]. Following subsections present the details of these conventional ISI mitigation approaches.

2.3.1 Time-domain Equalisation

Fig. 2.1 demonstrates the transmitter block diagram (Fig. 2.1(a)) with two receiver structures, which are the conventional separate equalisation and decoding (Fig. 2.1(b)) as well as the turbo equalisation [20] (Fig. 2.1(c)).

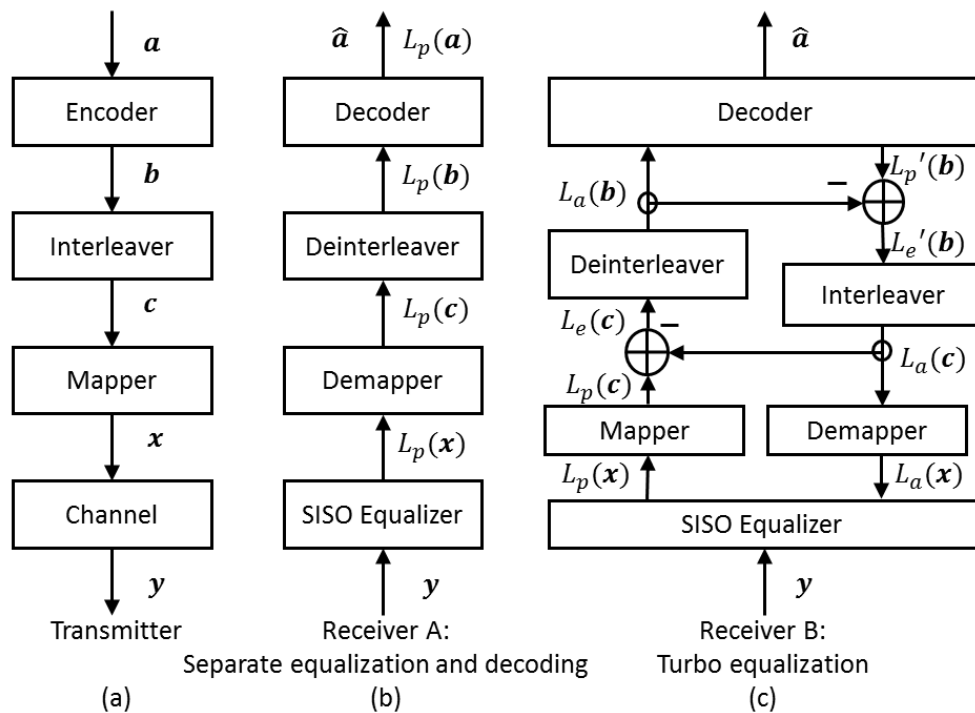


Figure 2.1 (a) Transmitter configuration with two receiver inducing equalisations: (b) the separate equalisation and decoding and (c) the turbo equalisation.

The conventional receiver carries out equalisation and decoding separately, which has been used in most practical communication systems. Here, the SISO equaliser block denotes the soft-input soft-output equaliser, which aims to make soft estimates of the transmitted symbols according to the received observations. It avoids using hard decision because this may destroy the possibility that a symbol might take on any particular value [20]. Furthermore, to achieve the minimum probability of error between the original transmitted symbol \mathbf{x} and its estimate $\hat{\mathbf{x}}$, a well-known method is to calculate an appropriate value for $\hat{\mathbf{x}}$ that can maximise the a posteriori probability (APP) [20]. Therefore, in Fig. 2.1 (b), the soft information $L_p(\mathbf{x})$ generated from the SISO equaliser denotes the log-likelihood ratios of the APP of \mathbf{x} , which can be represented by the following equation when BPSK mapping is used:

$$L_p(\mathbf{x}) = L(\mathbf{x}|\mathbf{y}) = \ln \frac{P(\mathbf{x} = +1|\mathbf{y})}{P(\mathbf{x} = -1|\mathbf{y})}. \quad (2.9)$$

Then, $L_p(\mathbf{x})$ passes through the de-mapper, de-interleaver and decoder to get the a posteriori information $L_p(\mathbf{c})$, $L_p(\mathbf{b})$ and $L_p(\mathbf{a})$ corresponding to the interleaved bit sequence \mathbf{c} , the coded bit sequence \mathbf{b} as well as the original information bit sequence \mathbf{a} at the transmitter. Finally, the hard decision $\hat{\mathbf{a}}$ is obtained as following:

$$\hat{a}_k = \begin{cases} 0, & L_p(a_k) \geq 0 \\ 1, & L_p(a_k) < 0 \end{cases}, \quad k = 0, 1, \dots, K - 1. \quad (2.10)$$

As shown in Fig. 2.1(c), differs from the separate equalisation and decoding, soft information generated from the equaliser first flows to the decoder, passing the demapper and the deinterleaver. Once the decoder processes the soft information, it generates its own soft information which indicates the relative likelihood of each original transmitted bit [20]. This soft information is then fed back to the interleaver, the mapper as well as the equaliser, to create a soft message passing loop between the equaliser and the decoder. Therefore, the a priori information input to the equaliser can be iteratively updated by using the iterative loop. After passing the demapper, the a posteriori information generated from the equaliser can be considered as a sum of the intrinsic information $L_a(\mathbf{c})$ and the extrinsic information $L_e(\mathbf{c})$ shown as follows:

$$L_p(\mathbf{c}) = \ln \frac{\sum_{\forall \mathbf{c}: c_i=0} p(\mathbf{y}|\mathbf{c}) \prod_{j=0}^{L-1} P(c_j)}{\sum_{\forall \mathbf{c}: c_i=1} p(\mathbf{y}|\mathbf{c}) \prod_{j=0}^{K-1} P(c_j)} = L_e(\mathbf{c}) + L_a(\mathbf{c}). \quad (2.11)$$

Feeding back the intrinsic information leads to positive feedback [44]. As a result, only the extrinsic information is exchanged in the iteration. As shown in Fig. 2.1 (c), $L_e(\mathbf{c})$ flows from the equaliser to the decoder. Similarly, $L_p'(\mathbf{b})$ generated from the decoder first subtracts the intrinsic information $L_a(\mathbf{b})$, resulting in the extrinsic information $L_e'(\mathbf{b})$ to be fed back to the equaliser.

Compared with the conventional separate equalisation and decoding receiver, a significant advantage is gained by performing the equalisation and decoding iteratively. By processing the a priori information delivered from the decoder, the equaliser

achieves a more reliable soft information, which improves the decoder to enhance the estimate of each information bit. Therefore, with the increase of iteration, the performance of signal detection can be significantly improved, showing effectiveness in ISI elimination.

In literature, two algorithms have been widely used to compute the APP for the time-domain soft-input soft-output equaliser, which are the trellis-based equalisation [20, 45] and the linear filtering based equalisation [46, 47].

2.3.1.1 Trellis-based Maximum a Posteriori Probability Equalisation

The trellis-based MAP method, which is also known as the forward/backward algorithm or BCJR algorithm, was proposed and named after by Bahl, Cocke, Jelinek and Raviv in 1974 [45]. It aims to estimate each transmitted symbol to a possible value that can maximise the APP according to the received observations. Fig. 2.2 and Fig. 2.3 show an example of a 3-tap reference channel and its corresponding trellis representation, respectively. The tapped delay line model is given by:

$$v_k = \sum_{l=0}^L h_l x_{k-l}, \quad k = 0, 1, \dots, K-1, \quad (2.12)$$

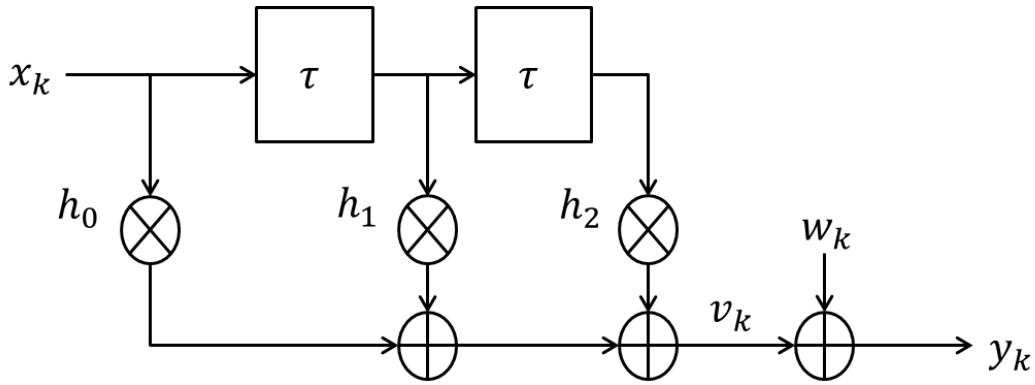


Figure 2.2 Tapped delay line circuit of a 3-tap reference channel: $h_0 = 0.407$, $h_1 = 0.815$ and $h_2 = 0.407$.

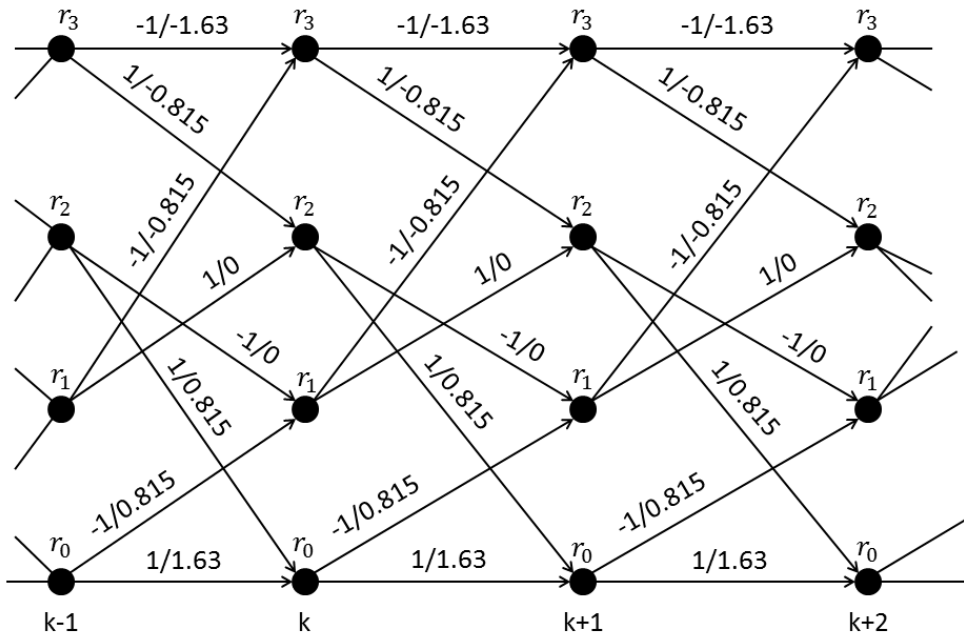


Figure 2.3 Trellis representation of the channel in Figure 2.2.

which contains L ($L = 2$) delay elements. K denotes the length of the transmitted symbol. Assume BPSK mapping is used, and that $S = \{r_0, r_1, r_2, r_3\}$ represents the set of possible states where $r_0 = (1,1)$, $r_1 = (-1,1)$, $r_2 = (1,-1)$ and $r_3 = (-1,-1)$.

The transitions from a state $s_k = r_i$ at time k to a state $s_{k+1} = r_j$ at time $k + 1$ are labelled with input/output pair $x_{i,j}/v_{i,j}$ in Fig. 2.3 [20].

The APP can be computed using the trellis representation via the joint distribution $p(s_k, s_{k+1}, \mathbf{y})$, which is the probability that the transmitted sequence path in the trellis contains the branch $(i, j, x_{i,j}, v_{i,j})$ at the time instance k . Consequently, the joint distribution can be represented as:

$$\begin{aligned} p(s_k, s_{k+1}, \mathbf{y}) &= p(\mathbf{y})P(s_k, s_{k+1}|\mathbf{y}) \\ &= p(s_k, s_{k+1}, (y_1, \dots, y_{k-1}), y_k, (y_{k+1}, \dots, y_N)), \end{aligned} \quad (2.13)$$

which can be decomposed as:

$$\begin{aligned} p(s_k, s_{k+1}, \mathbf{y}) \\ &= \overbrace{p(s_k, y_1, \dots, y_{k-1})}^{\alpha_k(s_k)} \cdot \overbrace{p(s_{k+1}, y_k | s_k)}^{\gamma_k(s_k, s_{k+1})} \cdot \overbrace{p(y_{k+1}, \dots, y_N | s_{k+1})}^{\beta_{k+1}(s_{k+1})}. \end{aligned} \quad (2.14)$$

In Equation (2.14), $\alpha_k(s_k)$ represents the probability that contains all paths in the trellis arrived at state s_k . $\gamma_k(s_k, s_{k+1})$ denotes the probability for the transition from s_k to s_{k+1} with symbol y_k . $\beta_{k+1}(s_{k+1})$ represents the probability that contains all possible paths from state s_{k+1} to s_N . By using the trellis, these three elements can be calculated as follows:

$$\gamma_k(r_i, r_j) = \begin{cases} P(x_k = x_{i,j}) \cdot p(y_k | v_k = v_{i,j}), & \text{if } (i, j) \in \text{trellis paths} \\ 0, & \text{if } (i, j) \notin \text{trellis paths} \end{cases} \quad (2.15)$$

$$\alpha_k(s) = \sum_{\forall s' \in S} \alpha_{k-1}(s') \gamma_{k-1}(s', s) \quad (2.16)$$

$$\beta_k(s) = \sum_{\forall s' \in S} \beta_{k+1}(s') \gamma_k(s', s). \quad (2.17)$$

Then the log-likelihood ratio of the a posteriori information in Equation (2.11) can be calculated by:

$$\begin{aligned} L_p(c_i) &= \ln \frac{P(c_i = 0 | \mathbf{y})}{P(c_i = 1 | \mathbf{y})} = \ln \frac{P(x_k = +1 | \mathbf{y})}{P(x_k = -1 | \mathbf{y})} \\ &= \ln \frac{\sum_{\forall (i,j) \in \text{Trellis}; x_{i,j}=+1} [\alpha_k(\gamma_i) \cdot p(y_k | v_k = v_{i,j}) \cdot \beta_{k+1}(\gamma_j)]}{\sum_{\forall (i,j) \in \text{Trellis}; x_{i,j}=-1} [\alpha_k(\gamma_i) \cdot p(y_k | v_k = v_{i,j}) \cdot \beta_{k+1}(\gamma_j)]}. \end{aligned} \quad (2.18)$$

In summary, the trellis-based MAP equalisation is able to achieve optimal equalisation. This is because it considers all of the possible channel states given the random input, i.e., +1 or -1, into the tap delay line at time k . However, the computational complexity of the trellis-based approach is determined by the number of trellis states, which grows exponentially with the number of channel taps L . In addition, when higher-order signal alphabet is used, the computational complexity would be exacerbated. For example, there will be 4^L states in the trellis if QPSK mapping is used.

2.3.1.2 Linear Filtering based Minimum Mean Square Error Equalisation

In contrast with the trellis-based method, the linear filtering-based approach performs only a linear filtering operation on the received signal. This algorithm was proposed by Tüchler et al. [46]. Considering the system shown in Fig. 2.2, the received signal can be represented as:

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{w}, \quad (2.19)$$

where \mathbf{H} is an $N \times K$ complex channel matrix, \mathbf{x} is a length- K complex random vector with PDF $\mathcal{CN}(\mathbf{x}; \mathbf{m}, \mathbf{v})$, and \mathbf{w} is a length- N complex random vector with PDF $\mathcal{CN}(\mathbf{w}; 0, \sigma_w^2 \mathbf{I})$ that is independent of \mathbf{x} . Therefore, the linear estimation of the transmitted symbol by using the observation \mathbf{y} is given by:

$$\hat{x}_k = \mathbf{a}_k^H \mathbf{y}_k + b_k, \quad k = 0, 1, \dots, K-1. \quad (2.20)$$

The aim of the minimum mean square error estimation is to compute an estimate of the transmitted symbol, which can minimise the mean squared error between the original transmitted signal and its estimate. Therefore, by computing the mean squared error $E(|x_k - \hat{x}_k|^2)$ and minimising it, \mathbf{a}_k and b_k can be achieved via the following equations:

$$\mathbf{a}_k = \text{Cov}(\mathbf{y}_k, \mathbf{y}_k)^{-1} \text{Cov}(\mathbf{y}_k, x_k) \quad (2.21)$$

and
$$b_k = E(x_k) - \mathbf{a}_k^H E(\mathbf{y}_k). \quad (2.22)$$

By using the mathematical equations for the mean and covariance, one can compute the mean μ_k and variance σ_k^2 of the estimate \hat{x}_k . Let the code bit sequence c_i be divided into bit subsequence $s_{k,j}$ with length J , and each subsequence is mapped to a symbol x_k . The extrinsic log-likelihood ratio for each code bit c_i can be computed according to the following mathematical expression proposed by Tüchler et al.'s [46]:

$$\begin{aligned} L_e(c_i) &= \ln \frac{P(c_i = 0 | \hat{x}_k)}{P(c_i = 1 | \hat{x}_k)} - L_a(c_i) \\ &= \ln \frac{\sum_{\forall s_k: s_{k,j}=0} p(\hat{x}_k | c_i = s_{k,j}) \prod_{\forall j': j' \neq j} P(c_i = s_{k,i'})}{\sum_{\forall s_k: s_{k,j}=1} p(\hat{x}_k | c_i = s_{k,j}) \prod_{\forall j': j' \neq j} P(c_i = s_{k,i'})} \\ &= \ln \frac{\sum_{\forall s_k: s_{k,j}=0} \exp\left(-\frac{|\hat{x}_k - \mu_k|^2}{\sigma_k^2} + \frac{\sum_{\forall j': j' \neq j} \tilde{s}_{k,j'} L_a(c_i)}{2}\right)}{\sum_{\forall s_k: s_{k,j}=1} \exp\left(-\frac{|\hat{x}_k - \mu_k|^2}{\sigma_k^2} + \frac{\sum_{\forall j': j' \neq j} \tilde{s}_{k,j'} L_a(c_i)}{2}\right)}, \end{aligned} \quad (2.23)$$

where the term $L_a(c_i) = \ln\left(\frac{P(c_i=0)}{P(c_i=1)}\right)$ denotes the a priori information of each code bit.

The value of $\tilde{s}_{k,j}$ depends on the value of $s_{k,j}$ as follows:

$$\tilde{s}_{k,i} = \begin{cases} +1, & s_{k,j} = 0 \\ -1, & s_{k,j} = 1 \end{cases}. \quad (2.24)$$

In summary, the linear filtering based equalisation algorithm provides a sub-optimal signal estimation performance with a lower computational complexity compared with the trellis-based estimation algorithm [20, 46-48]. However, its computational complexity is still a significant concern [49], especially for channels with large number of taps, i.e., the power line channel considered in this thesis.

2.3.2 OFDM

Nowadays, OFDM has been recognised as a popular scheme for broadband digital communication, which is used in many applications such as digital television and audio broadcasting, digital subscriber line internet access, wireless networks, power line networks and 4G mobile communications [50].

A simple block diagram of an OFDM-based PLC system is shown in Fig. 2.4. A cyclic prefix, denoted as CP, is inserted at the transmitter after the inverse fast Fourier transform; i.e., the IFFT block. At the receiver, it removes cyclic prefix at the CP removal block before the fast Fourier transform; i.e., the FFT block. Here, the cyclic prefix refers to the repetition of the end of each symbol block x . It serves with two purposes. The first one is as a guard interval to eliminate ISI from the previous symbol. The second one is to allow the linear convolution of a frequency-selective multipath channel to be modelled as circular convolution, which reduces the computational complexity for frequency-domain equalisation. This is because the circular convolution at time-domain can be converted into scalar multiplication at frequency-domain.

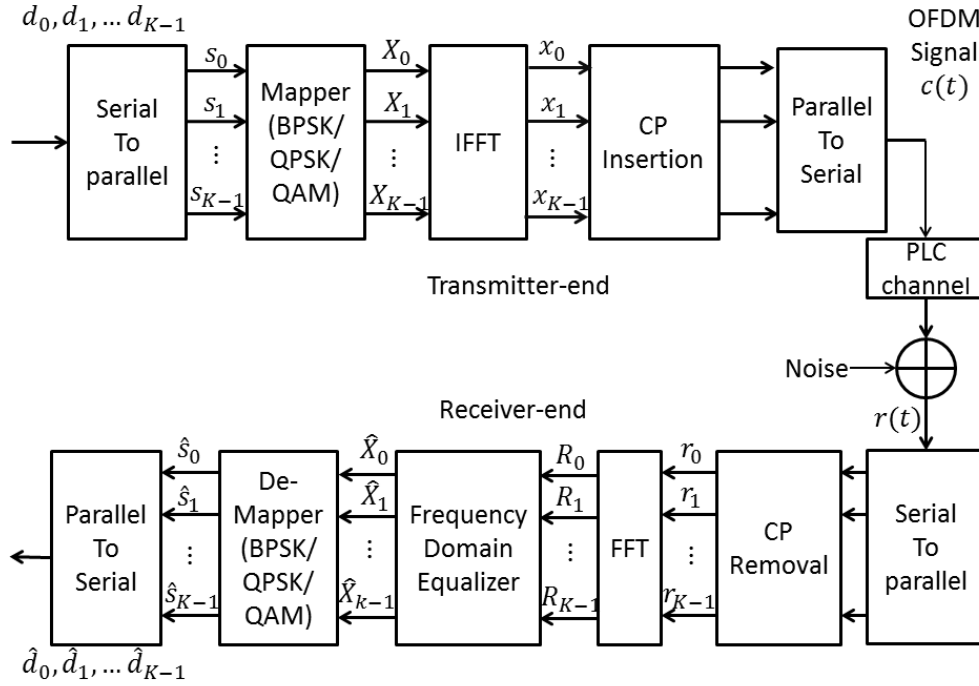


Figure 2.4 Block diagram of OFDM-based PLC system

In summary, OFDM-based PLC system can easily cope with severe channel conditions without inducing complicated time-domain equalisation. Therefore, OFDM-based PLC approaches are at the centre of the upcoming standardisation process led by the Institute of Electrical and Electronics Engineers [2]. However, the signal superposition of these orthogonal subcarriers in OFDM leads to a large PAPR, which makes IN detection difficult [18, 41-43]. Moreover, the OFDM-based PLC systems are sensitive to carrier frequency offsets [41].

2.4 Single-Carrier Frequency-Domain Equalisation

Due to the EMC constraints, the large PAPR of OFDM becomes a major concern for the

PLC system. However, the heavily dispersive power line channel makes the conventional single carrier modulation with time-domain equalisation a bad choice due to the prohibitive complexity. To this end, SC-FDE has been proposed as an interesting and complementary alternative to OFDM [41]. It combines the single carrier modulation with frequency-domain equalisation to achieve low computational complexity whilst avoiding the large PAPR. In literature, SC-FDE based wireless communications has been widely investigated from the problem of channel estimation to ISI mitigation issues [51-53]. The similarity of multipath propagation phenomenon between PLC and wireless communications makes SC-FDE a great potential in combating the ISI in PLC [19, 21].

The block diagram of SC-FDE based PLC system is shown in Fig. 2.5. This system differs from the OFDM-based system (see Fig. 2.4) that no IFFT is performed at the transmitter. After the symbol mapper, cyclic prefix is inserted at the beginning of each symbol block and the resulting data sequence is transmitted serially. The main superiority of SC-FDE is listed as follows. Firstly, similar as the OFDM system, cyclic prefix is inserted and removed at the CP insertion and CP removal blocks respectively. Therefore, SC-FDE based communication systems provide comparable computational complexity to that of OFDM. The second superiority is that the performance of the SC-FDE-based PLC system is similar to, or even better than, the OFDM-based PLC systems under different scenarios with or without coding [18, 42]. Furthermore, SC-FDE avoids the inherent drawbacks associated with OFDM as discussed in Section

2.3.2, especially the large PAPR.

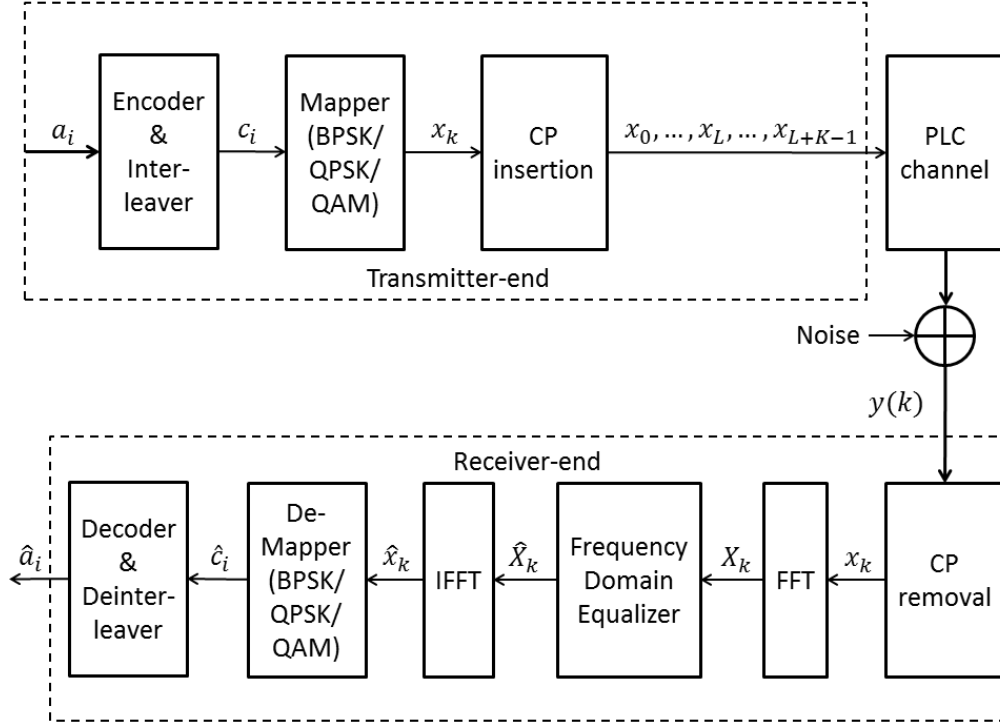


Figure 2.5 Block diagram of SC-FDE-based PLC system.

Ng and Chauh [19] compared the performance of the SC-FDE-based PLC system with the OFDM-based PLC system under realistic PLC channels. In addition, two frequency-domain equalisation algorithms have been compared: zero forcing and minimum mean square error criteria. Their results overturned the usual belief that OFDM signalling is more resistant to multipath fading than classical single-carrier transmission. Furthermore, La-Gatta et al. [21] first addressed the presence of IN in SC-FDE based PLC system. They used low density parity check code as the coding algorithm to combat IN and compared SC-FDE with conventional single-carrier decision

feedback equalisation. Simulation results show that when IN is introduced, coded SC-FDE with minimum mean square error equalisation based system offers a distinct performance gain over single-carrier decision feedback equalisation. However, although different channel coding approaches are used, there is still 6 dB to 7 dB BER performance degradation due to the presence of IN.

In summary, the SC-FDE-based PLC system has a lower PAPR than OFDM-based PLC system. Therefore, it provides a better ability to meet the EMC constraints in PLC and makes IN to be easily detected at time-domain. In addition, it has been proved that SC-FDE-based system outperforms OFDM in terms of BER under specific reference PLC channels. However, the challenge is that the frequency-domain equalisation based on conventional separate equalisation and decoding does not represent an optimal solution to signal detection over ISI channels. Moreover, a powerful IN mitigation approach is needed to cope with the 6-7 dB performance degradation due to the impact of IN.

2.5 IN Mitigation

Apart from ISI, IN is another challenging issue that dramatically affects the data transmission performance in PLC. In order to cope with the detrimental impact of IN and improve the reliability of data communication under practical PLC systems, IN mitigation modules are desirable. However, most of the IN mitigation approaches in

literature are established on the OFDM based PLC system. Therefore, this section introduces two popular IN mitigation methods for the OFDM based PLC system: the receiver front-end IN processor and the equaliser backend IN processor.

2.5.1 Receiver Front-End IN Processor

The diagram of the receiver front-end IN mitigation approach is shown in Fig. 2.6, which introduces an IN pre-processor block to the receiver front-end. Thus, the received signal y_k first passes through the IN pre-processor to mitigate IN and get the new received signal y'_k . The objective of the IN pre-processor shown in Fig. 2.6 is to first detect whether a received signal symbol is affected by IN; i.e., exceeding a threshold, by considering the fact that an IN symbol has relatively large amplitude. It then combats the detrimental effect of IN by applying nonlinear processing to the IN affected symbols.

In 2008, Zhidkov [14] proposed and compared three popular receiver front-end IN mitigation methods for OFDM receivers, namely, clipping nonlinearity, blanking nonlinearity, and joint clipping and blanking nonlinearity. Specifically, the clipping nonlinearity clips the IN affected received symbols to specific values by performing nonlinear processing to the original IN affected symbols. The blanking nonlinearity directly blanks the received symbols to zero once their amplitudes exceed the blanking threshold. On the other hand, joint clipping and blanking nonlinearity combines both clipping and blanking processes. In which, a received symbol will be blanked to zero if its amplitude is higher than the blanking threshold. If a received symbol's amplitude is

higher than the clipping but lower than the blanking threshold, it will be clipped to a predetermined value. Otherwise, it remains in the signal with no changes.

Mathematically, these three schemes are shown as follows:

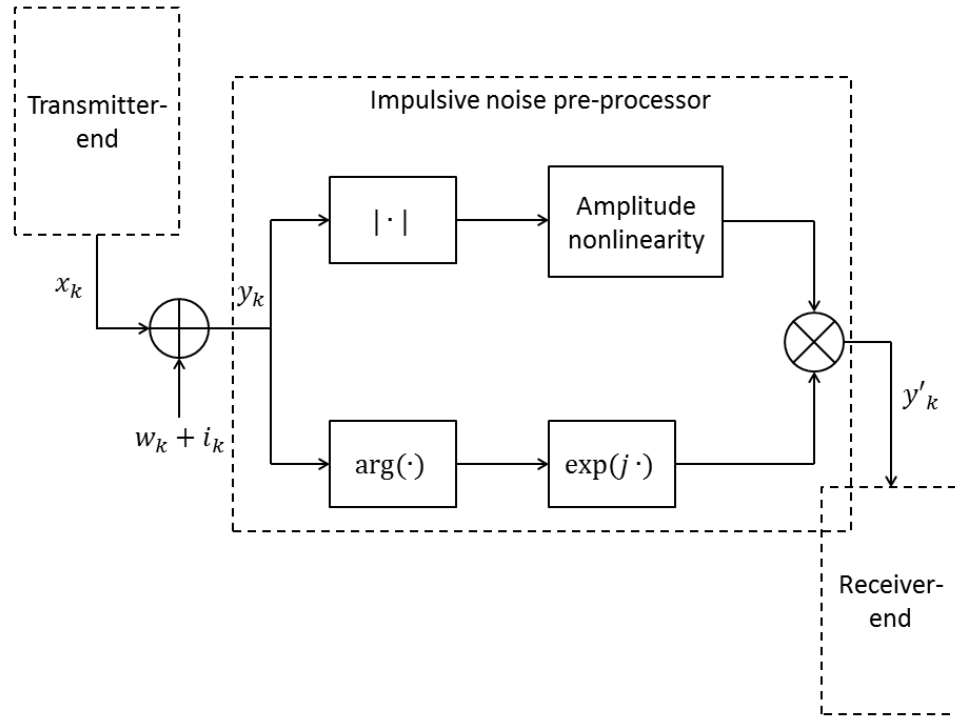


Figure 2.6 Block diagram of receiver front-end IN mitigation processor.

a) clipping nonlinearity

$$y'_k = \begin{cases} y_k, & |y_k| \leq T_c \\ T_c e^{j\arg(y_k)}, & |y_k| > T_c \end{cases} \quad k = 0, 1, \dots, K-1 \quad (2.25)$$

b) blanking nonlinearity

$$y'_k = \begin{cases} y_k, & |y_k| \leq T_b \\ 0, & |y_k| > T_b \end{cases}, \quad k = 0, 1, \dots, K-1 \quad (2.26)$$

c) joint clipping and blanking nonlinearity

$$y'_k = \begin{cases} y_k, & |y_k| \leq T_c \\ T_c e^{j\arg(y_k)}, & T_c < |y_k| \leq T_b \\ 0, & |y_k| > T_b \end{cases}, \quad k = 0, 1, \dots, K-1. \quad (2.27)$$

In these equations, T_c and T_b denote the clipping threshold and the blanking threshold, respectively. K is the length of the signal transmission block. Zhidkov [14] used a hunting method to derive the optimal clipping and blanking thresholds, which are obtained by minimising the symbol error rate. In the case of joint clipping and blanking nonlinearity, the blanking threshold is chosen as 1.4 times the clipping threshold. The numerical results show that under a weak IN environment, clipping nonlinearity outperforms blanking nonlinearity slightly [14]. In practise, when IN is strong, blanking nonlinearity outperforms clipping nonlinearity. The author concludes that the best solution is the joint clipping and blanking nonlinearity because it combines the advantages of both the clipping and the blanking schemes.

To achieve the closed-form expression of the optimal clipping threshold, Ndo et al. proposed a novel approach in 2010 [54]. In this work, the optimal threshold determination is based on achieving the trade-off between the false alarm and the good detection of IN. They evaluated and compared two threshold determination criteria: weighted combination and Siegert. A key limitation is that they only

considered the baseband communications, i.e., real-valued transmitted signal, which makes the approach inappropriate for QPSK or quadrature amplitude mapping.

In summary, IN mitigation schemes based on receiver front-end nonlinearity pre-processors have simple system structures and mathematical representations, which make them easy to be implemented. However, signal symbols with high amplitude will cause incorrect triggering of the clipping or blanking processor, which may generate IN detection errors and lead to dramatic performance degradation.

2.5.2 Equaliser Back-End IN Processor

In comparison with the above IN mitigation solutions, which simply perform thresholding to the whole received signal, Zhidkov [13] proposed a novel adaptive IN mitigation scheme for OFDM-based communication system. The basic block diagram is given in Fig. 2.7.

In this block diagram, after FFT, the frequency-domain received signal \mathbf{Y} can be expressed as follows:

$$\mathbf{Y} = \mathbf{H}\mathbf{X} + \mathbf{W} + \mathbf{U}, \quad (2.28)$$

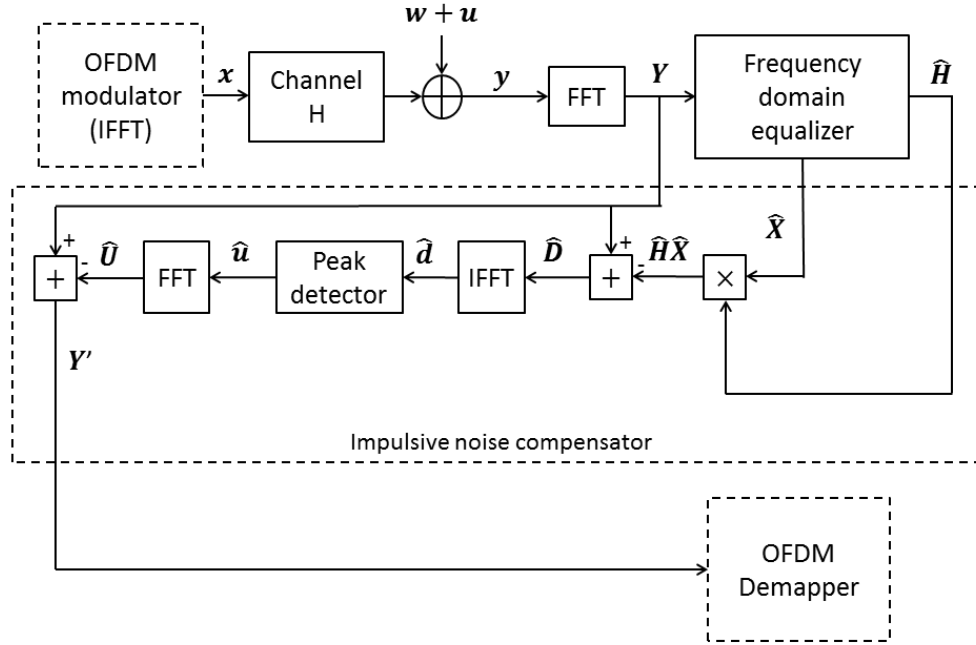


Figure 2.7 Block diagram of equaliser back-end IN mitigation processor.

where H denotes the channel matrix, X represents the frequency-domain transmitted signal, W and U denote the frequency-domain background noise and the frequency-domain IN respectively. The aim of the equaliser back-end IN processor is to estimate the frequency-domain IN, i.e., U , and subtract it from the frequency-domain received signal Y . Therefore, it first performs signal cancellation, i.e., $\hat{H}\hat{X}$ is first subtracted from Y , thus, the estimate of the total additive frequency-domain noise, denoted as \hat{D} , is obtained. Then, by using the IFFT, one can get the total time domain noise \hat{d} , which contains the background noise as well as the IN. The time domain IN, i.e., \hat{u} , is then detected and estimated using the peak detector block shown in Fig. 2.6. This block processes an algorithm that is similar to the

blanking method, specifically:

$$\hat{\sigma}^2 = \frac{1}{N} \sum_{k=0}^{N-1} |\hat{d}_k|^2 \quad (2.29)$$

and

$$\hat{u}_k = \begin{cases} \hat{d}_k, & \text{if } |\hat{d}_k|^2 > C \hat{\sigma}^2 \\ 0, & \text{otherwise} \end{cases}, \quad k = 0, 1, \dots, K-1, \quad (2.30)$$

where C is the threshold value according to the small probability of false detection.

Afterwards, IN is eliminated by subtracting $\hat{\mathbf{U}}$ from \mathbf{Y} .

In summary, the equaliser back-end IN mitigation method avoids the phenomenon of incorrect thresholding triggers by first subtracting the effect of data signal from the received signal. However, PLC system is under a strong IN environment, which makes the estimate of signal $\hat{\mathbf{X}}$ generated via the frequency-domain equaliser to be unreliable due to the spreading of frequency-domain IN symbols. This then causes estimate errors of the IN, thereby degrades the system performance.

2.6 Summary

In summary, this thesis addresses the following outstanding issues remaining in PLC.

2.6.1 Outstanding Issues

1. Time-domain equalisation achieves optimal signal detection for ISI channel.

However, the heavily dispersive power line channel makes the computational complexity a severe concern.

2. OFDM can be used to combat the ISI in PLC with providing low complexity frequency-domain equalisation. However, major concerns are that the inherent large PAPR of OFDM symbols leads to difficulties in IN detection, and the OFDM based PLC system may not be a powerful approach to achieve good performance under hostile PLC channels. Furthermore, due to the limitation of signal power transmitted in power line according to the EMS constraints, a challenging problem is to develop a robust method that can achieve considerable BER performance under low SNR.
3. By applying low complexity frequency-domain equalisation to the single carrier modulation, SC-FDE provides low PAPR as promising alternative to OFDM. However, conventional non-iterative frequency-domain equalisation is not an optimal solution to cope with the ISI channel. In previous works considering SC-FDE based PLC system, although different coding algorithms are used, there is still 6 dB to 7 dB performance degradation due to the occurrence of IN.
4. In the literature of receive front-end IN processor, signal symbols would have interference to IN detection. On the other hand, the equaliser back-end IN processor avoids this drawback by first subtracting the contribution signal from the received signal. However, this method achieves bad performance when the estimate of the transmitted signal is not reliable.

In order to address the aforementioned outstanding issues, this thesis proposes to use single carrier modulation because its low PAPR. In addition, a powerful iterative receiver is designed for PLC. This novel receiver introduces an iterative IN mitigation module to the frequency-domain turbo equalisation, which supplies information to each other. Therefore, with the increase of iteration, both of the turbo equalisation and the IN mitigation can be improved, thereby ISI and IN can be mitigated iteratively. Next chapter presents the detailed structure, mathematical models and simulation results of the proposed approach.

Chapter 3 Proposed Iterative Receiver Structure, Algorithm and Performance

This chapter presents the algorithms as well as the simulation results of the proposed iterative receiver, which is designed for time invariant frequency selective power line channel with the presence of impulsive noise. The transceiver block diagram is shown in Fig. 3.1. Similar to the transmitter of an SC-FDE scheme (discussed in Chapter 2), after mapping, cyclic prefix is inserted to the transmitted signal x_k . Then the signal passes through the power line channel, which is affected by ISI and IN (contained in n_k). Details of the transmitted and received signal models are given in Section 3.1. After that, cyclic prefix is removed and the received signal y_k is input to the proposed iterative receiver. At the receiver, firstly, IN-EC estimates and cancels IN at time-domain. Then, the frequency-domain turbo equalisation processes the ‘IN free’ received

symbols and generates an estimate for each transmitted symbol. By processing the soft information delivered from the equaliser, the decoder generates its own estimate for each encoded bit. This soft information enables the improvement of the signal detection through the soft message passing loop inside turbo equalisation. Moreover, it is fed back to the IN-EC module to achieve a more accurate IN estimation. Section 3.2 outlines the details of the proposed SC-FDTE based PLC system, coupled with iterative IN mitigation. The algorithm of the novel IN-EC module is proposed in Section 3.3. Section 3.4 presents and analyses the simulation results. Finally, this chapter is summarised in Section 3.5.

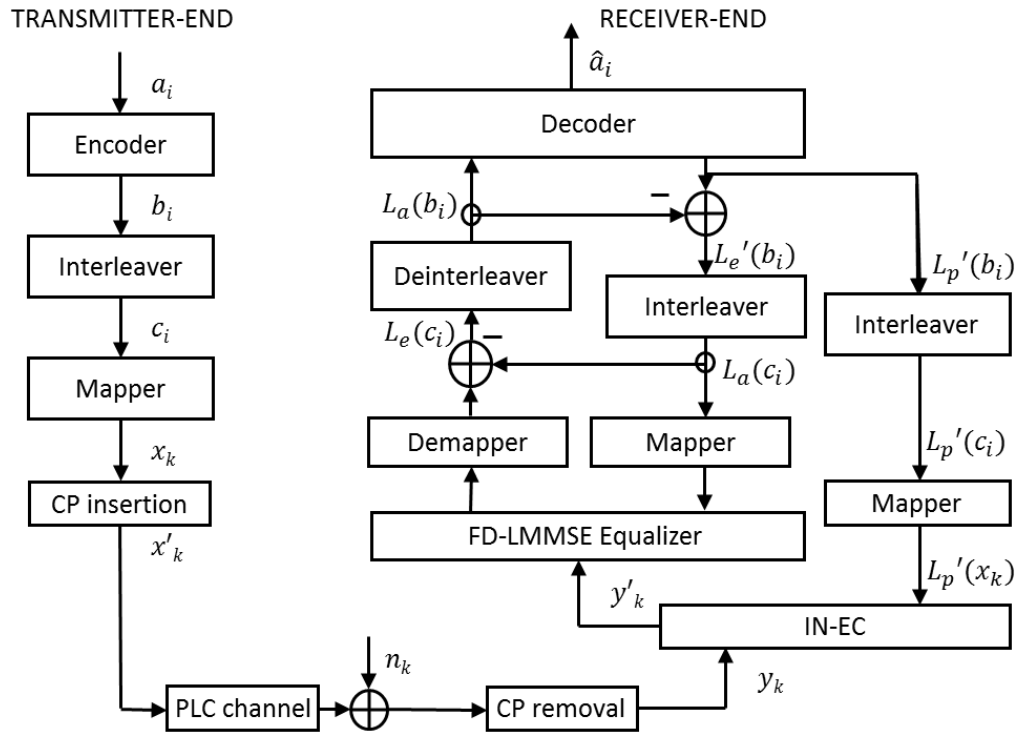


Figure 3.1 Block diagram of the proposed single carrier modulation which combines frequency domain turbo equalisation with iterative IN mitigation. .

3.1 Signal Model

As can be seen from Fig. 3.1, the incoming binary data sequence $\{a_i\}$ first passes through an encoder. This encoder adds some additional redundant information to the original binary data sequence, which aims to protect the original data from errors during transmission. Fig. 3.2 shows the block diagram of the rate-1/2 convolutional encoder. At each time i , one input bit a_i yields two output bits b_{2i-1} and b_{2i} ; i.e., $b_{2i-1} = a_i \oplus a_{i-2}$ and $b_{2i} = a_i \oplus a_{i-1} \oplus a_{i-2}$. After that, the coded binary sequence $\{b_i\}$ is permuted by an interleaver shown in Fig. 3.1 to avoid long error bursts. The interleaver processes random interleaving that is completely reversible at the receiver.

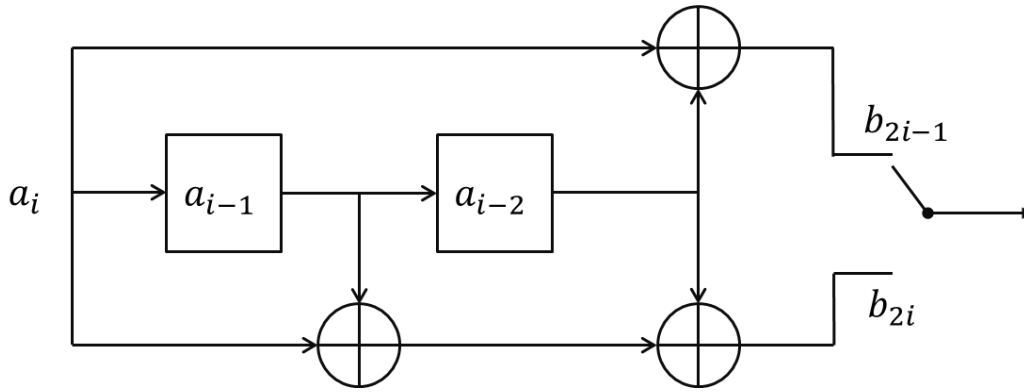


Figure 3.2 Block diagram of the encoder for a convolutional code.

Then, the interleaved bit sequence $\{c_i\}$ is input to a mapper. The role of the mapper is to convert the bit sequence $\{c_i\}$ to a symbol sequence x_k , which can be modulated onto the single carrier for block transmission through the PLC channel. Specifically, it divides the bit sequence $\{c_i\}$ into binary sub-sequences with length Z .

Each binary sub-sequence is mapped to a symbol x_k based on the mapping alphabet $\chi = \{\alpha_j, j = 1, 2, \dots, 2^Z\}$. Here, each element α_j corresponds to a binary vector $\mathbf{s}_j = [s_{j,1}, s_{j,2}, \dots, s_{j,Z}]^T$. The bit sequence $\{c_i\}$ can be rewritten as $\{c_{k,z}\}$, which denotes the corresponding z -th code bit in the symbol x_k .

After that, cyclic prefix is inserted into the transmitted signal for block transmission. The length of cyclic prefix must be at least equal to the length of the multipath PLC channel. Therefore, linear convolution of the frequency selective channel can be converted to circular convolution, which allows low complexity frequency-domain processing. After cyclic prefix insertion, the signal symbol \mathbf{x}' is shown as follows:

$$\mathbf{x}' = [x_0, \dots, x_{M-1}, x_M, \dots, x_{M+K-1}]^T, \quad (3.1)$$

where K and M denote the block length and the cyclic prefix length, respectively.

The signal symbol \mathbf{x}' is then transmitted through the power line channel which can be modelled as a length L tapped delay line. This thesis uses h_0, h_1, \dots, h_{L-1} to represent the taps and assumes that they are time invariant. Note, the transmitted symbol is affected by the additive noise n_k , which consists of the background noise and the IN. After removing cyclic prefix, the received signal \mathbf{y} is given by:

$$\mathbf{y} = \tilde{\mathbf{H}}\mathbf{x} + \mathbf{n} \quad (3.2)$$

↓

$$\begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_K \end{bmatrix} = \begin{bmatrix} h_0 & 0 & \dots & 0 & h_{L-1} & \dots & h_1 \\ h_1 & h_0 & \dots & & 0 & \dots & h_2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ h_{L-1} & h_{L-2} & \dots & & & & \vdots \\ 0 & h_{L-1} & \dots & & & & \vdots \\ \vdots & \vdots & \dots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & h_{L-1} & h_{L-2} & \dots & h_0 \end{bmatrix} \begin{bmatrix} x_0 \\ x_1 \\ \vdots \\ x_{K-1} \end{bmatrix} + \begin{bmatrix} n_0 \\ n_1 \\ \vdots \\ n_{K-1} \end{bmatrix},$$

where the power line channel matrix $\tilde{\mathbf{H}}$ is a circulant matrix as shown in the matrix form.

3.2 Single-Carrier Frequency-Domain Turbo Equalisation with Iterative IN Mitigation

This section outlines the proposed iterative receiver. Specifically, the received signal first passes through the proposed IN-EC module as shown in Fig. 3.1. This module works at time domain with an objective to mitigate IN from the received signal. Detailed algorithm of the IN-EC module will be introduced in Section 3.3. Then, the resulting time-domain ‘IN-free’ signal \mathbf{y}' is input to the frequency-domain soft-input soft-output equaliser; i.e., FD-LMMSE equaliser in Fig. 3.1. It first processes normalised discrete Fourier transformation to the ‘IN-free’ received signal, resulting in a frequency-domain signal model shown below:

$$\mathbf{F}\mathbf{y}' = \mathbf{F}\tilde{\mathbf{H}}\mathbf{F}^H \cdot \mathbf{F}\mathbf{x} + \mathbf{F}\mathbf{w}, \quad (3.3)$$

which can be adapted as

$$\mathbf{Y}' = \mathbf{D}\mathbf{X} + \mathbf{W}, \quad (3.4)$$

where \mathbf{Y}' , \mathbf{X} and \mathbf{W} denote the frequency-domain ‘IN-free’ signal, transmitted signal and background noise respectively. Note that, residual IN may be contained in the ‘IN-free’ signal due to unreliable signal estimate, in particular, at the first iterations. \mathbf{D} is a diagonal matrix; i.e., $\text{Diag}\{D_0, D_1, \dots, D_{K-1}\}$. This is because the matrix multiplication between the circulant matrix $\tilde{\mathbf{H}}$ and the column vector \mathbf{x} in time-domain is converted to scalar multiplication between the diagonal matrix \mathbf{D} and the column vector \mathbf{X} in frequency-domain. This significantly reduces the computational complexity of the following equalisation algorithm.

As shown in Fig. 3.1, the extrinsic information $L_e(c_i)$ is then flowed to the decoder in the soft information passing loop. This thesis uses the method proposed by Guo and Huang [55] to compute $L_e(c_i)$, which provides a more concise representation compared with the conventional mathematical model proposed by Tüchler et al.’s (see Chapter 2). The concise mathematical model for $L_e(c_i)$ (also denoted as $L_e(c_{k,z})$) is shown in Equation (3.5):

$$\begin{aligned} L_e(c_{k,z}) &= \ln \frac{\sum_{\alpha_j \in \chi_z^0} p(\mathbf{y}|x_k = \alpha_j) \prod_{z' \neq z} P(c_{k,z'} = s_{j,z'})}{\sum_{\alpha_j \in \chi_z^1} p(\mathbf{y}|x_k = \alpha_j) \prod_{z' \neq z} P(c_{k,z'} = s_{j,z'})} \\ &= \ln \frac{\sum_{\alpha_j \in \chi_z^0} \exp(-\frac{|x_k - m_k^e|^2}{v_k^e}) \prod_{z' \neq z} P(c_{k,z'} = s_{j,z'})}{\sum_{\alpha_j \in \chi_z^1} \exp(-\frac{|x_k - m_k^e|^2}{v_k^e}) \prod_{z' \neq z} P(c_{k,z'} = s_{j,z'})}, \end{aligned} \quad (3.5)$$

where $s_{j,z}$ represents the binary subsequence corresponding to symbol x_k as discussed in Section 3.1. χ_z^0 and χ_z^1 denote two alphabet subsets and their elements corresponds to binary subsequences with the z -th bit being 0 and 1, respectively. m_k^e and v_k^e are the extrinsic mean and extrinsic variance of x_k , which can be obtained via the following equations:

$$m_k^e = v_k^e \left(\frac{m_k^p}{v_k^p} - \frac{m_k^a}{v_k^a} \right) \quad (3.6)$$

and

$$v_k^e = \left(\frac{1}{v_k^p} - \frac{1}{v_k^a} \right)^{-1}. \quad (3.7)$$

Here, the a priori mean and variance m_k^a and v_k^a of the transmitted symbol can be calculated using the feedback log-likelihood ratio of the a priori probability (see $L_a(c_i)$ in Fig. 3.1), from the decoder. The conversion from $L^a(c_i)$; i.e., $L^a(c_{k,z})$, to $m_k^a \triangleq E(x_k)$ and $v_k^a = \text{Cov}(x_k, x_k)$ is given in Table I.

Table I Conversion from a priori log-likelihood ratio to a priori mean and a priori variance

Mapping algorithm	m_k^a	v_k^a
BPSK	$m_k^a = \tanh(L^a(c_{k,1})/2)$	$v_k^a = 1 - m_k^a ^2$
QPSK	$m_k^a = \frac{1}{\sqrt{2}} \cdot \tanh\left(\frac{L^a(c_{k,1})}{2}\right) + \frac{1}{\sqrt{2}} \cdot \tanh\left(\frac{L^a(c_{k,2})}{2}i\right)$	$v_k^a = 1 - m_k^a ^2$
8-PSK	$l_z = \tanh\left(\frac{L^a(c_{k,z})}{2}\right), z = 1,2,3,$ $m_k^a = \frac{(1 + \sqrt{2})i - 1}{4} \cdot l_1 - \frac{(1 + \sqrt{2} + i)}{4} \cdot l_2 + l_3 \cdot \left(\frac{1 - \sqrt{2} + i}{4}\right) \cdot l_1 + \frac{1 + (\sqrt{2} - 1)i}{4} \cdot l_2$	$v_k^a = 1 - m_k^a ^2$

Furthermore, the a posteriori mean m_k^p and a posteriori variance v_k^p in Equations (3.8) and (3.9) are calculated by applying the minimum mean square error principle [56] to the frequency-domain signal model (Equation (3.4)), which yields the following mathematical expressions:

$$\mathbf{m}^p = \mathbf{m}^a + \mathbf{F}^H \mathbf{D}^H \left(\mathbf{D} \mathbf{D}^H + \frac{\sigma_w^2}{\overline{v^a}} \mathbf{I} \right)^{-1} (\mathbf{Y}' - \mathbf{D} \mathbf{F} \mathbf{m}^a), \quad (3.8)$$

$$v_0^p = v_1^p = \dots = v_{K-1}^p = \frac{1}{K} \sum_{k=0}^{K-1} \left(\frac{1}{\overline{v^a}} + \frac{|d_k|^2}{\sigma_w^2} \right)^{-1}, \quad (3.9)$$

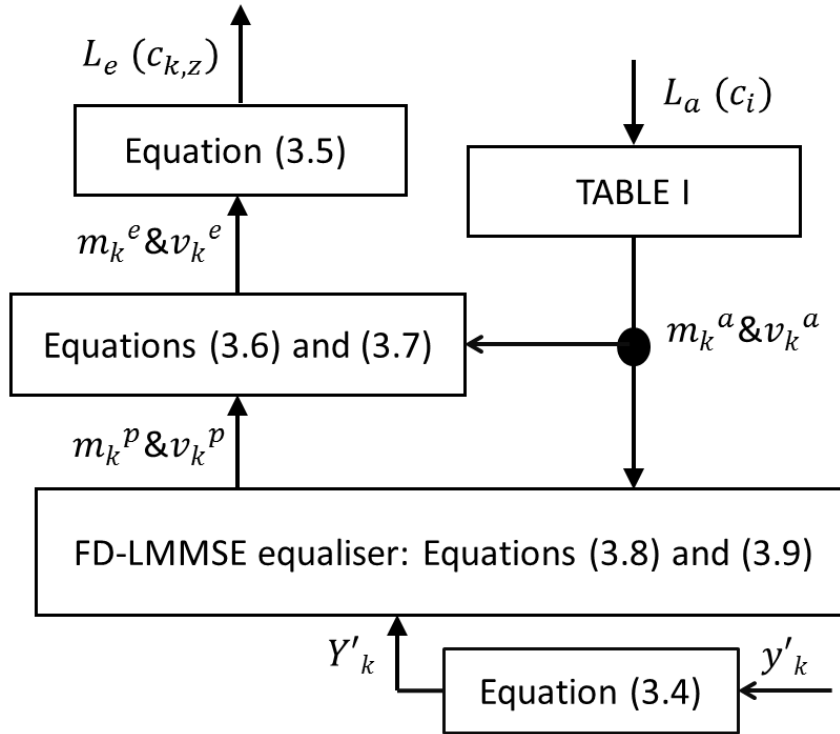


Figure 3.3 Flowchart of the algorithm used to compute the extrinsic information based on the observation and the a priori information.

where $\overline{v^a}$ represents the average value of the elements in \mathbf{v}^a , σ_w^2 denotes the variance of the background noise, d_k represents the k -th element in the diagonal matrix \mathbf{D} and K is the transmitted block length. Fig. 3.3 gives a detailed flowchart of the algorithm used to compute the extrinsic information $L_e(c_{k,z})$ using $L^a(c_i)$ and y'_k .

After the soft-input soft-output equalising, the de-interleaved log-likelihood ratio $L_a(b_i)$ is then input to the soft-input soft-output decoder as the a priori information for decoding. The decoder generates a new extrinsic log-likelihood ratio $L_e'(b_i)$, and feeds it back to the equaliser to enable the next iteration (see Fig. 3.1). In the final iteration, hard decisions are made by the decoder for the information bits $\{a_i\}$.

3.3 Iterative IN-EC

This section outlines the algorithm and the mathematical models for the proposed IN-EC module. According to Equation (3.2), the time-domain received signal \mathbf{y} is given by:

$$\mathbf{y} = \tilde{\mathbf{H}}\mathbf{x} + \mathbf{w} + \mathbf{i}, \quad (3.10)$$

which comprises three components, the signal portion $\tilde{\mathbf{H}}\mathbf{x}$, the background noise portion \mathbf{w} and the IN portion \mathbf{i} . The objective of the IN-EC is to remove the IN, i.e., \mathbf{i} , from the received signal \mathbf{y} . However, IN may be ‘hided’ in the data signal when it has a comparable magnitude with the signal (i.e., the signal to IN ratio is relatively high). This makes the detection of IN challenging. In order to prevent incorrect clipping, the IN-EC first subtracts the effect of the data signal from the observation \mathbf{y} , yielding to a time-domain residual signal in time as follows:

$$\hat{\mathbf{r}} = \mathbf{y} - \tilde{\mathbf{H}}\hat{\mathbf{x}} = \mathbf{w} + \mathbf{i} + \tilde{\mathbf{H}}(\mathbf{x} - \hat{\mathbf{x}}) = \mathbf{i} + \mathbf{w}', \quad (3.11)$$

where $\hat{\mathbf{x}}$ denotes the estimate of \mathbf{x} , which is calculated based on the a posteriori information from the decoder. As shown in Fig. 3.1, the a posteriori information of $\{b_i\}$, i.e., $L_p'(b_i)$, rather than the extrinsic information is fed into the IN-EC to generate $\hat{\mathbf{x}}$. This is because the extrinsic information only flows in the turbo equalisation loop to avoid positive feedback and the a posteriori information can achieve a better estimate of \mathbf{x} . Assume that QPSK mapping is used. The estimate of the transmitted signal $\hat{\mathbf{x}}$ is calculated as follows:

$$\hat{x}_k = m_k^p = \frac{1}{\sqrt{2}} \cdot \tanh\left(\frac{L_p'(c_{k,1})}{2}\right) + \frac{1}{\sqrt{2}} \cdot \tanh\left(\frac{L_p'(c_{k,2})}{2}\right) i. \quad (3.12)$$

The residual signal $\hat{\mathbf{r}}$ is then obtained by substituting Equation (3.12) into (3.11). After that, the IN-EC first identifies the locations of IN from the residual signal $\hat{\mathbf{r}}$ using the proposed sorting-based or thresholding-based method. Then it estimates IN at its occurrence locations by treating the IN \mathbf{i} as desired signal to be estimated and $\mathbf{w} + \tilde{\mathbf{H}}(\mathbf{x} - \hat{\mathbf{x}})$ as background noise \mathbf{w}' . The procedure of the IN-EC algorithm is as follows:

Step1. IN location detection

A. Sorting-based method

Sorting based method sorts the residual signal samples in decreasing order of amplitude, and assumes that the first Q samples contain IN, where Q is given by:

$$Q = \text{total symbol number} * p * \varepsilon_{limit}. \quad (3.13)$$

Here, p represents the IN occurrence probability. ε_{limit} is a limit value from zero to one with the objective to reduce the number of Q . By considering that IN has higher amplitude than the background noise \mathbf{w}' , ε_{limit} is calculated as follows:

$$\varepsilon_{limit} = 1 - \text{Prob}(|i| \leq |w'|) \quad (3.14)$$

where

$$\begin{aligned} \text{Prob}(|i| \leq |w'|) &= \int_0^{+\infty} \int_{|i|}^{+\infty} P_{|i|}(|i|) P_{|w'|}(|w'|) d|w'| d|i| \\ &= \frac{\sigma_{w'}^2}{\sigma_i^2 + \sigma_{w'}^2}. \end{aligned} \quad (3.15)$$

In Equation 3.15, $P_{|i|}(|i|)$ and $P_{|w'|}(|w'|)$ both follow Rayleigh distributions. σ_i^2 denotes the variance of the IN; i.e., \mathbf{i} , and $\sigma_{w'}^2$ denotes the variance of the background noise; i.e., \mathbf{w}' , which is given by:

$$\sigma_w'^2 = \tilde{H}(k,:) ^2 * v_k^p = \tilde{H}(k,:) ^2 * (1 - |m_k^p|^2). \quad (3.16)$$

Therefore, the values of $\sigma_w'^2$ and ε_{limit} are iteratively updated. This is because m_k^p , which approximately equals to the estimates of transmitted symbols, changes with the increase of iteration.

B. Thresholding-based method

Thresholding based method uses a threshold to test each element in $\hat{\mathbf{r}}$. If the amplitude of a vector exceeds the threshold, it is assumed to contain IN. The core of this method is to obtain the optimal threshold T . Therefore, it first computes the conditional probability of correct detection of IN and the false alarm avoidance of IN. Note that, both of these probabilities are functions of the threshold T . Then, the optimal value of T can be obtained by computing the trade-off between the correct detection and the false alarm of IN.

The probability of correct detection of IN is given by:

$$\begin{aligned} S_t(T) &= 2 \int_T^{+\infty} \text{Rayleigh}(|n_k|, \sigma_2) d|n_k| \\ &= 2 \int_T^{+\infty} \frac{|n_k|}{\sigma_2^2} \exp\left(\frac{-|n_k|^2}{2\sigma_2^2}\right) d|n_k| \\ &= 2 \cdot \exp\left(\frac{-T^2}{2\sigma_2^2}\right). \end{aligned} \quad (3.17)$$

In addition, the probability of the false alarm avoidance of IN is given by:

$$\begin{aligned}
S_p(T) &= 2 \int_0^T \text{Rayleigh}(|n_k|, \sigma_1) d|n_k| \\
&= 2 \int_0^T \frac{|n_k|}{\sigma_1^2} \exp\left(\frac{-|n_k|^2}{2\sigma_1^2}\right) d|n_k| \\
&= 2 \cdot \left(1 - \exp\left(\frac{-T^2}{2\sigma_1^2}\right)\right).
\end{aligned} \tag{3.18}$$

In Equations (3.17) and (3.18), the amplitude of n_k , i.e., $|n_k|$, follows Rayleigh distribution. Moreover, the false alarm of IN is computed by using one minus the false alarm avoidance, which yields to the following equation:

$$\overline{S_p} = 1 - S_p = 2 \cdot \exp\left(\frac{-T^2}{2\sigma_1^2}\right) - 1, \tag{3.19}$$

which is the function of T as well as S_t . As a larger S_t leads to a larger $\overline{S_p}$, the trade-off between these two probabilities can be obtained by maximising the difference between them. Thus, an optimal threshold should satisfy the following equation:

$$\begin{aligned}
T_{optimal} &= \operatorname{argmax}_{T>0} \{S_t - \overline{S_p}\} \\
&= \operatorname{argmax}_{T>0} \left\{ 2 \cdot \exp\left(\frac{-T^2}{2\sigma_2^2}\right) - 2 \cdot \exp\left(\frac{-T^2}{2\sigma_1^2}\right) + 1 \right\}
\end{aligned} \tag{3.20}$$

Let $\xi'(T)$ to represent the derivation of T . In order to maximise $S_t - \overline{S_p}$, the derivation of T needs to be zero; i.e., $\xi'(T_{optimal}) = 0$. Therefore, the optimal threshold $T_{optimal}$ is obtained by the following equation:

$$\begin{aligned} T_{optimal} &= \sqrt{\frac{2\sigma_1^2\sigma_2^2}{\sigma_2^2 - \sigma_1^2} \ln\left(\frac{\sigma_2^2}{\sigma_1^2}\right)} \\ &= \sigma_w \sqrt{\frac{2(1+\mu)}{\mu} \ln(1+\mu)}. \end{aligned} \quad (3.21)$$

Compared with the thresholding based IN detection method, the sorting-based method is easily implemented. However, it requires extra information of the IN occurrence probability. On the other hand, the thresholding-based method may achieve better performance as it searches all samples in $\hat{\mathbf{r}}$ to detect the occurrence of IN. The performance of both sorting-based and thresholding-based IN location detection methods are simulated and compared in Section 3.4.

Step2. IN estimation

Given the occurrence locations of IN, the next step is to estimate IN at these locations. This thesis uses two estimation approaches: least square (LS) estimation shown in Equation (3.22) and minimum mean square error (MMSE) estimation shown in Equation (3.23).

$$\text{LS:} \quad i'_k = \begin{cases} \hat{r}_k, & k \in \text{IN locations} \\ 0, & \text{otherwise} \end{cases} \quad (3.22)$$

$$\text{MMSE:} \quad i'_k = \begin{cases} \frac{\sigma_i^2}{\sigma_i^2 + \sigma_w'^2} \cdot \hat{r}_k, & k \in \text{IN locations} \\ 0, & \text{otherwise} \end{cases}. \quad (3.23)$$

Note, in the MMSE estimation, when the value of σ_i^2 is significantly larger than that of $\sigma_w'^2$, i.e., strong IN environment, the value of the coefficient $\frac{\sigma_i^2}{\sigma_i^2 + \sigma_w'^2}$ is approximately one. In this case, the least square estimation and minimum mean square error estimation have similar results.

Step3. IN cancellation

After IN estimation, IN-EC subtracts the estimate of IN from the received signal to achieve the 'IN-free' signal y'_k as follows:

$$y'_k = y_k - i'_k. \quad (3.24)$$

Finally, y'_k is input to the soft-input soft-output equaliser; i.e., FD-LMMSE equaliser, as mentioned in Section 3.2 to achieve frequency-domain turbo equalisation.

In summary, this chapter proposes a novel SC-FDTE based PLC system coupled with iterative IN mitigation. Theoretically, by using the two message passing loops designed in the receiver, where one between the equaliser and the decoder; another one between the IN-EC and the decoder, it improves both performance of the signal

detection and the IN mitigation. Moreover, the performance of the IN mitigation module can be improved based on a more reliable estimate of signal symbols, and the updated 'IN-free' received signal, in turn, makes a more accurate input 'IN free' observation for the signal detection algorithm. Therefore, the proposed iterative approach for PLC is able to achieve significant performance gain compared with conventional non-iterative OFDM and SC-FDE based PLC systems.

In addition, IN-EC module first subtracts signal portion contained in the received observation, then detects IN from the residual signal. Consequently, the novel iterative IN mitigation avoids triggering incorrect clipping in the receiver front-end IN processor. The incorrect clipping is caused by signal symbols with large amplitudes, because these useful signal symbols might be considered as IN and then clipped. Moreover, given the proposed IN-EC algorithms, the sorting based method is easily implemented and the thresholding based method can achieve a better IN detection. Simulation results for the proposed approaches as well as comparisons with conventional strategies are presented in the next section.

3.4 Simulation Results and Analysis

This section investigates performance of the proposed SC-FDTE with iterative IN mitigation receiver structure under PLC channel under impulsive environment. Firstly, simulation results of the PLC channel and the IN are outlined in section 3.4.1. In order

to evaluate the ISI mitigation performance improvement of the SC-FDTE based PLC system over that of the OFDM and the SC-FDE based PLC systems, Section 3.4.2 compares the BER performance of these systems under two circumstances: IN free environment and impulsive environment. In the IN free environment, only the background noise is contained in the total additive noise. On the other hand, the impulsive environment introduces IN. After that, Section 3.4.3 demonstrates the performance of the proposed sorting based method and the thresholding based method for IN-EC in terms of convergence rate and BER. Here, convergence rate denotes the variation of BER with the increase of iteration, which aims to show the speed that BER approaching its limit. Finally, Section 3.4.4 compares the BER performance of the proposed SC-FDTE based PLC system coupled with novel iterative IN mitigation with other conventional approaches to test the effectiveness of the proposed approach in ISI and IN mitigation.

3.4.1 Simulation Results for PLC Channel and IN

As mentioned in Chapter 2, this thesis uses Zimmermann and Dostert's [27] multipath model and Bernoulli-Gaussian model to implement the PLC channel matrix and generate IN, respectively. Therefore, by using the parameters of a typical 4-path in-home reference PLC channel (see Table II), the channel frequency response $H(f)$ is obtained based on Equation (2.1) in Chapter 2. Fig. 3.4(a) shows the amplitude response. It can be seen that the magnitude transfer function $|H(f)|$ clearly shows the notches which are corresponding to the branches between transmitter and receiver.

Besides, the low-pass characteristic is quite obvious, namely, both depth and sharpness of the notches experience attenuations with the increase of frequency. The impulse response can be determined from the frequency response, as shown in Fig. 3.3(b), which can be modelled as a length L tapped delay line.

Table II Parameters of a 4-path reference power line channel

Attenuation Parameters		
$k = 1$	$a_0 = 0$	$a_1 = 7.8 \cdot 10^{-10} \text{ s/m}$
Path Parameters		
i	g_i	$d_i(\text{m})$
1	0.64	200
2	0.38	222.4
3	-0.15	244.8
4	0.05	267.5

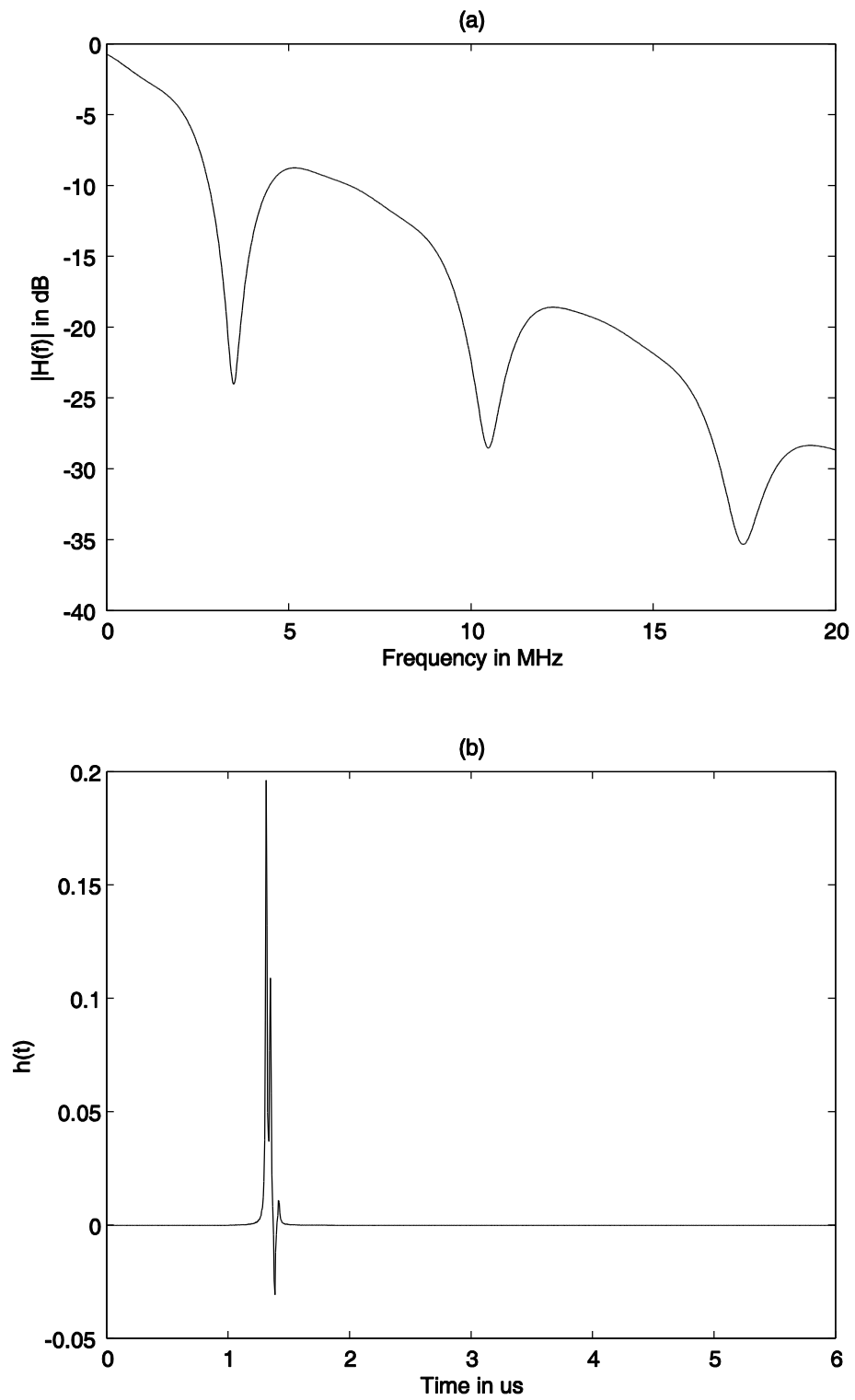
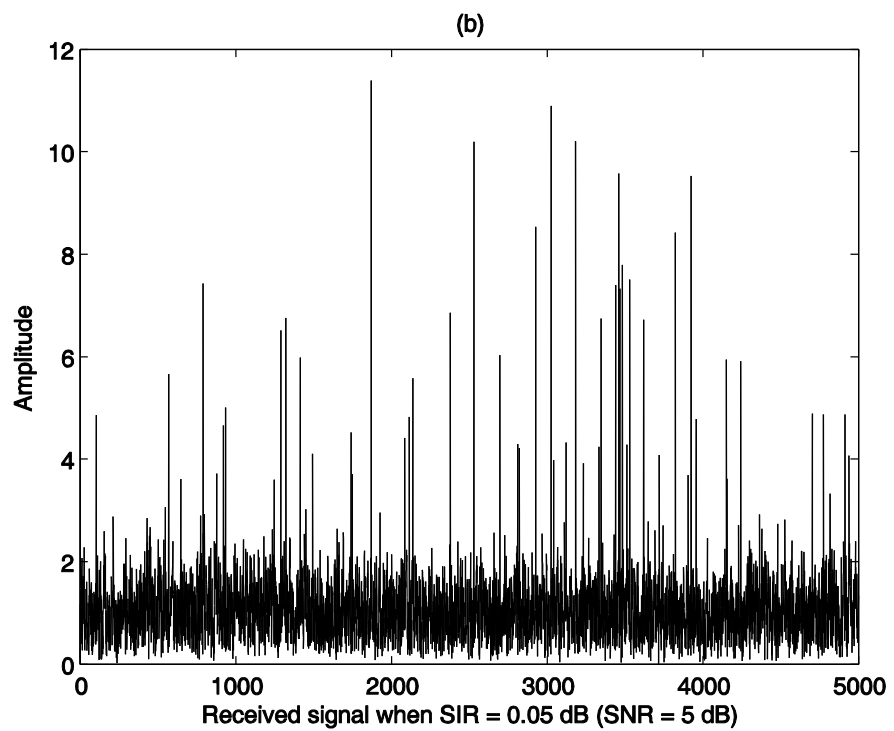
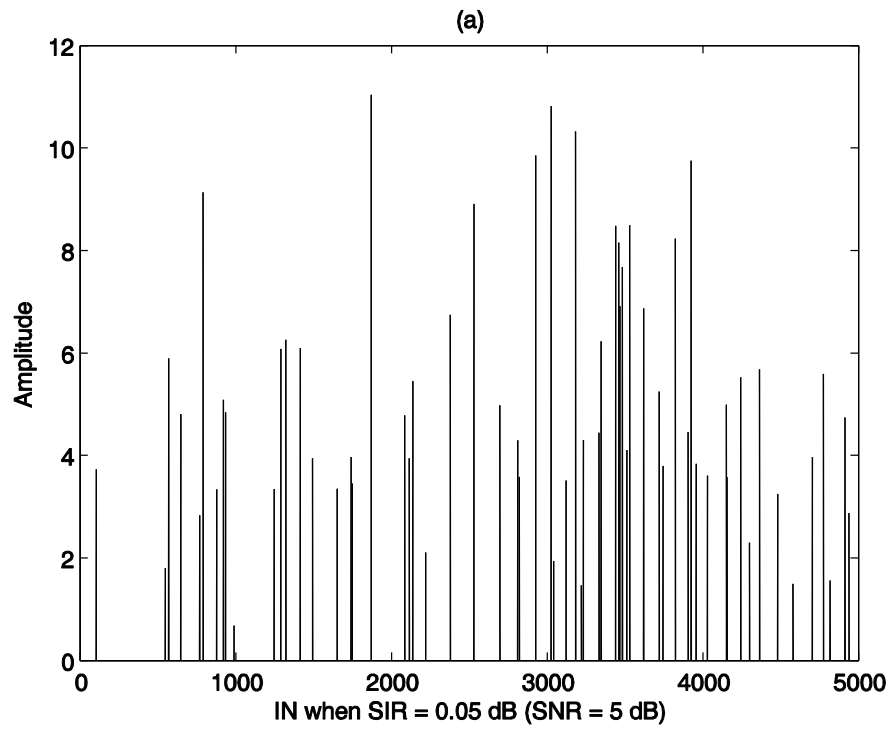


Figure 3.4 Amplitude response (a) and impulse response (b) for the 4-path reference PLC channel.

In order to generate IN based on the Bernoulli-Gaussian model, this thesis uses the parameters that have been widely used in literature [17, 32, 33, 57-59]. Specifically, the IN occurrence probability is 0.01, i.e., $p = 0.01$, and the variance of IN equals to 100 times that of the background noise; i.e., $\mu = 100$. Fig. 3.5 illustrates the amplitudes of two IN examples and the corresponding received signals. Signal symbol length is 5000 and the SIRs equal to 0.05 dB (SNR = 5 dB) and 0.1 dB (SNR = 10 dB), respectively. It is observed that the generated IN has random occurrence and random amplitude shown in Fig. 3.5(a) and Fig. 3.5(c). Moreover, the corresponding received signals, see Fig. 3.5(b) and Fig. 3.5(d), show that some impulses are concealed by signal, especially when SIR is large (see Fig. 3.4(d)). Fig. 3.4 demonstrates that IN mitigations based on thresholding the received signal; i.e., receiver front-end, may cause incorrect clipping of the useful signal if a signal symbol has comparable amplitude with IN.



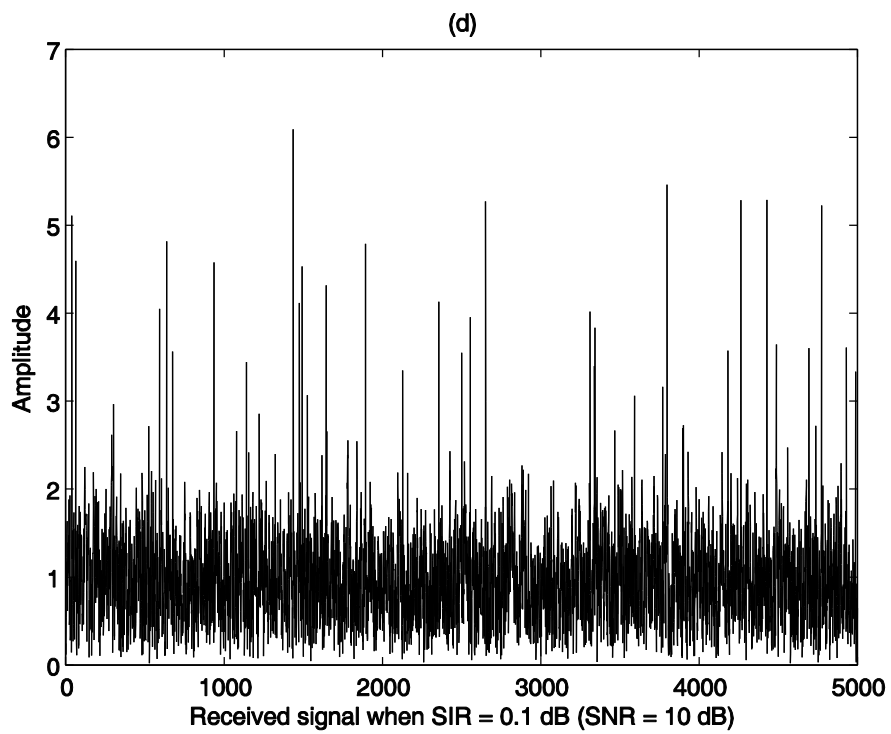
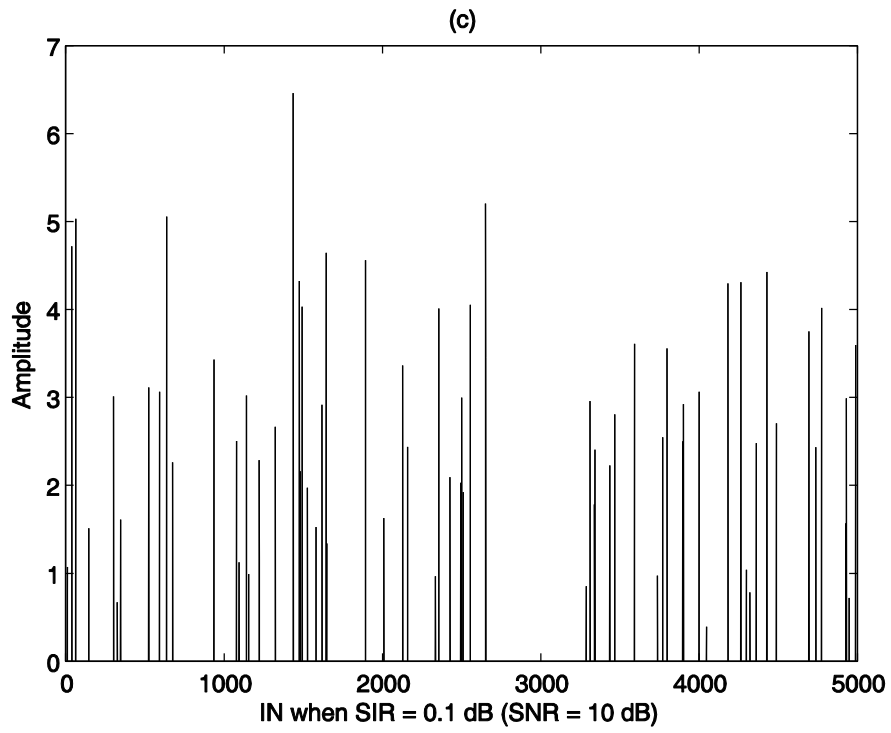


Figure 3.5 Two examples of IN and the corresponding received signal with symbol length=5000 under SIR=5 dB (a) and (b) and SIR=10 dB (c) and (d), respectively.

The other parameters used in the subsequent simulations are as follows: the length of the information bit frame is 12798; the encoder is a rate-1/2 convolutional encoder with generator (5, 7), which is initialised to an all-zero state; the interleaver applies random interleaving and the mapper uses the quadrature phase-shift keying Gray mapping. Moreover, the single-carrier block length K is fixed to 128.

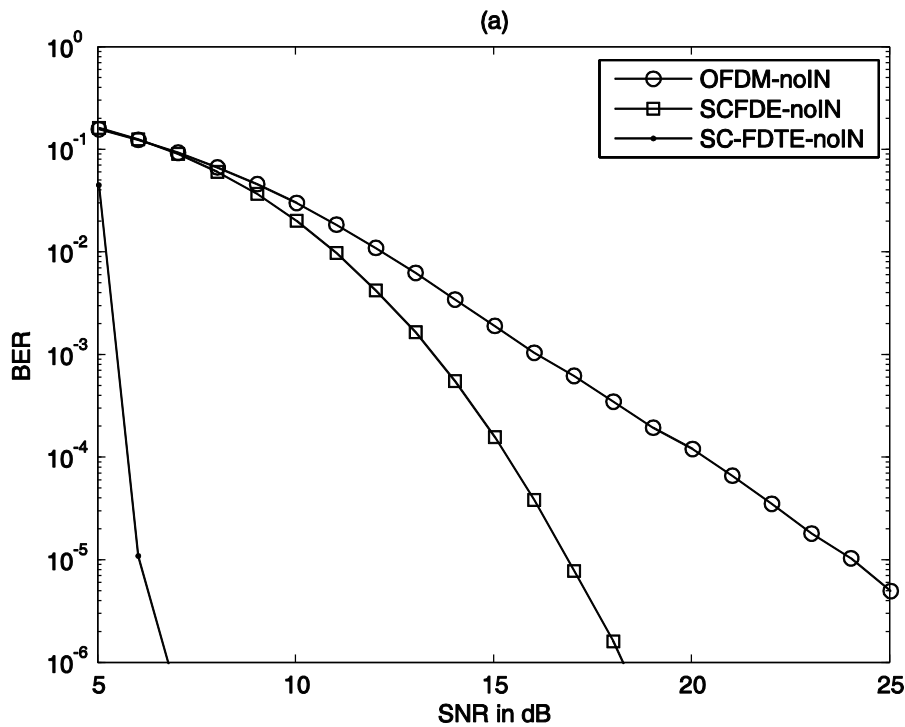
3.4.2 BER Performance of OFDM, SC-FDE and SC-FDTE based PLC Systems

Given the aforementioned parameters, this section compares the performance of the OFDM-, SC-FDE- and SC-FDTE-based PLC systems in terms of BER under two scenarios: (1) IN free environment, denoted as noIN in the following figures; and (2) impulsive environment, denoted as IN in the following figures. In this experiment, both OFDM and SC-FDE based PLC systems use the non-iterative receiver structure as shown in Chapter 2. On the other hand, the proposed SC-FDTE PLC system runs 10 iterations.

Fig. 3.6 shows the BER performance of these PLC systems. It can be seen that the SC-FDE based PLC system outperforms the OFDM based PLC system in both scenarios. This means that SC-FDE has an advantage over OFDM in coping with the multipath PLC channel. Fig. 3.6 also shows that the SC-FDTE approach has the best performance, which achieves a more than 10 dB performance gain compared with the OFDM- and SC-FDE based PLC systems no matter IN is generated or not. Fig. 3.6(a) indicates the ISI mitigation ability of these PLC systems, it can be observed that the SC-FDTE-noIN is able to effectively mitigate ISI and outperforms the OFDM-noIN and the SC-FDE-noIN

by 20 dB and 11 dB respectively. Moreover, by comparing the curves between Fig. 3.6(a) and (b), it shows that IN significantly degrades the BER performance. Even for the SC-FDTE based PLC system, a 9 dB performance degradation can be observed.

In summary, robust SC-FDTE based PLC system can effectively mitigate ISI and significantly outperforms the non-iterative OFDM and SC-FDE based PLC systems in ISI elimination. Moreover, the presence of IN leads to severe performance degradations to all of these PLC systems, which indicates that powerful IN mitigation is desirable to cope with the 9 dB performance gap.



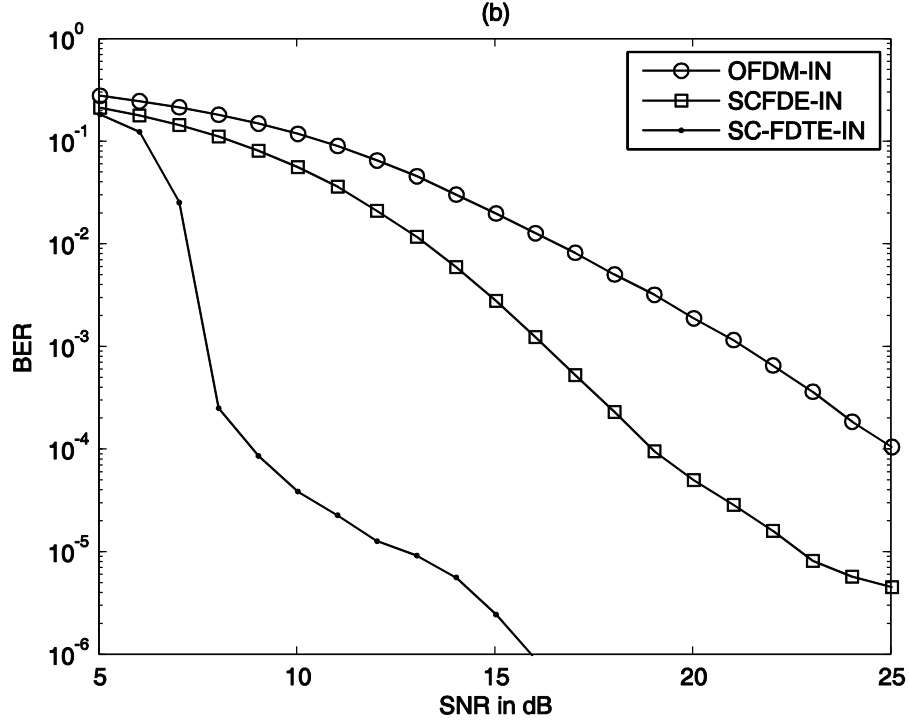
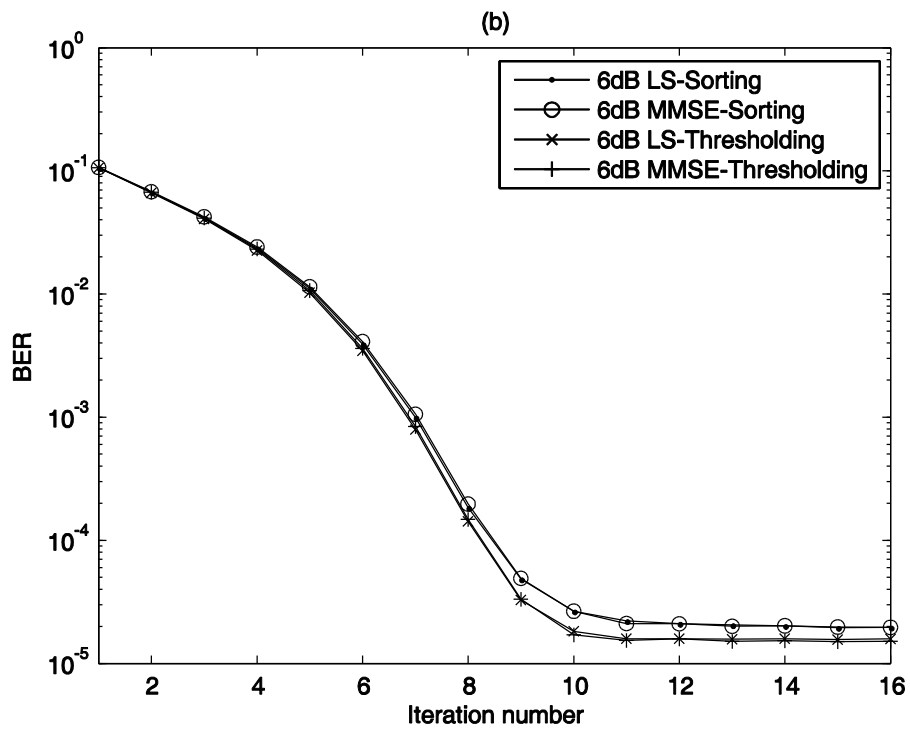
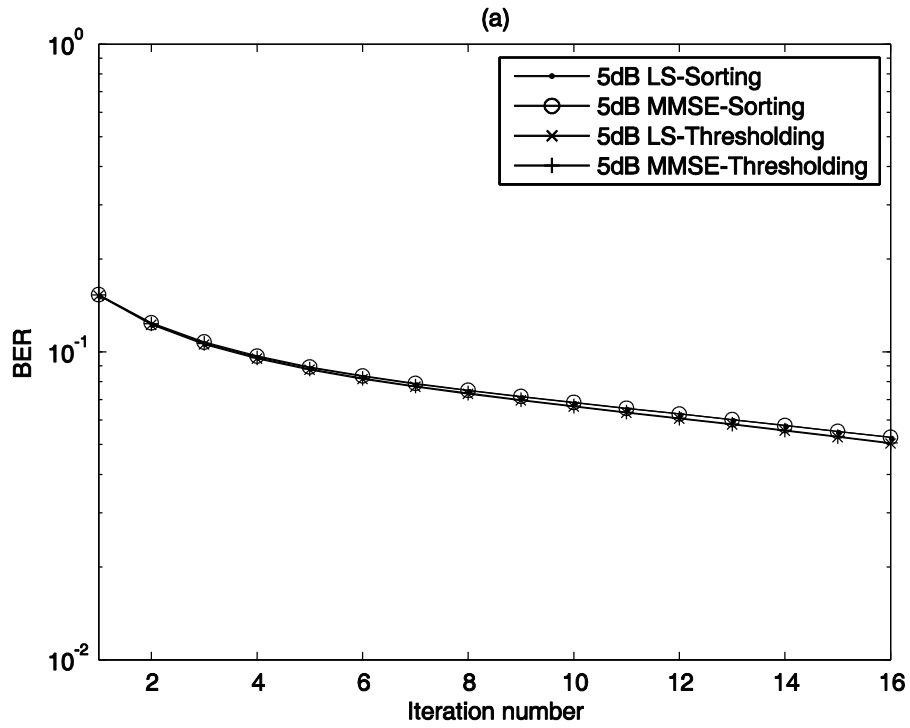


Figure 3.6 BER performance comparison between OFDM-, SC-FDE- and SC-FDTE based PLC systems under two scenarios: (a) IN free environment, and (b) impulsive environment (Parameters for IN: $p = 0.01, \mu = 100$).

3.4.3 Convergence Rates and BER Performance of the Proposed IN-EC Algorithms

This section compares the convergence rate and BER performances of LS-Sorting, MMSE-Sorting, LS-Thresholding and MMSE-Thresholding IN-EC algorithms based on SC-FDTE PLC systems. Here, LS and MMSE denote least square estimation and minimum mean square error estimation for IN. Sorting and thresholding represent the proposed sorting based IN detection method as well as the thresholding based IN detection method. The simulation results of convergence rates in terms of SNRs equalling to 5 dB, 6 dB, 7 dB and 8 dB are shown in Fig. 3.7(a), (b), (c) and (d),

respectively.



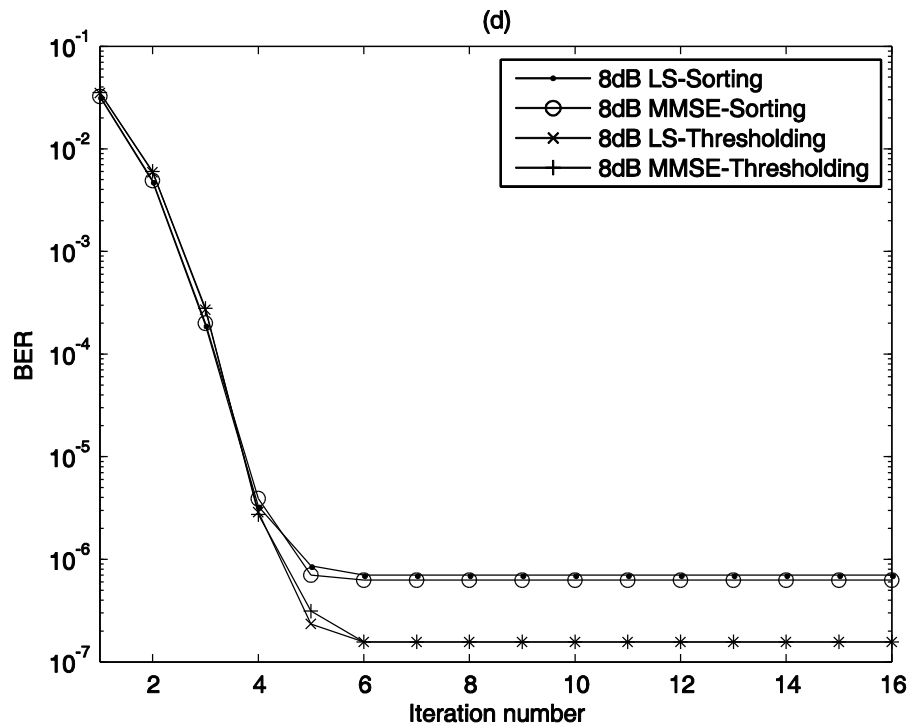
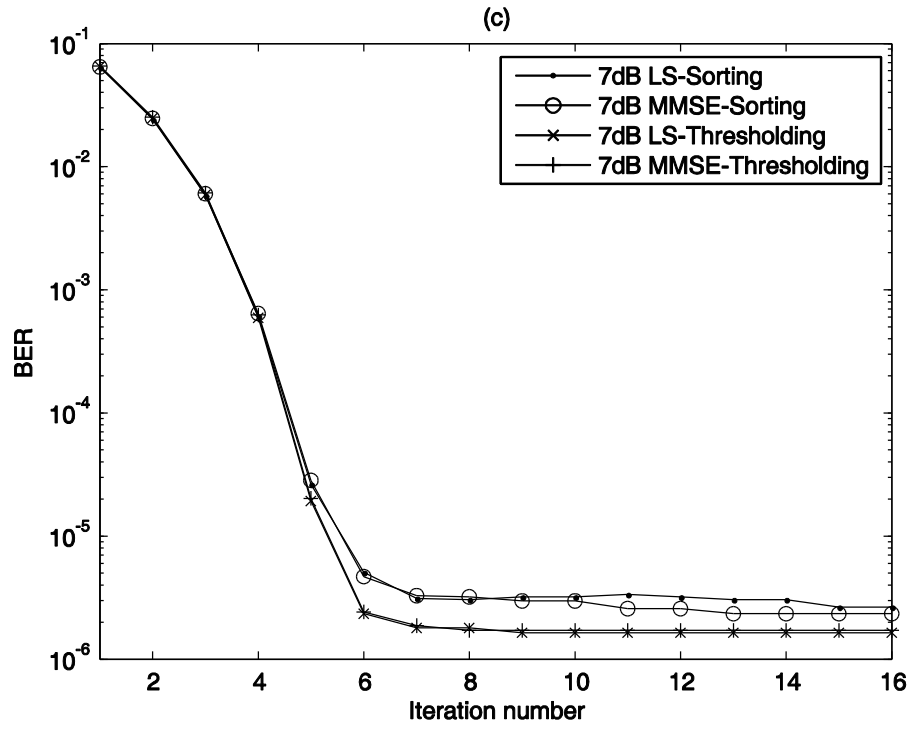


Figure 3.7 Convergence rate of the proposed IN-EC algorithms under different SNR: (a) SNR = 5 dB, (b) SNR = 6 dB, (c) SNR = 7 dB, (d) SNR = 8 dB.

From Fig. 3.7, it can be seen that a larger SNR leads to a faster convergence rate for these algorithms. Moreover, under different SNRs, the LS-Thresholding and the MMSE-Thresholding outperform the LS-Sorting and the MMSE-Sorting by achieving lower BERs after converging. In addition, with the increase of iteration, all of these proposed iterative IN-EC algorithms converge at the 10th iteration. Thus, this thesis fixes the number of iteration to ten in the rest experiments.

Fig. 3.8 compares the performance of the aforementioned IN-EC algorithms in terms of BER performance. Note, all of these iterative IN-EC algorithms run ten iterations. In addition, two bounds are also given for reference, which are LS-knownIN and MMSE-knownIN. These two bounds are obtained by estimating IN using LS and MMSE estimations at certain IN occurrence locations. From Fig. 3.8, it is observed that both performance of the LS-Thresholding and the MMSE-Thresholding is close to that of the LS-knownIN and the MMSE-knownIN. Moreover, the LS-Thresholding outperforms the LS-Sorting by 0.5 dB. Similarly, the MMSE-Thresholding outperforms the MMSE-Sorting by 0.5 dB as well. On the other hand, the least square estimation based systems and the minimum mean square error estimation based systems have similar BER when using the same IN location detection algorithms. A similar phenomenon can also be found between the curves of LS-knownIN and MMSE-knownIN.

In summary, with the increase of SNR, SC-FDTE based PLC systems coupled with the proposed IN-EC algorithms achieve faster convergence rates and all converge after

ten iterations. Moreover, no matter which IN estimation approach is used, IN detection performance of both sorting based method and thresholding based method approaches the optimal, with the thresholding method slightly outperforming the sorting based method.

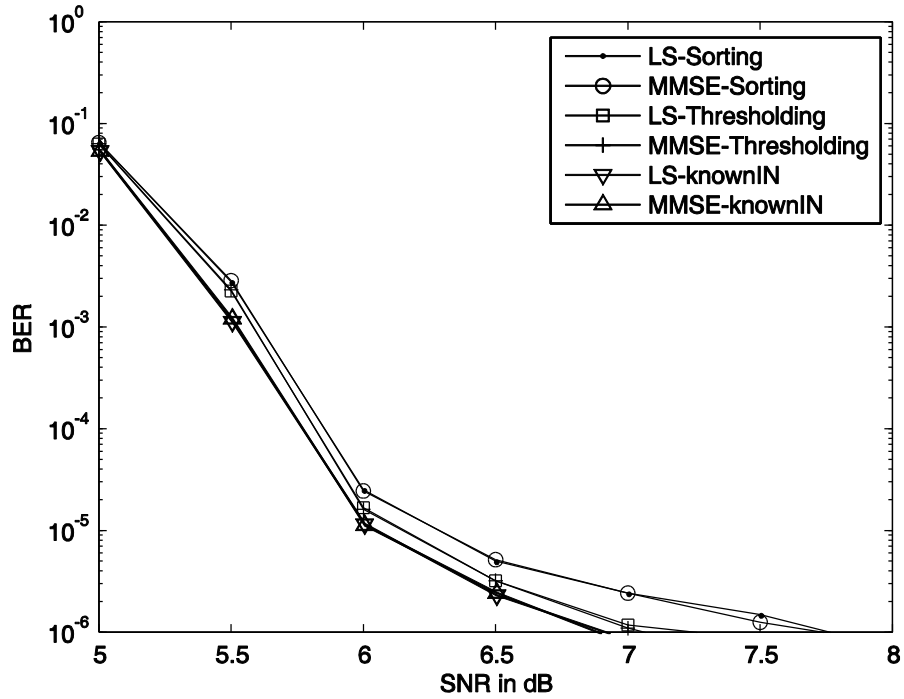


Figure 3.8 BER performance comparison between SC-FDTE based PLC systems coupled with the proposed IN-EC algorithms.

3.4.4 BER Performance of the Proposed Receiver based PLC System and the Conventional PLC Systems

This section compares the proposed SC-FDTE with iterative IN-EC approaches; i.e.,

SC-FDTE MMSE-Sorting and SC-FDTE MMSE-Thresholding, with the conventional non-iterative PLC approaches; i.e., OFDM-Equaliser backend INM, OFDM-Receiver frontend INM, SC-FDE-Equaliser backend INM and SC-FDE-Receiver frontend INM. Note that, in the joint clipping and blanking algorithm, the optimal clipping threshold is computed based on the method introduced by Ndo et al [54] (see Chapter 2), and the blanking threshold is chosen as 1.4 times the clipping threshold. The iterative SC-FDTE approach coupled with non-iterative receiver front-end IN mitigation (SC-FDTE-Receiver front-end INM) is also implemented to test the performance improvement of the novel iterative IN-EC module. In addition, the BER performance of the communication system based on additive white Gaussian noise channel, i.e., AWGN, as well as the SC-FDTE PLC system under IN free environment (SC-FDTE noIN) is presented as the performance bounds for ISI mitigation and IN mitigation, respectively.

As shown in Fig. 3.9(a), when SNR is smaller than 20 dB, the OFDM-Receiver frontend INM achieves a performance similar to that of the OFDM-Equaliser backend INM. Similar phenomenon can be seen between the SC-FDE-Receiver frontend INM and the SC-FDE-Equaliser backend INM. However, with the increase of SNR, both of the OFDM-Receiver frontend INM and the SC-FDE-Receiver frontend INM suffer from severe performance degradations. This is due to the incorrect clipping of the useful signal symbols in the receiver front-end IN processor. On the other hand, both of the OFDM-Equaliser backend INM and the SC-FDE-Equaliser backend INM are proved to avoid such BER degradation. This is because the equaliser back-end IN processor first

subtracts the impact of signal portion from the received signal. Therefore, signal symbols with large amplitude will not affect IN detection and mitigation. Furthermore, the SC-FDTE-Receiver frontend INM achieves a BER of 10^{-6} when SNR is 15 dB. Although SC-FDTE based PLC system with non-iterative IN mitigation does not suffer from performance degradation as other receiver front-end IN processor based PLC systems, the performance of this PLC system is still bad due to the weak non-iterative IN mitigation. Fig. 3.9(a) also shows that both of the SC-FDTE MMSE-Sorting and the SC-FDTE MMSE-Thresholding achieve significant performance gain, i.e., more than 20 dB, compared with the non-iterative OFDM-Equaliser backend INM and the SC-FDE-Equaliser backend INM. Moreover, under the same SC-FDTE based PLC system, both of the proposed SC-FDTE MMSE-Sorting and SC-FDTE MMSE-Thresholding outperform the non-iterative IN mitigation, i.e., SC-FDTE-Receiver frontend INM, by more than 7 dB.

Fig. 3.9(b) shows a zoomed up part of Fig. 3.9(a). It can be seen that with the increase of SNR, the BER of SC-FDTE no IN approaches the AWGN when SNR is larger than 6.5 dB. This indicates that the SC-FDTE is a robust method to cope with the ISI PLC channel and its signal detection performance is close to the optimal bound under the IN free scenario. Moreover, both of the SC-FDTE MMSE-Sorting and the SC-FDTE MMSE-Thresholding in Fig. 3.9(b) deliver superior BER performance, i.e., only a 0.2 dB performance gap can be observed between the proposed SC-FDTE MMSE-Thresholding and the optimal IN and ISI mitigation bounds.

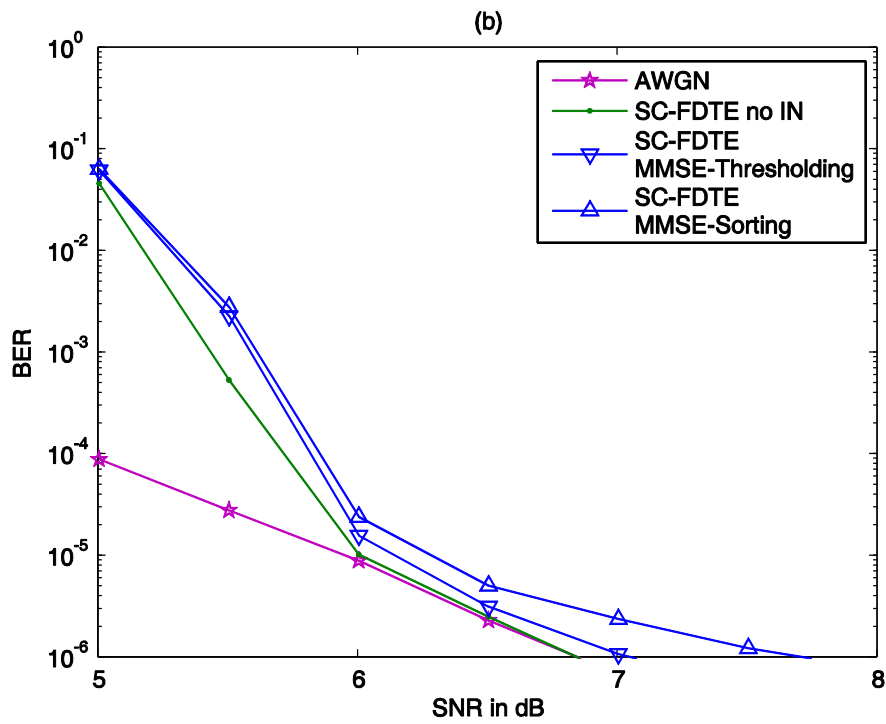
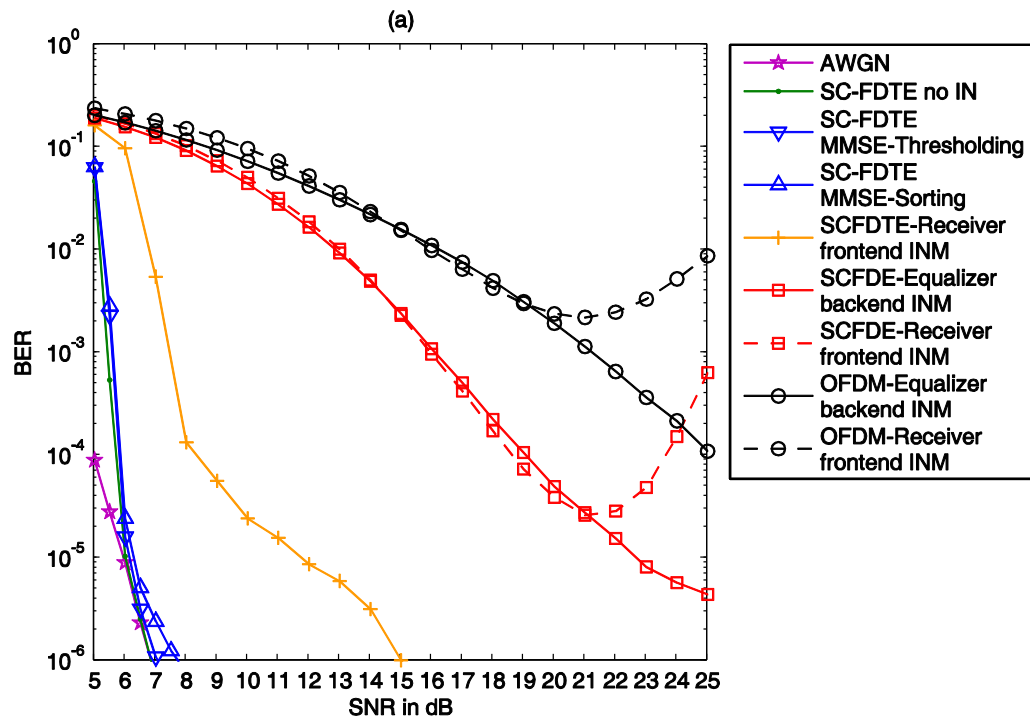


Figure 3.9 BER performance comparisons between the proposed PLC system and the conventional PLC systems.

In summary, both OFDM and SC-FDE based PLC systems coupled with receiver front-end IN processor lead to performance degradations caused by incorrect clipping when SNR is relatively large. On the other hand, equaliser back-end IN processor avoids this degradation and are able to cope with IN at high SNRs. Furthermore, SC-FDTE based PLC system is the best and the most robust system, which can achieve satisfactory BER performance at low SNR. Therefore, even coupled with the receiver front-end IN processor, this system does not suffer from BER performance degradation. However, non-iterative IN mitigation provides bad performance in IN mitigation. Even for the robust SC-FDTE based PLC system, there is still an 8 dB performance degradation to be addressed.

In addition, the proposed SC-FDTE based PLC system coupled with iterative IN mitigation can effectively mitigate ISI and IN in PLC, and achieves significant performance gains compared with the conventional PLC systems coupled with non-iterative IN processors. It also distinctly outperforms the SC-FDTE based PLC system with non-iterative IN mitigation. Moreover, iterative IN-EC using the proposed thresholding based IN detection method delivers a performance close to the bound.

3.5 Summary

This chapter presents detailed algorithm of the proposed SC-FDTE based PLC system with iterative IN mitigation. The system couples an iterative IN mitigation module; i.e.,

IN-EC, with turbo equalisation. With the increase of iteration, both performance of the IN mitigation and the turbo equation can be improved. Moreover, two IN detection methods are proposed for the IN-EC module: sorting based method and thresholding based method. The proposed iterative receiver structure is able to iteratively mitigate IN and ISI and achieves distinct performance gain compared with conventional non-iterative OFDM and SC-FDE PLC systems. Moreover, single carrier modulation addresses the EMC constraints for PLC systems.

Simulation results in Section 3.4 verify the effectiveness of the proposed iterative receiver structure on ISI and IN mitigation. The proposed system significantly outperforms the conventional OFDM and SC-FDE based PLC systems and achieves the BER that is very close to the performance bounds. In addition, both of the novel IN detection methods for IN-EC present distinct IN detection performance which approaches the performance of the optimal IN detection. Moreover, it is observed that the thresholding based method outperforms the sorting based method.

Chapter 4 Conclusion and Future Work

4.1 Conclusion and Contributions

As a promising communication technology and an effective alternative solution for the existing wireline and wireless communication systems, PLC has become an active research topic. The major advantage of PLC is the universal existence of power lines, which not only enables remote regions having access to the global internet, but also saves human and material resources from establishing additional communication infrastructure. However, the specific topology of power lines and the different electrical appliances plugged in the power system pose challenges for PLC. Specifically, ISI caused by multipath propagation and signal reflections at branches between the transmitter and the receiver leads to severe signal distortions. In addition, the switching transients of electrical appliances generate strong IN in the PLC channel,

which significantly degrades the reliability of data communications. Except for the ISI and IN, in order to avoid interference to other communication systems, the EMC constraints regulate a limit to the signal power transmitted in the power line systems.

To address these challenges, this thesis proposes to use single carrier modulation due to its lower PAPR compared with the conventional multicarrier modulation. Moreover, a novel iterative receiver, i.e., frequency domain turbo equalisation with iterative IN mitigation, has been developed. Frequency-domain equalisation provides lower complexity compared with the time-domain equalisation, which is able to cope with the heavily dispersive PLC channel. On the other hand, turbo equalisation makes a powerful ISI elimination approach with performance approaching the optimal MAP signal detection. The objective of the IN-EC is to mitigate IN from the received signal. It follows the proposed three-step algorithm, which includes the IN location detection, IN estimation and IN cancellation. In this thesis, two IN detection methods are designed to be implemented in the IN-EC: the sorting based method and the thresholding based method. It is worth highlighting that the turbo equalisation facilitates the iterative operation between the equaliser and IN-EC. The equaliser delivers estimate of the transmitted data signal to the IN-EC and IN-EC supplies the turbo equaliser with 'IN free' received signal. Consequently, the iterative receiver is able to mitigate ISI and IN iteratively, thereby achieving a significant performance gain compared with existing PLC techniques.

The effectiveness on ISI and IN mitigation of the proposed iterative receiver is verified in Chapter 3. Specifically, under a 4-path reference PLC channel, PLC system based on the proposed receiver significantly outperforms the conventional

non-iterative OFDM and SC-FDE based PLC systems, which are coupled with non-iterative IN mitigation, by about 20 dB at a BER of 10^{-5} , and it is able to achieve a performance close to the AWGN bound. In addition, It is verified that, PLC system with IN-EC based on either the proposed sorting or thresholding IN detection approach shows a performance approaching the IN detection bound, where the IN occurrence location are exactly known. Besides, PLC system with IN-EC based on the thresholding IN detection method outperforms that of the sorting IN detection method. As a conclusion, this thesis makes the following contributions:

1. This thesis proposes a novel receiver for PLC that enables iterative ISI and IN mitigations. Specifically, this receiver combines an iterative IN mitigation approach, i.e., the IN-EC module, with robust SC-FDTE. Therefore, in all iterations of the receiver, the IN-EC and the turbo equalisation supply information to each other, i.e., the estimate of the transmitted signal generated via the turbo equalisation is input to the IN-EC, and in turn, the IN-EC feeds its output 'IN free' received signal to the turbo equaliser. Compared with the conventional OFDM and SC-FDE based PLC systems with non-iterative IN mitigation approaches, the proposed iterative receiver is more powerful by introducing soft message passing loop. Simulation results in Chapter 3 demonstrate that, the SC-FDTE based PLC system with iterative IN mitigation significantly outperforms the conventional non-iterative OFDM and SC-FDE based PLC systems with receiver front-end IN processor or equaliser back-end IN processor.

2. This thesis proposes a novel iterative IN mitigation module. It constitutes of three components, namely, IN location detection, IN estimation and IN mitigation. However, due to the ‘interference’ caused by large amplitude signal symbols, it is difficult to detect and estimate IN from the received observation, especially when the SIR is relatively high. Therefore, before carrying out the IN location detection, the proposed IN-EC first attempts to eliminate the effect of the data signal from the received signal through signal cancellation. By using the estimates of the transmitted signal symbols input to the IN-EC, signal cancellation can be achieved. Then, IN-EC uses the sorting based IN detection method or the thresholding based IN detection method to detect the IN occurrence locations. After IN localisation, this module estimates IN at its occurrence locations and hence mitigates IN from the received signal. The distinct performance improvement of this iterative IN mitigation module compared with conventional non-iterative IN mitigations is demonstrated in simulation results shown in Section 3.4.4. In addition, it is verified that PLC system with IN-EC based on the thresholding IN detection method outperforms that of the sorting IN detection method.

4.2 Suggested Future Research Directions

To further improve the data communication reliability of practical PLC systems or wireless systems in an impulsive environment, the following research directions will be

helpful:

1. In practical PLC systems, especially the indoor PLC system, several electric appliances are plugged in the system. Thus, users randomly turn up and down these appliances, e.g., television, water heater or washing machine, which induces various time diverse characteristics. Thus, to cope with a more realistic PLC, future work should consider the time-varying characteristic of the PLC channel.
2. In the proposed algorithms for the IN-EC module, the parameters of the IN occurrence probability and the IN variance are required. However, in practice, these parameters may not be available. So the estimation of the parameters could be future work. Another interesting topic is to design non-parametric IN estimation approaches.
3. Compared with SC-FDTE, generalised approximate message passing based frequency-domain turbo equalisation has been proved to achieve significant performance gain with a slight sacrifice of complexity [49]. For this reason, novel approaches based on generalised approximate message passing are in prospect of achieving further performance improvement for PLC.

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