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Abstract

This paper proposes a new control strategy and a novel modulation technique for a grid-connected photovoltaic (PV) system using a single-phase five-level flying capacitor (FC) based active-neutral-point-clamped (ANPC) converter. The proposed modulator can control the FC voltage to follow the requested reference value and simultaneously generate the required ac output voltage regardless of the values of the dc capacitor voltages of the converter. By implementing this method, smaller values of dc-link and flying capacitors can be used even in applications that could experience ripple or transient in the capacitors voltage. In the grid-connected single-phase five-level ANPC, where the capacitors can experience pulsation power and dc-link balancing issues, the selection of the reference voltage value for the FC can play an important role to balance the average values of the dc-link capacitors voltage. The proposed new control strategy uses a new reference voltage for the FC to be applied by the new modulator to have an average balanced dc-link voltages as well as an ac output voltage with good power quality. Simulation studies demonstrate the effectiveness of the proposed modulation technique and control strategy even with using relatively small dc capacitors to produce high quality output voltage and current and maintaining an average balanced dc-link voltages.

Keywords

pv, system, converter, applied, voltage, dc, anpc, control, unbalanced, novel, strategy, five, single, phase, level, modulation, grid, connected

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Novel Modulation and Control Strategy for Five-level ANPC Converter with Unbalanced DC Voltage Applied to a Single-Phase Grid Connected PV System

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Abstract—This paper proposes a new control strategy and a novel modulation technique for a grid-connected photo-voltaic (PV) system using a single-phase five-level flying capacitor (FC) based active-neutral-point-clamped (ANPC) converter. The proposed modulator can control the FC voltage to follow the requested reference value and simultaneously generate the required ac output voltage regardless of the values of the dc capacitor voltages of the converter. By implementing this method, smaller values of dc-link and flying capacitors can be used even in applications that could experience ripple or transient in the capacitors voltage. In the grid-connected single-phase five-level ANPC, where the capacitors can experience pulsation power and dc-link balancing issues, the selection of the reference voltage value for the FC can play an important role to balance the average values of the dc-link capacitors voltage. The proposed new control strategy uses a new reference voltage for the FC to be applied by the new modulator to have an average balanced dc-link voltages as well as an ac output voltage with good power quality. Simulation studies demonstrate the effectiveness of the proposed modulation technique and control strategy even with using relatively small dc capacitors to produce high quality output voltage and current and maintaining an average balanced dc-link voltages.

Index Terms—Active-neutral-point-clamped (ANPC) converter, flying capacitor, multilevel converters, photovoltaic (PV) power system, pulse width modulation, voltage balancing.

I. INTRODUCTION

IN recent years, multi-level converters have been under research and development for several industrial applications [1]. One of new topologies of multilevel converters is a five-level active neutral point clamped (5LANPC) converter which was introduced by ABB to combine the flexibility of the multi-level floating capacitor converters with the robustness of NPC converters [2]. Recently, the proposed topology was commercialized for industrial motor drive applications and has been proposed for a 6 MVA wind power application [1], [3]. Fig. 1 shows a circuit of a single phase FC-based 5LANPC

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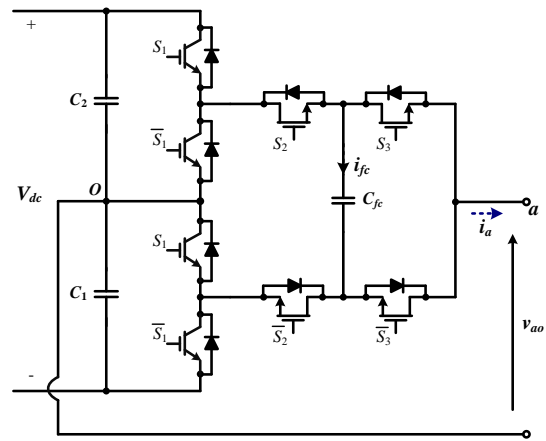


Fig. 1. Single-phase five-level ANPC converter

converter which can be used in low voltage applications. The redundancy in the switching states of the FC-based ANPC converter allows the voltage across FC to be regulated. To generate the switching pulses, a variety of strategies has been presented to generate the output voltage with reduced harmonics and simultaneously regulate the FC voltage of the converter such as Carrier-based PWM [4], modified triangular carrier-based PWM [5], selective harmonic elimination PWM (SHE-PWM) [6] and optimized pulse pattern [7]. The use of five-level vector PWM in three phase applications using switching redundancies to control FC voltages are presented in [8]-[10].

Although different techniques have been reported to control and generate switching pulses in the FC-based 5LANPC converter, virtually in all of the approaches, the dc-link capacitors are considered balanced or controlled to be balanced. But in some applications or under transient conditions, the dc-link capacitor voltages can experience voltage variation and become unbalanced. This paper presents a new approach to regulate the FC voltage to follow the requested reference voltage and produce the requested output voltage even when there is unbalance in the dc-link capacitor voltages. In addition, because of the specific structure of 5LANPC converter, a new

TABLE I
SWITCHING STATES OF THE FIVE-LEVEL ANPC CONVERTER

Switching states	S_1	S_2	S_3	Phase voltage V_{ao}	V_{ao} Symmetrical	FC Current i_{fc}
V_1	0	0	0	$-V_{C1}$	$-V_{dc}/2$	0
V_2	0	0	1	$V_{fc} - V_{C1}$	$-V_{dc}/4$	$-i_a$
V_3	0	1	0	$-V_{fc}$	$-V_{dc}/4$	i_a
V_4	0	1	1	0	0	0
V_5	1	0	0	0	0	0
V_6	1	0	1	V_{fc}	$V_{dc}/4$	$-i_a$
V_7	1	1	0	$V_{C2} - V_{fc}$	$V_{dc}/4$	i_a
V_8	1	1	1	V_{C2}	$V_{dc}/2$	0

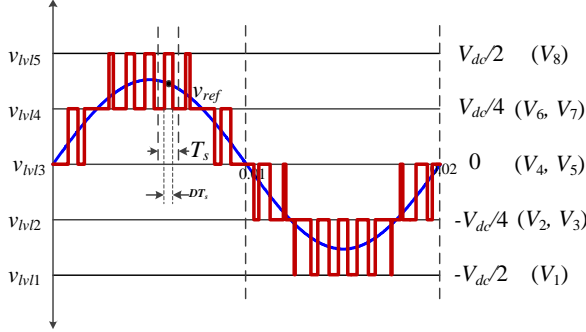


Fig. 2. Inverter PWM output voltage with redundancy in switching states to generate a sinusoidal output voltage

technique based on the ability to control the FC voltage is introduced to control the dc-link average voltage balancing while ripple can be in the capacitors voltage.

This paper is organized in the following way. In Section II, the operation principles of FC-based ANPC converter are presented. The FC-based ANPC converter control strategy to control the FC voltage and generate the requested output voltage using a new modulation technique is discussed in Section III. In Section IV, the issues related to a single-phase grid-connected 5LANPC converter is discussed. The performance evaluation of the proposed system is investigated under different operating conditions in Section V and finally conclusions are summarized in Section VI.

II. FLYING CAPACITOR BASED ANPC CONVERTER OPERATIONAL PRINCIPLES

The phase-leg of the five-level FC based ANPC converter is shown in Fig. 1. The dc-link consists of two capacitors each of which is rated at half of the dc-link voltage. This topology requires a flying capacitor per phase, the voltage of which should normally be one quarter of the dc-link voltage to generate uniform step levels at the output phase voltage as shown in Fig. 2. The outer switches (S_1, \bar{S}_1) operate at a lower switching frequency and should be able to withstand twice the voltage of S_2 and S_3 switches. In low-voltage power applications, insulated gate bipolar transistors (IGBTs) could be utilized for the outer switches and lower blocking voltage MOSFETs with higher switching capability can be used for (S_2, \bar{S}_2) and (S_3, \bar{S}_3) switches as illustrated in Fig. 1. The operation of the switch pairs (S_1, \bar{S}_1), (S_2, \bar{S}_2) and (S_3, \bar{S}_3) are complementary.

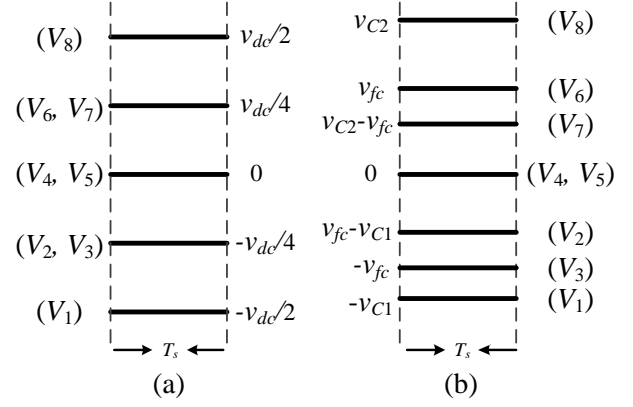


Fig. 3. Switching states and corresponding output voltage levels during a short time-step for (a) symmetrical voltage conditions, (b) unsymmetrical voltage conditions

The five-level FC-based ANPC converter consists of eight switching states which generate the different voltage levels at the output based on the capacitors voltages as shown in Table I. If the voltages across the dc-link capacitors are balanced and the voltage across FC is $V_{dc}/4$, five possible levels of the output voltage V_{ao} will be generated based on the different switching states as shown in Table I. In this case, some of the switching states are redundant in generating certain output voltage level. For example, V_6 and V_7 are redundant switching states to generate $V_{dc}/4$. Similarly (V_2, V_3) and (V_4, V_5) are redundant states to generate $-V_{dc}/4$ and 0 respectively. Although, the redundant switching states (V_2 and V_3), (V_6 and V_7) generate the same output voltage level, their affect on the FC voltage is opposite to each other due to the change in the direction of FC current. The ability to generate the same output voltage level with the opposite effect on FC voltage gives an opportunity to regulate the voltage across it. The rate of change of the voltage across FC can be expressed as:

$$\frac{d}{dt} v_{fc} = \frac{i_a}{C_{fc}} (S_2 - S_3) \quad (1)$$

Where S_2 and S_3 are equal to '0' when the switch is OFF and equal to '1' when the switch is ON.

In some applications, because of the limitations of the size of the dc-link capacitors, the dc-link could experience voltage variations. For example, in single-phase grid-connected applications, the dc-link power can have second harmonic ripple that will cause second harmonic ripple across the dc-link capacitor voltage. Also, dc-link voltage variations could be caused by applications where AC rectifier is used to provide the dc-link voltage for the converters.

Generally, the dc-link voltage can have voltage variation in steady-state, dynamic and transient conditions. In these conditions, capacitor voltages will not be symmetrical. (In this paper, a symmetrical condition is defined as $V_{C1} = V_{C2} = 2V_{Cf}$) This will result in V_{ao} having more than five different output voltage levels as illustrated in Table I. Further, the difference between the voltage levels are not equal. In this case, the switching states (V_2, V_3) and (V_6, V_7) would

not produce the same voltage level and the effect of these different voltage levels must be considered in the switching time calculations for the generation of the required output voltage. The resulting different voltage levels are illustrated in Fig. 3(a) and (b) for balanced and unbalanced conditions respectively for a specific time-step. In a balanced condition, the reference for FC voltage is usually set to be $V_{dc}/4$. However in an unbalanced condition, the reference for the FC voltage needs to be investigated. It can play an important role to balance the average values of the dc-link capacitor voltages as well as to control the output voltage harmonics. Different control techniques and strategies can be used to determine the reference value of FC voltage depending on the applications. For example, the FC reference voltage can be a fixed value regardless of the dc-link voltage variations or can be $(V_{C1} + V_{C2})/4$ or a value that can satisfy the application requirements.

III. PROPOSED MODULATION TECHNIQUE WITH FC VOLTAGE CONTROLLER FOR FIVE-LEVEL FC BASED ANPC CONVERTER

In this paper, a novel modulation technique is proposed to determine the appropriate switching states to be selected to generate the requested output voltage as well as controlling the FC voltage to the requested FC voltage during a sampling time both for balanced and unbalanced conditions. Adding FC reference voltage accompany with output reference voltage as input of the modulator which is able to follow them in variable and unbalanced dc-link voltage condition, will improve controlling ability of the five-level ANPC inverter system to be applied in variety of applications.

A. Basic Concept of the Averaging Technique

Generally, the average value of the output voltage, v_{o_s} , in each sample time T_s , can be expressed as in (2) which forms the basis of the modulation technique.

$$v_{o_s} = \frac{1}{T_s} \int_0^{T_s} v_{ao}(t) dt \quad (2)$$

In (2), $v_{ao}(t)$ is output switching voltage. Fig. 4 shows the reference requested waveform (v_{ref}) lies between two voltage levels v_{lvlx} and v_{lvly} and the resulting output voltage tracks the reference waveform based on (1). For illustration purposes, the reference requested waveform (v_{ref}) shown in Fig. 4 is assumed to be constant until t_C and then decreases linearly until t_D .

If the capacitor sizes are large enough, even though there is a voltage fluctuation across the capacitors, it can be assumed that the changes in the capacitors voltage during a sample time is neglected. Applying this assumption, the variations in the voltage levels v_{lvlx} and v_{lvly} shown in Fig. 4(b) are neglected and assumed to be v_{lvlx_s} and v_{lvly_s} during T_s . Therefore, (2) can be simplified to (3).

$$\begin{aligned} v_{ref_s} &= v_{o_s} = \frac{1}{T_s} \int_0^{T_s} v_{ao}(t) dt \\ v_{o_s} &= (1 - D_s)v_{lvlx_s} + D_s v_{lvly_s} \end{aligned} \quad (3)$$

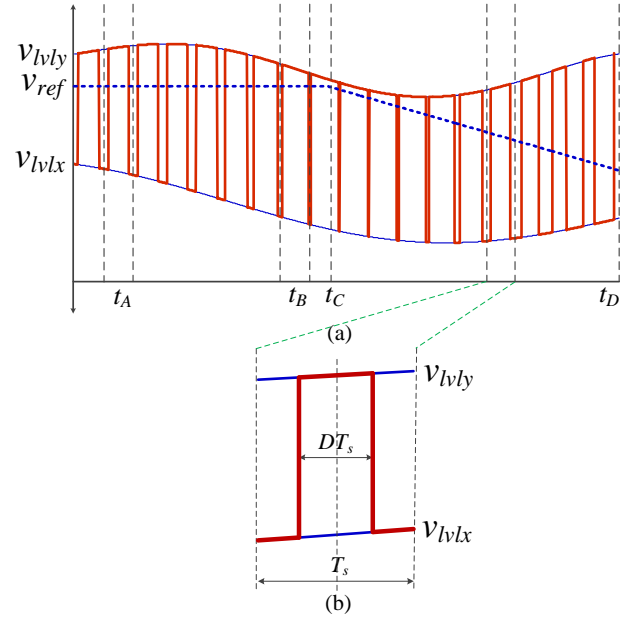


Fig. 4. Applying variable nearest voltages to generate PWM voltage to track the reference voltage

Generally, in order to generate v_{ref_s} from two different voltage levels v_{lvlx_s} and v_{lvly_s} in a specific duration time, the duty-cycle (T_s) can be determined from (3) as shown in (4).

$$D_s = \frac{v_{ref_s} - v_{lvlx_s}}{v_{lvly_s} - v_{lvlx_s}} \quad (4)$$

Fig. 4 illustrates the changes in the duty-cycle for different operating conditions. For example to generate the required output voltage during the time periods t_A and t_B , the duty-cycle is varied depending on the chosen voltage levels, v_{lvlx} and v_{lvly} , even though in this case, v_{ref} is a constant value.

B. Proposed Modulation Technique with FC Voltage Control

From Section III(A), the averaging method can be implemented to obtain the requested output voltage in a Five-level ANPC inverter. In Section II, the operational principles of a five-level FC based ANPC converter have been discussed for different voltage values across the three capacitors. In the symmetrical condition, the five different voltage levels can be utilized to generate the requested output voltage where some of them have redundancy in the switching state selection. For example when the output reference voltage is between $V_{dc}/4$ and $V_{dc}/2$, the switching states V_6 and V_8 or V_7 and V_8 can be utilized. To select which of these is to be used (V_6 or V_7), the main objective is to reduce the difference between the reference and the actual FC voltage. Based on (1), to regulate the FC voltage, the polarity of the output current must be considered in selecting the switching states V_6 or V_7 . When the polarity of the output current is positive, the selection of V_6 will cause the FC to be discharged and hence the voltage will be reduced while the selection of V_7 will cause the FC to be charged and hence the FC voltage will be increased.

Traditionally, the modulator only requires the output reference voltage as an input and the FC voltage is assumed to

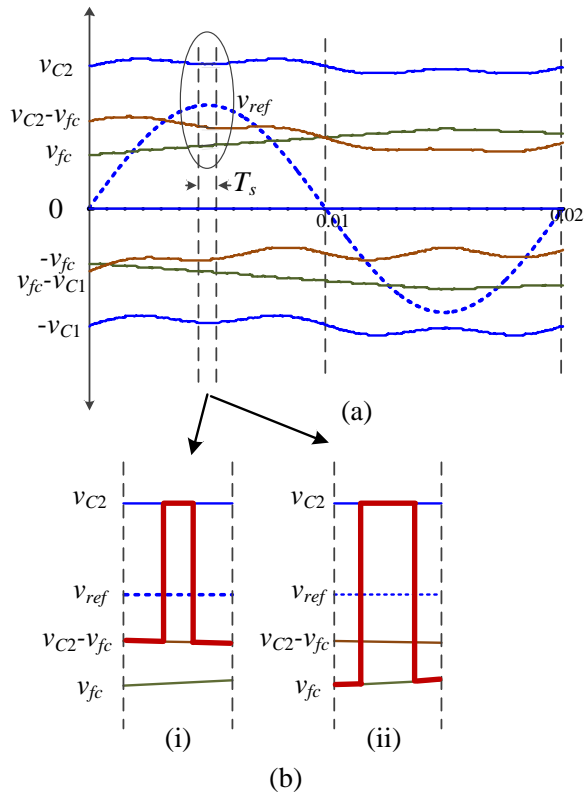


Fig. 5. (a) Applicable voltage levels to implement requested output voltage during a period under varying dc capacitor voltages (b) effect of selection of different voltage level on duty cycle during an special time-step to have same reference output voltage

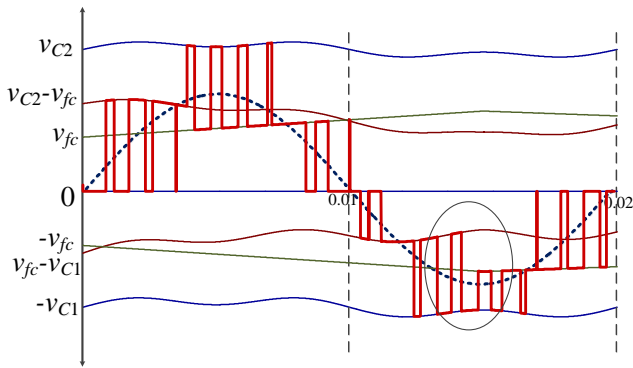


Fig. 6. Modulator selection of the appropriate voltage level under varying dc capacitor voltages to generate a sinusoidal output voltage

be regulated to $V_{dc}/4$ and during switching selection in the modulator, the dc-link capacitors are assumed to be balanced. However, in general, the value of the reference FC voltage has to be taken into account as described in Section II for balanced and unbalanced dc-link voltages. Therefore the modulator should have an additional input in the form of the reference FC voltage. This approach provides an improvement to the ability of the modulator and more flexibility for the control system.

Fig. 5(a) shows an operating condition where the capacitor

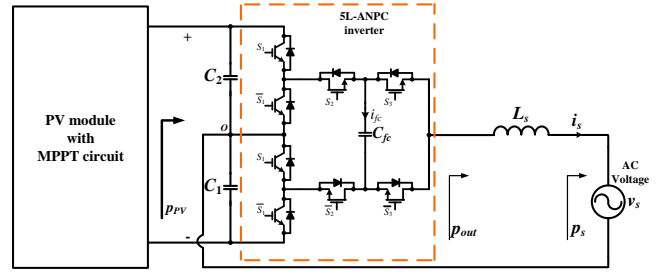


Fig. 7. A single-phase grid-connected PV system using Five-level ANPC converter

voltages are fluctuating and unbalanced. During the time step, T_s , shown in Fig. 5(a), eight different voltage levels are available to generate the required output voltage. Based on the averaging technique, the two nearest appropriate voltage levels need to be utilized to generate the requested output voltage. In this case, the voltage level V_{C2} is one of the appropriate nearest voltage levels. Even though the voltage level $(V_{C2} - V_{fc})$ is also one of the nearest voltage levels, it may not be the appropriate voltage level to select. A rule to determine the selection of the appropriate voltage level can be based on the effect it has on the FC voltage. For example, during a certain time step, if the actual FC voltage is less than the reference voltage, then the FC must be charged by selecting the appropriate switching state using (1). In (1), if the output current (i_a) is positive, the selection of the voltage level $(V_{C2} - V_{fc})$ will cause FC to be charged and if it is negative, the selection of voltage level (V_{fc}) will cause FC to be charged. Therefore, depending on the sign of (i_a), either the voltage level $(V_{C2} - V_{fc})$ or the voltage level (V_{fc}) need to be selected. The effect of the selection to generate the required output voltage will cause the duty cycle to be varied as shown in Fig. 5(b). Fig. 6 shows the modulator selection of the appropriate voltage level under varying dc capacitor voltages to generate a sinusoidal output voltage for a particular reference FC voltage and output current.

IV. SINGLE-PHASE GRID CONNECTED FIVE-LEVEL ANPC PHOTOVOLTAIC SYSTEM

A single-phase grid-connected PV system using a five-level ANPC inverter has the advantage of having high quality output voltages by using an optimal number of low voltage switches. One of the important issues in single phase application is the dc-link capacitor voltage ripple and balancing. In a three-phase three-wire application, the dc-link capacitor voltage balancing can be achieved by controlling the zero-sequence voltage of the inverter. But in the single-phase structure, because of effect on the output voltage, this technique is not applicable and in this case, the control of the flying capacitor voltage can play an important role in solving the problem.

A. Power and voltage ripple in the capacitors

Fig. 7 shows a single-phase grid-connected PV system using a five-level ANPC inverter. To analyze the system behaviour under steady-state conditions, it is assumed that the inverter operates with unity power factor with low current THD. Under

these conditions, the grid voltage and the inverter current are given by (5) and (6) respectively:

$$v_s = V_m \sin(\omega t) \quad (5)$$

$$i_s = I_m \sin(\omega t) \quad (6)$$

The power transmitted to the ac grid voltage is:

$$\begin{aligned} p_s &= v_s i_s = V_m I_m \sin^2(\omega t) \\ &= \frac{V_m I_m}{2} - \frac{V_m I_m}{2} \cos(2\omega t) \end{aligned} \quad (7)$$

and then inverter ac side power is:

$$\begin{aligned} p_{out} &= v_{out} i_s = (v_s + L_s di_s/dt) i_s \\ &= \frac{V_m I_m}{2} - Pr_m \cos(2\omega t + \phi) \end{aligned} \quad (8)$$

where

$$\phi = \arctan(L_s \omega I_m / V_m); Pr_m = \frac{I_m}{2} \sqrt{V_m^2 + (L_s \omega I_m)^2}$$

Based on (7) and (8), the power transmitted to the grid and power transferred from the ac side of inverter have the same dc value but different ac value. To investigate the operation requirements of the modulator and the control system, the dissipation of the inverter is assumed to be neglected and the PV modules and the maximum power point tracker (MPPT) circuit are assumed to transfer dc power to the dc side of the inverter, where the value is dependent on the PV modules and the sun irradiation. Therefore, when the system is in a stable condition, the output power from the PV modules with MPPT circuit, P_{PV} , shown in Fig. 7 must be equal to the dc part of p_{out} which is $V_m I_m / 2$. If the inverter dissipation is neglected, the difference between p_{out} and P_{PV} must cause the three capacitors of the inverter C_1 , C_2 and C_f to experience power ripple. The power ripple in a capacitor will produce voltage ripple across the capacitors as given in (10).

$$\frac{dW_{C_i}}{dt} = \frac{d}{dt} \left(\frac{1}{2} C_i v_{C_i}^2 \right) = p_{C_i} \quad (9)$$

$$dv_{C_i} = p_{C_i} \frac{dt}{C_i v_{C_i}} \quad (10)$$

This voltage ripple in the dc voltage of the capacitors in the conventional modulator will cause harmonics in the inverter output voltage. Furthermore, it can cause unexpected behavior on the control system action. One solution to reduce the ripple magnitude of the capacitor voltages is to increase the size of the capacitors. This will result in increased cost, size and weight of the system. Further it cannot solve completely the issues related to voltage ripple and also any transient on the capacitor voltages can produce unexpected transient on the output voltage and the system behaviour.

Also, in the grid-connected, single-phase five-level ANPC system, power ripple will not be shared between the capacitors simultaneously. As shown in Table I when the output voltage is positive, C_2 is transferring power to the output and when the output voltage is negative, C_1 is transferring the power, however, during the whole period, both capacitors are involved in receiving power from the PV circuit. Therefore, not only the dc-link capacitors have voltage ripple problems because

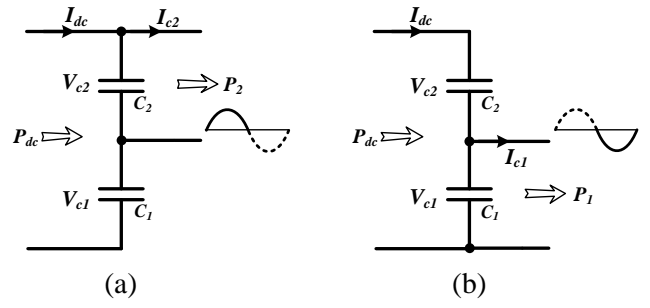


Fig. 8. Power transmission interaction of dc-link capacitors during two half cycle of the output voltage period for a three-level inverter or a five-level inverter with constant FC voltage

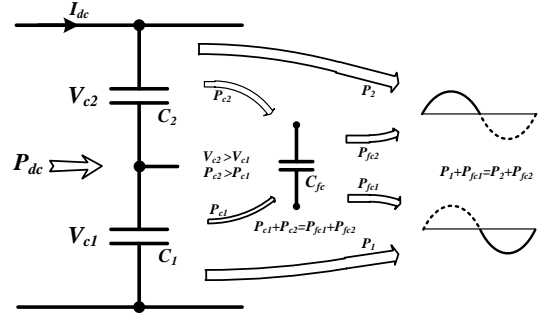


Fig. 9. Power transmission interaction of dc capacitors during two half cycle of the output voltage period for a five-level inverter to control dc-link balancing and having symmetrical output voltage

of their power ripple, but also they have different timing in their ripples which can produce instantaneous unbalancing of dc-link voltages. To reduce the effect of the dc voltage ripple on the output waveform, the proposed modulation technique in Section III can be used.

However, two issues still need to be considered, first is the phenomena of the possible divergence of the dc-link capacitor voltages and second is the selection of the FC voltage reference and its effect on the system.

B. Instability and Inherent Stability in The dc-link Voltages in Single-phase Three-level and Five-level ANPC Inverters

The unbalance in the dc-link capacitor voltage can be caused by issues such as the tolerance in the capacitor values, leakage currents, unequal switching losses, unsymmetrical switching, any transient in the system, unsymmetrical ac side current or improper control strategy.

The divergence of the dc-link voltage can be one of the major problems of a single-phase three-level and five-level ANPC inverters.

To explain the phenomena, a grid-connected three-level inverter is first discussed. In the three-level inverter, two capacitors C_1 and C_2 in Fig. 8 are involved in the power transmission activity. The average power transmitted from the dc-side P_{dc} to the ac-side is the sum of P_1 and P_2 . The power P_1 is related to the power transmitted to the ac-side through the capacitor C_1 which occurs during one half cycle of the inverter output voltage and P_2 is related to the other half cycle

of the inverter output voltage when the power is transmitted through C_2 . In the normal steady-state operation, regardless of the capacitors voltage, P_1 and P_2 must be equal to have two symmetrical half cycle currents. Therefore, under any balanced or unbalanced dc-link voltage or transient conditions, the modulator must produce a symmetrical output voltage to ensure sinusoidal current in the ac side. However, traditional modulators will normally assume balanced dc-link capacitor voltages to produce the symmetrical output voltage. If the capacitor voltages are unbalanced, an unsymmetrical output voltage will be produced, depending upon to the values of the unbalanced capacitor voltages. This behaviour will produce distortion in the ac side current, however this can help to produce inherent dc-link balancing ability, because when the capacitor with the higher voltage transfers higher power to the output, the capacitor voltage will automatically decrease more than that of the capacitor with the lower voltage.

But if the modulator is designed to produce a symmetrical output voltage in an unbalanced dc-link voltage condition (V_{c1} not equal to V_{c2}), P_1 and P_2 will be equal and hence I_{c1} and I_{c2} will be different. If the input current from the dc-side is considered to be constant during the period, the capacitor with the higher voltage will now have lower average output current compared to the capacitor with the lower voltage. This will lead to the divergence of the two capacitor voltages, with the voltage of the higher voltage capacitor increasing higher and higher and the voltage of the lower voltage capacitor decreasing lower and lower.

This phenomena can also occur in a single-phase five-level ANPC inverter when the FC voltage is controlled to be a constant value and acts only as an intermediary for the power transfer from the dc-link capacitors to the ac side of the inverter.

Fig. 9 shows the power flows of a single-phase five-level ANPC inverter where V_{C_2} is greater than V_{C_1} . To produce a symmetrical output voltage, $P_2 + P_{fc2}$ must be equal to $P_1 + P_{fc1}$. Since the FC voltage is controlled to have a constant value, during the positive cycle of the output voltage, P_{fc2} is equal to P_{c2} and during next half cycle, P_{fc1} is equal to P_{c1} . Therefore, $P_2 + P_{c2}$ (from capacitor C_2) must be equal to $P_1 + P_{c1}$ (from capacitor C_1). Hence, similar to the single-phase three-level inverter, there will be divergence in the two capacitor voltage values.

However, in single-phase or three-phase applications of a five-level ANPC inverter, it is possible to take advantage of the flying capacitor to control the balancing of the dc-link capacitors, if the FC voltage does not have to be controlled to a constant value and the FC is allowed to be charged or discharged as required during a cycle of the output voltage. To control the voltage balance in the dc-link capacitors, the capacitor C_2 should transfer higher power ($P_2 + P_{c2}$) than that from the capacitor C_1 ($P_1 + P_{c1}$) to reduce the voltage unbalance in the dc-link capacitors. This can be achieved by not controlling the FC voltage to a constant value. P_{c2} can be controlled to be higher from P_{fc2} causing the FC voltage to rise. The excess power stored in the FC can be used in the next half cycle to help C_1 to generate the output power ($P_1 + P_{fc1}$),

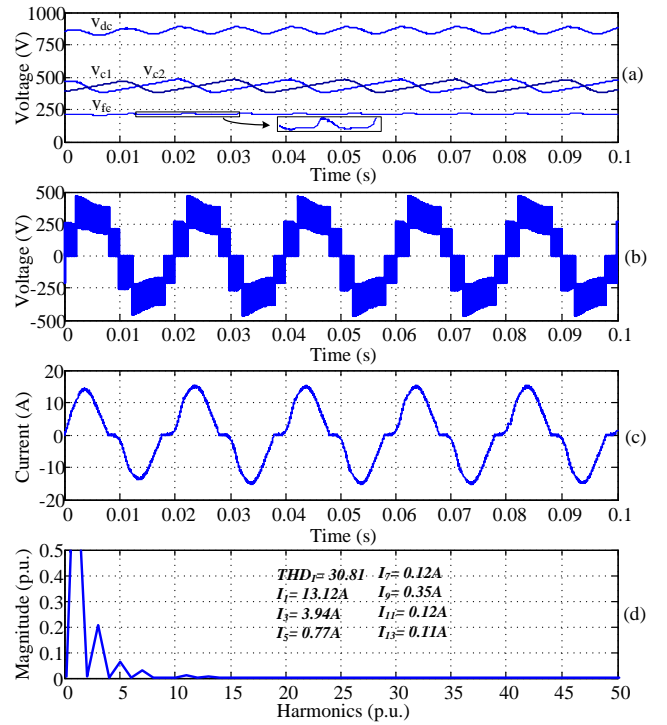


Fig. 10. Results of applying conventional modulation technique with dc-link capacitors equal to $300\mu f$: (a) dc-link voltage, dc-link capacitors voltage, FC voltage (b) inverter output voltage (c) Inverter output and ac grid current (d) magnitude of current harmonics in pu.

which causes the FC voltage to reduce to its original value at the end of the cycle. In this way, the capacitor C_2 will transfer higher power than capacitor C_1 leading to the desired voltage balance in the dc-link capacitors.

This can be implemented by the new modulator which can control the output voltage to be symmetrical regardless of the values of capacitor voltages. In this paper, we propose that the FC reference voltage of the new modulator has to be selected to follow $V_{C_2}/2$ during the positive cycle of the output reference voltage and then to follow $V_{C_1}/2$ during the negative cycle of the output reference voltage. In the balanced dc-link voltage condition when V_{C_1} is equal to V_{C_2} then the defined reference voltage for FC will be equal to $V_{dc}/4$.

V. PERFORMANCE EVALUATION AND SIMULATION RESULTS

A simulation has been carried out using MATLAB/Simulink to verify the effectiveness of the proposed modulator and control technique for the five-level ANPC inverter application for a single-phase grid-connected PV system. The simulation is based on Fig. 7 and it is assumed that the PV modules and the MPPT circuit transfer a constant power to the dc-side of the inverter regardless of the variation on the dc-link voltages of the inverter assumed to be between 700V to 1000V. The value of transferred power from the MPPT circuit is depend on power available from the PV and can varied for different sun irradiation. During 100 ms simulation, it is considered to be constant and equal to 2kW. In Fig. 7, the AC grid voltage

(V_s) is 240V and the series inductor L_s is 4.8mH. The control system is designed to transfer the PV power to the AC grid with unity power factor. The simulations have been carried out for both the conventional and the proposed modulator with different values of dc-link capacitors. To investigate the effectiveness of the proposed modulator and control strategy on balancing of the dc-link capacitor voltages, the simulations are carried out using a constant value of FC reference voltage as $V_{dc}/4$ and using the proposed technique of setting the reference FC voltage as $V_{C_2}/2$ during the positive cycle of the output reference voltage and as $V_{C_1}/2$ during the negative cycle of the output reference voltage. The flying capacitor value is $500\mu F$. The sample time (T_s) is $50\mu s$ representing a 20KHz output switching frequency.

Fig. 10 shows the simulation results of the system using the conventional multi-carrier modulation technique to generate the inverter switching signals. The conventional modulator applies the average of the dc voltage to generate a per-unit reference waveform to be applied for conventional modulation technique. To investigate the effect of the value of the capacitor, initially the dc-link capacitor values is set as $300\mu F$ to examine the quality of the output voltage and inverter current using a small dc-link capacitors. The FC reference voltage in the simulation is set equal to one-quarter of the dc-link voltage. Fig. 10(a) shows the dc-link voltage V_{dc} , the dc-link capacitor voltages V_{C_1} and V_{C_2} and the flying capacitor voltage V_{fc} . Fig. 10(a) shows that the voltage of V_{dc} varies by around 100V and the variation of each dc-link capacitor voltage is around 150V, which is a significant variation. Fig. 10(b) shows the five-level output of the inverter voltage waveform where each output level follows the variation in the dc capacitor voltages accompanied by the high frequency switching pulses. Fig. 10(c) shows the inverter output current which contains harmonics due to the ripple in the dc capacitor voltages shown in Fig. 10(a). The spectrum of the inverter current harmonics is shown in (d), showing that most of the harmonics of the inverter current are 3rd, 5th and 7th and the total harmonic distortion (THD) is 30.81%, which is quite significant.

The traditional solution to reduce the dc voltage ripple problem is to increase the size of dc-link capacitors. This will result in the improvement of the output current quality. To test this, the dc-link capacitor values are both now increased to 10 times their original value ($3000\mu F$). Fig. 11 illustrates the results of the simulation using the same modulation technique and FC reference voltage as in the previous simulation. Fig. 11(a) shows the dc-link voltage V_{dc} , the dc-link capacitor voltages V_{C_1} and V_{C_2} and the flying capacitor voltage V_{fc} . Fig. 11(a) shows that the variation in all voltages are reduced. To demonstrate that there is still ripple in the capacitor voltages, a small section of each graph is zoomed to show this. Fig. 11(b) shows the five-level inverter output voltage waveform showing that the reduced variation in the capacitor voltages are reflected in the reduced variation in each output level. Fig. 11(c) shows the inverter current with improved waveform quality and reduced harmonic content as shown in Fig. 11(d) where the THD is now only about 2.1% and third harmonic current magnitude is about 2.07% and the other harmonic currents are negligible in

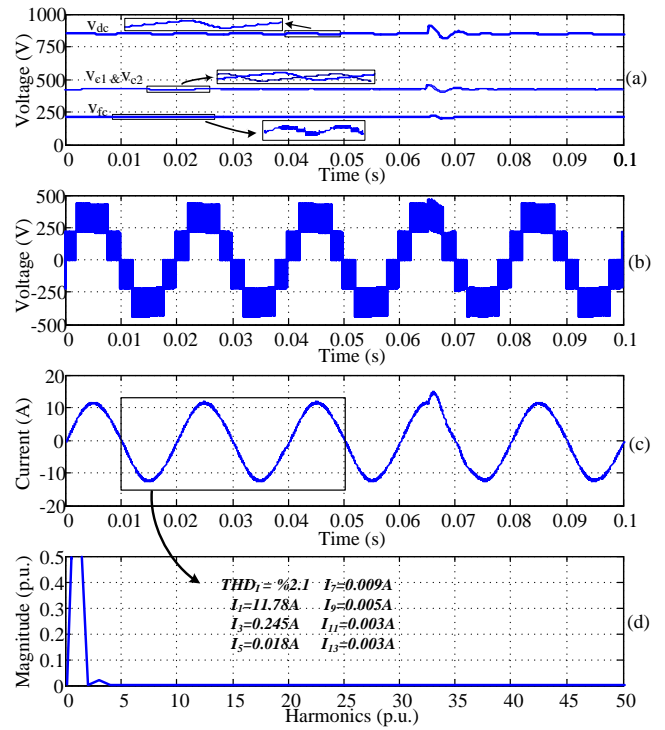


Fig. 11. Results of applying conventional modulation technique with dc-link capacitors equal to $3mf$: (a) dc-link voltage, dc-link capacitors voltage, FC voltage (b) inverter output voltage (c) Inverter output and ac grid current (d) magnitude of current harmonics in pu.

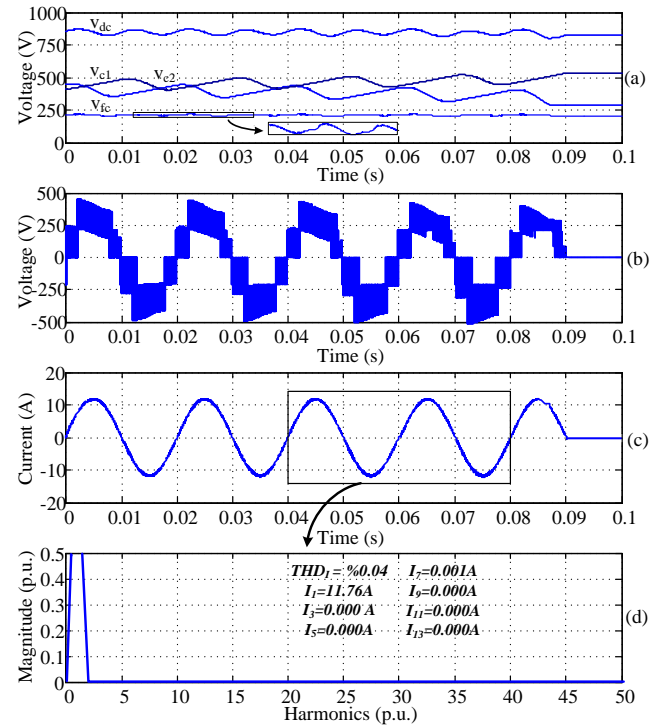


Fig. 12. Results of applying proposed modulation technique with dc-link capacitors equal to $300\mu f$ and FC reference voltage equal to $v_{dc}/4$: (a) dc-link voltage, dc-link capacitors voltage, FC voltage (b) inverter output voltage (c) Inverter output and ac grid current (d) magnitude of current harmonics in pu.

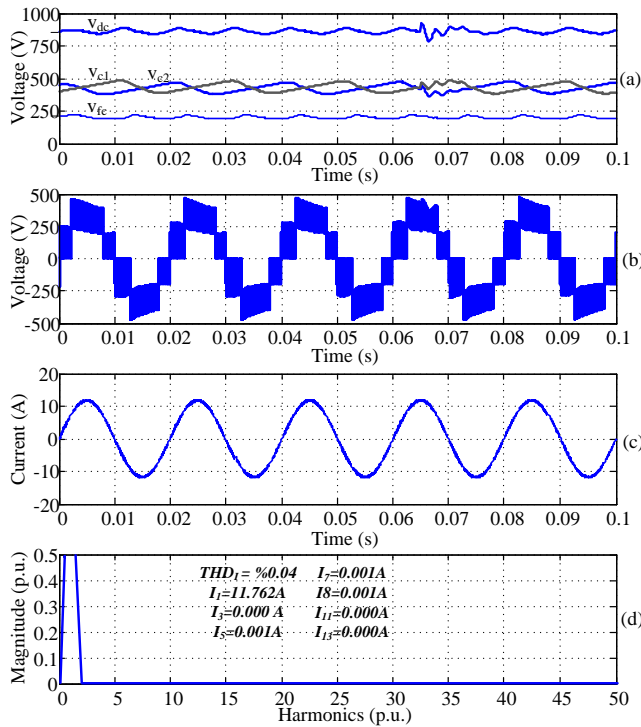


Fig. 13. Results of applying proposed modulation technique with dc-link capacitors equal to $300\mu f$ and FC reference voltage equal to half of engaged dc-link capacitor in each output half cycle: (a) dc-link voltage, dc-link capacitors voltage, FC voltage (b) inverter output voltage (c) Inverter output and ac grid current (d) magnitude of current harmonics in pu.

value. However, any transient in the dc-link capacitor voltages, as shown in Fig. 11(a) at $t = 65$ ms can cause the inverter current in Fig. 11(c) to be distorted and therefore has higher harmonic content.

To demonstrate the effectiveness of the proposed modulator to reduce the effect of the dc voltage ripple on the output current waveform, the dc-link capacitors are returned back to the lower value of $300\mu F$ and the FC reference voltage is set to be equal to one-quarter of the dc voltage. Fig. 12(a) shows the dc voltage V_{dc} , the dc-link capacitor voltages V_{c1} and V_{c2} and the flying capacitor voltage V_{fc} . Fig. 12(a) shows that V_{dc} still varies by around 100V as before. Fig. 12(b) shows the five-level output of the inverter voltage waveform where each output level follows the variation in the dc capacitor voltages accompanied by the high frequency switching pulses as previously, however the inverter output voltage has been modified in its switching time as mention in III(A). This will result in a much cleaner inverter output voltage as shown in Fig. 12(c), and much reduced harmonic content and THD as shown in Fig. 12(d) where the THD of inverter current is now only 0.04%. However, Fig. 12(a) also shows that the average voltage of V_{c1} is increasing while the average voltage of V_{c2} is decreasing which indicates that the system has dc-link voltage divergence problem. When the divergence reaches an unacceptable level, the control system turned the inverter off after 90 ms. To demonstrate the effectiveness of the proposed method of varying the reference FC voltage in

the the modulator to solve the problem of capacitor voltage divergence in the previous simulation, the dc-link capacitors remains at their low value $300\mu F$ and the FC reference voltage of the new modulator has to be selected to follow $V_{C2}/2$ during the positive cycle of the output reference voltage and then to follow $V_{C1}/2$ during the negative cycle of the output reference voltage as given in Section IV(B). Fig. 13(a) shows dc voltage V_{dc} , dc-link capacitors voltage V_{c1} and V_{c2} and flying capacitor voltage V_{fc} . Fig. 13(a) shows that V_{dc} still varies by 100V as before, however the divergence problem has now been solved, while achieving a clean current waveform as shown in Fig. 13(c). Fig. 13(d) shows that the THD is very good and is around 0.04%. Further, a transient in the dc-link capacitor voltages as shown in Fig. 13(a) at $t = 65$ ms does not cause the inverter current in Fig. 13(c) to be distorted.

VI. CONCLUSIONS

A novel modulation and control strategy for a five-level FC based ANPC converter has been presented. A theoretical framework of a novel extended modulation technique for unsymmetrical and symmetrical voltage conditions of a five-level ANPC converter has been proposed. The application of the proposed modulation and control strategy, for a single-phase grid-connected PV system using a five-level FC based ANPC converter to produce ac output voltages with good power quality under both symmetrical and unsymmetrical condition, has been investigated. Issues related to the balancing of dc-link voltages and its associated problems are discussed and a new control strategy has been introduced to solve the dc-link voltage divergence problem. The proposed strategy is applicable for other applications of the five-level FC-based ANPC converter. The effectiveness of the proposed modulation technique and control strategy was demonstrated by the simulation results, demonstrating the ability of the system to operate properly using smaller size of dc-link capacitors to produce ac output voltage and current with good power quality even under transient condition.

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