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CMOS-APS for HEP applications: Design and test of innovative architectures

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Abstract

A set of innovative active pixel architectures has been conceived and implemented in standard CMOS technology. Active circuits are introduced into the pixel, to increase S/N ratio and to perform basic signal processing. Testing of such devices, however, becomes critical, due to the circuit relative complexity and to the need of accurately evaluating timing and position of the impinging radiation. A test strategy has thus been devised, exploiting a NIR laser source, which has been carefully characterized and tuned. The NIR laser allows for emulating, in a much more controllable fashion, a MIP event. This allow for validation of novel pixel architectures proposed and, more generally, of the whole design flow. © 2005 IEEE.

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Alessandro Marras, Daniele Passeri, Pisana Placidi, Guido Matrella, Marco Petasecca, Leonello Servoli, Gian Mario Bilei and Paolo Ciampolini

***Abstract*– A set of innovative active pixel architectures has been conceived and implemented in standard CMOS technology. Active circuits are introduced into the pixel, to increase S/N ratio and to perform basic signal processing. Testing of such devices, however, becomes critical, due to the circuit relative complexity and to the need of accurately evaluating timing and position of the impinging radiation. A test strategy has thus been devised, exploiting a NIR laser source, which has been carefully characterized and tuned. The NIR laser allows for emulating, in a much more controllable fashion, a MIP event. This allow for validation of novel pixel architectures proposed and, more generally, of the whole design flow.**

I. Introduction

STANDARD submicrometer CMOS technology is attractive for the fabrication of semiconductor radiation detectors. With respect to more conventional approaches, it allows for higher spatial resolution, lower power consumption, more effective integration of active circuitry and lower manufacturing cost. However, it implies worse charge collection performance and potentially higher design cost.

In recent works [1,2,3] design and fabrication of CMOS-APS detectors was discussed, aimed at high-energy physics applications. The choice of standard CMOS fabrication process allows for smart detectors to be conceived: efficient active circuitry can be implemented on the sensor chip, allowing for compensating the inherently low charge collection efficiency and for implementing on-chip signal processing capabilities. In this summary, we suggest some possible improvement of active pixel architectures, based on further exploitation of active pixel circuitry. Advanced microelectronics allow for pixel-size shrinking, which, in turn, fosters better spatial resolution properties. Smaller pixels, however, together with more complex read-out circuitry, makes chip testing more demanding. We therefore also discuss techniques which have been devised for testing the radiation-sensitive, active-pixel chips.

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II. Physical Simulation and Protoypes

As mentioned above, standard CMOS processes do not allow for the fabrication of highly efficient photodiodes aimed at charge collection purposes, since low supply voltages and low-resistivity substrates prevent large volumes from being depleted. Unless a relatively thick, low-doped epi-layer is available, the collected-charge budget, for a Minimum Ionizing Particle (MIP) crossing, can be as low as 1000 electrons, leading to very small voltage swing at the cathode.

Dark-current noise, charge-collection efficiency and output signal dynamic depends on the actual geometry in a non-trivial fashion. Device simulation (ISE-TCAD Dessis simulator [4]) was exploited to select the technology process (among those commercially available) suitable for MIP detection, and to optimize the sensitive element geometry (Fig. 1).

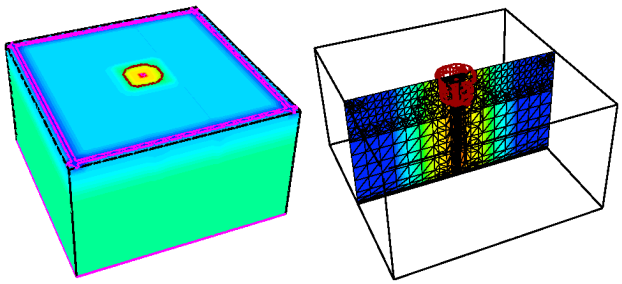

Fig. 1. 3D device simulation: photodiode doping profile (left)and electron distribution after a MIP crossing (right). The photodiode junction is highlighted

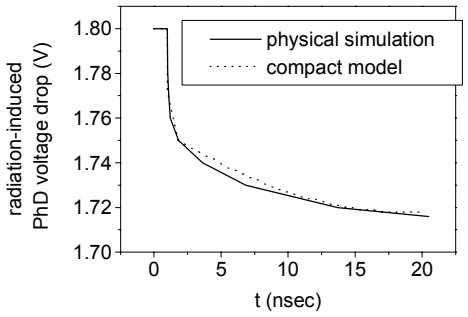

Fig. 2. Comparison between pixel responses predicted at physical level and at circuit level for a MIP crossing. A satisfactory agreement is achieved.

A compact circuit model for the photodiode was conceived and parametrized, based on DESSIS results, and simulation of

large detector arrays were performed in a Cadence/Spectre environment (Fig. 2).

Due to the small charge budget made available by the hit of a Minimum Ionising Particle (MIP), the careful control of parasitic devices and the actual sizing of sensitive area are of the utmost importance, in order to optimize charge-collection and noise properties.

Based on device simulation results, UMC 0.18µm CMOS fabrication process was validated. Such a technology features 6 metal and 1 polysilicon layer; it provides no epitaxial layer and the supply voltage is limited to 1.8V. The substrate is therefore far from being fully depleted; simulations [5],[6] show that the effective charge collection is practically limited to a sensitive volume which is about ten micrometers deep.

Two prototype chips have been designed and fabricated in a MPW framework (Fig. 3); chips include traditional APS structures, as well as more elaborated pixel architectures.

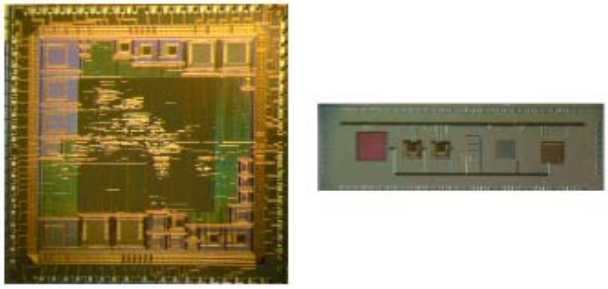

Fig. 3. RAPS01 prototype (left) and RAPS01 prototype (right)

III. Innovative Architectures

A high-gain, in-pixel amplification structure can be useful to preserve a satisfactory S/N ratio: the amplified pixel output signal can also be readily exploited for processing purposes.

The pixel scheme shown in Fig. 4 has been devised and investigated; the small voltage swing at the photodiode cathode drives a high-gain, on-pixel CMOS amplifier, which, in turn, drives a source-follower buffering stage.

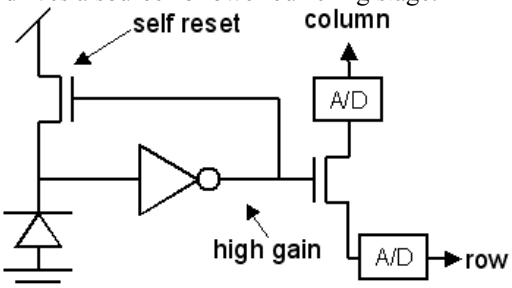

Fig. 4. Schematics of a self-resetting, high-gain pixel, suitable for asynchronous readout.

The sensor array acts as a switch matrix, in which column- and row-lines are opportunely precharged at complementary values. As soon as a pixel is hit, its output turns on the switch so that charge sharing between row and column lines occurs, allowing for asynchronous detection of *x*-*y* hit coordinates.

An additional advantage comes from the availability of a positive pulse at the amplifier output of the hit pixel, which can be straightforwardly fed back to drive the photodiode reset transistor. So doing, a self-triggered reset can be carried out, and fully asynchronous operating mode is attained, with no need of periodic reset signals [7].

The corresponding layout view, requiring a 10µm x10µm silicon area, is shown in Fig. 5.

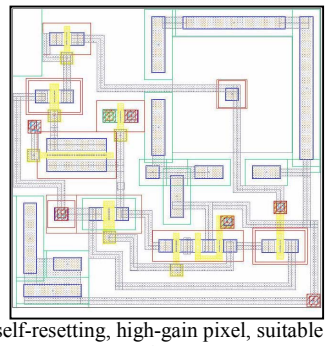

Fig. 5. Layout of a self-resetting, high-gain pixel, suitable for asynchronous readout.

Following the same guidelines, different features can be integrated at the pixel level: the circuit shown in Fig. 6, along with a possible layout (Fig. 7), implements Correlated Double Sampling (for Fixed Pattern Noise (FPN) and kTC noise suppression). In the given circuit, the capacitor is charged at dark output voltage, just after the reset phase, by turning on M_a and M_b transistors. Then, at the read phase, just M_a is turned on, so that the capacitor retains its voltage and the signal at the gate of the ouput stage transistor is the difference between the two sampled values.

Power dissipation is limited by active power switching, by using additional control transistors shown in figure.

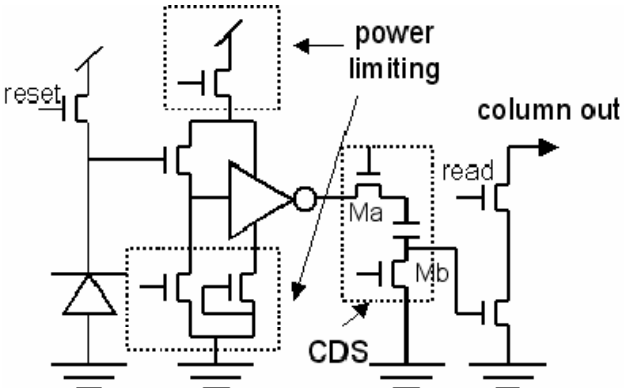

Fig. 6. Schematics and layout of a high-gain pixel capable of in-pixel Correlated Double Sampling

Pixel layout has been optimized by means of device simulation, aiming at minimizing charge losses due to parasitic junctions. Although a large number of active device is used, the pixel area is still limited to 10 µm x 10 µm.

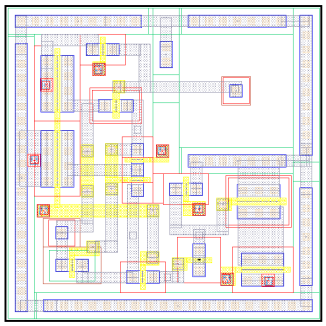

Fig. 7. Layout view for pixel with internal CDS.

Simulated responses are illustrated in Fig. 8: for the first pixel architecture, the row/column controlled current is shown, whereas the output voltage shift is reported for the other. In both cases, parasitic junctions do not compromise responses, regardless of the actual hit position. Simulations have been carried out, accounting for variable particle-hit positions, allowing toestimate a spatial resolution of 2.6 µm, far below the pixel pitch.

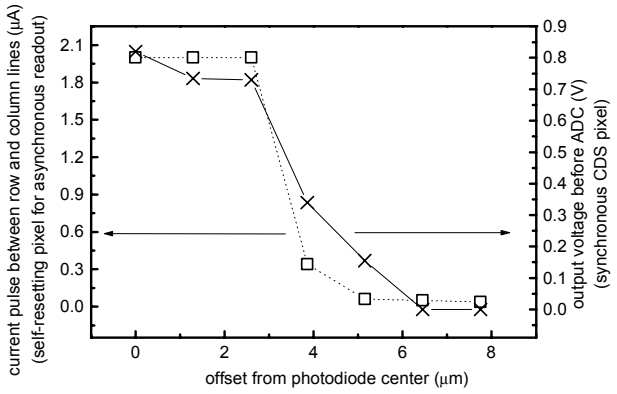

Fig. 8. Simulated performances for both structures before ADC.

IV. Measurements

RAPS01 and RAPS02 chips [3], [7] include several active pixel arrays, featuring different architecture variants. Although primarily aimed at MIPS detection, spatial resolution properties of such chips can be efficiently characterized by means of a laser optical beam. By using a pulsed infrared laser source, indeed, beam position and synchronization issues can be more easily dealt with. On the other hand, laser intensity should be carefully calibrated to approximate the ionization track produced by a minimum ionization particle [8], accounting also for optical reflection losses and refraction. Simulations have been carried out to validate the MIP emulation.

In order to cope with these issues, an optical test-bench has been designed and fabricated. It features a mechanical movement section with sub-micrometer positioning capabilities (repeatability of positioning: 0.2 µm) and an optic axis with a beam-splitter. This allows for the focalisation of the beam (Near InfraRed laser for the irradiation), as well as for obtaining a control image of the irradiated domain.

The characterization of the laser source was made by comparing the response of different sensitive devices, in particular a single, lumped-element photodiode and microstrip detectors. The optical test bench is reported in Fig. 9.

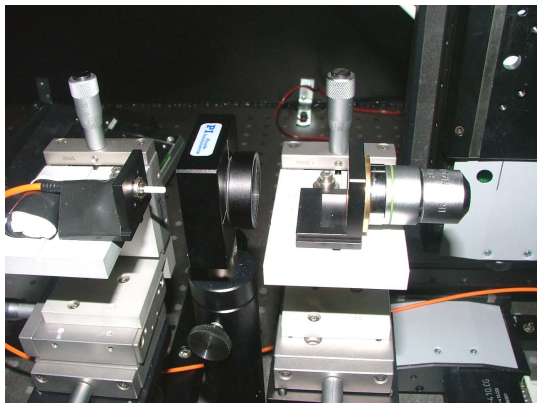

Fig. 9. Optical test bench.

A first test was carried out in order to determine the laser spot size; to this purpose, the output of a single pixel was monitored while moving the laser source by single steps of 1 µm. This procedure allowed for the reconstruction of the spatial optical power distribution reported in Fig. 10.

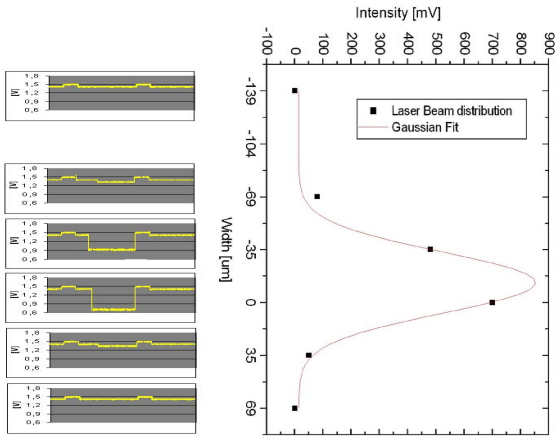

Fig. 10. Spatial optical power distribution.

The standard deviation of the gaussian fit can be assumed as a measure of the effective spot diameter. A 40 µm-wide laser spot has been obtained in the illustrated case. Then, spatial resolution of the detector has been evaluated, by comparing outputs of different adjacent pixels. Fig. 11 shows the response of a 4x4 subset of pixels (featuring a 14µm pitch) and demonstrates how a significant discrimination among pixel can be obtained. This is due to the relatively shallow sensitive layer, which prevent generated charge from spreading too far from the hit site. I.e, charge diffusion does not significantly affect micrometric resolution.

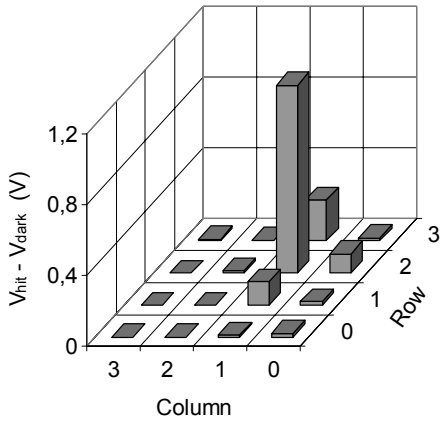

Fig. 11. Response of a 4x4 subset of pixels.

V. CONCLUSIONS

In conclusion, a set of innovative active pixel architectures has been conceived and implemented in standard CMOS technology. Active circuits are introduced into the pixel, to increase S/N ratio and to perform basic signal processing. Testing of such devices poses severe problems, due to the circuit relative complexity and to the need of finely controlling timing and position of the impinging radiation. test strategy has thus been devised, based on a NIR laser source, which has been carefully characterized and tuned, in order to emulate, in a much more controllable fashion, a MIP event. This allow for validation of novel pixel architectures proposed (actual test is under way) and, more generally, of the whole design flow.

Thanks to the flexibility of the optical test bench and to configurability options of the circuits, also perspective applications of the devices, different from HEP applications, can be evaluated.

I.e.., simulations and some preliminary tests show that the sensor should provide appreciable responses even to different radiation sources, which could be useful for microimaging applications.

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