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Design and development of a 3-Phase saturated core high temperature superconducting fault current limiter

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DESIGN AND DEVELOPMENT OF A 3-PHASE SATURATED CORE HIGH TEMPERATURE SUPERCONDUCTING FAULT CURRENT LIMITER

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Abstract—**The occurrence of fault currents and system sensitivity to fault currents are both increasing in modern power systems. Along with extensive damage to network hardware, considerable consumer losses (due to network unavailability) can result from fault current events. One device that is designed to reduce the impact of fault currents and increase network availability is the Fault Current Limiter (FCL). This paper describes the design and development of a 3-Phase saturated core High Temperature Superconducting (HTS) FCL. This particular type of FCL exhibits negligible power losses during the un-faulted state and also provides instantaneous reaction and recovery during fault events. Optimisation of the design parameters for this device is discussed in this paper. Characterisation results from experimental cores and analyses using the finite element method are also discussed in terms of the design process. Finally, the performance of a prototype 3-phase device is experimentally characterised.**

I. Introduction

The increasing demands placed on modern power grids, along with changes in infrastructure and the introduction of newer technologies into grids, have led to increases in both the occurrence of fault currents and the sensitivity of network equipment to fault currents [1], [2]. Recent power failures, such as those in Auckland New Zealand (1998, 2006 and 2009), North America (2003), Malaysia (2005) and Sydney Australia (2009), illustrate the vulnerability of modern electrical networks. This vulnerability is also predicted to increase as further devices associated with renewable energy sources (such as sources dependent on wind and sunshine) are continually added to electrical networks [1], [2]. While electrical faults can cause quite severe and costly damage to network hardware, consumer losses due to network unavailability are often much higher. In the USA alone it has been estimated that the cost of power interruptions to consumers could be as high as $135 billion per annum [3]. One class of device that is designed to both protect and improve the availability of electrical networks is the Fault Current Limiter (FCL).

FCLs ideally provide high transient fault impedance for limiting the amplitude of fault currents, while imposing negligible steady state un-faulted AC terminal impedance. There are several different FCL technologies that have recently attracted research attention including solid state FCLs [4], superconducting resistive FCLs [5], [6], and saturated core superconducting FCLs [7], [8]. Solid state FCLs rely on solid state switches to control the fault current (usually IGBTs) and have a very low un-faulted impedance, but suffer from high steady state power losses due to the power electronics. Superconducting resistive FCLs rely on quenching of the superconductor to limit fault currents. In other words, the fault current drives the device out of the superconducting state, which results in a rapid increase in impedance and provides fault current limiting. These devices have negligible un-faulted impedance; however, they suffer from slow recovery. In comparison, saturated core superconducting FCLs are designed such that the superconductor is de-coupled from the high voltage source. Hence, there is no quenching of the superconductor during a fault and recovery is instant.

Saturated core FCLs have existed as a concept since the late 1970s [9]; however, significant research and development on these devices did not begin until after the discovery of High Temperature Superconductors (HTS). In a saturated core FCL the change in permeability between saturated and unsaturated states of the steel core is utilised to simultaneously provide a low steady state un-faulted AC terminal impedance and high transient fault impedance (for current limiting). The role of the superconducting coil is simply to bias the core into saturation. Hence, power losses during the un-faulted state are negligible, fault reaction and recovery are instant, and the superconductor is protected from the high fault currents.

This paper presents the design and development details of a 3-phase saturated core FCL. Characterisation results from experimental cores, including the single-phase prototype system (described in [7] and [8]), and finite element analyses are discussed in terms of the 3-phase system design process. Optimisation of the design parameters is also discussed. The performance of a prototype 3-phase device is then experimentally characterised in terms of DC saturation, steady state performance and fault current limiting ability.

II. System Design

A. Principles of a Saturated Core FCL

In discussing the principles of operation of any FCL device it is convenient to introduce the concepts of *insertion impedance* and *fault impedance*. For the purpose of this

discussion, insertion impedance is defined as the AC terminal impedance (of any FCL device) during normal un-faulted conditions. The manner in which the impedance increases during a fault is typically device dependent; however, for most FCL technologies the increase is continuous and not as a step function. Hence, fault impedance is best defined as the steady state equivalent impedance that would result in the same fault current limiting effect. As discussed in Section I, the saturated steel core FCL meets the fundamental FCL requirements of a low insertion impedance and high fault impedance through the change in permeability between saturated and unsaturated states of the steel core. This concept can be demonstrated through an analysis of the magnetisation properties of typical steel core material. As an example, consider the properties of M3 laminated electrical steel shown in Figure 1.

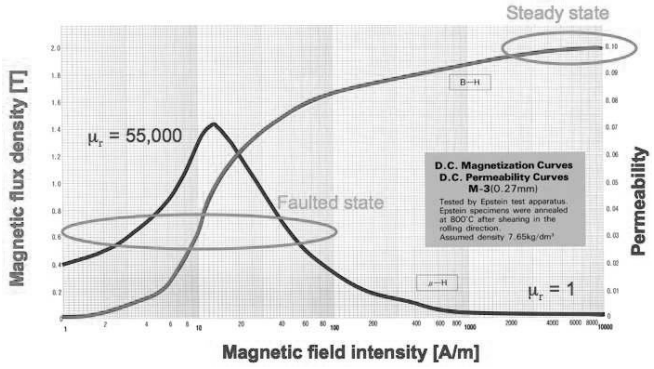

Figure 1. Material Properties of M3 Laminated Steel

In a saturated core FCL a DC current carrying winding is used to bias the core. The number of ampere-turns supplied by the biasing winding need to be high enough to sufficiently saturate the core. A separate winding is then used to carry the normal AC load current. During steady state un-faulted conditions the low current in the AC winding results in the flux density oscillating through a minor loop and not the full B-H loop. The top right hand corner of Figure 1 shows the region where M3 laminated steel saturates. During un-faulted conditions the flux density is oscillating within this "Steady state" region. As can be seen in Figure 1, the permeability of the material at this field intensity is approximately equal to the permeability of air; hence, the impedance of the AC winding is equivalent to that of an air-cored inductor. During a fault event the rising current causes the flux density to oscillate through a much larger region of the B-H loop. As the core de-saturates and moves into the "Faulted state" region shown in Figure 1, the permeability of the core material increases. Hence, the impedance of the AC winding also increases, subsequently limiting the fault current.

A diagram illustrating the basic elements of a single-phase saturated core FCL is shown in Figure 2. Since only one half of the AC fault cycle will drive a core out of saturation, 2 separate AC coils and cores are required to effectively limit both the positive and negative half cycles of a single-phase fault current. Note that for effective limiting of both half cycles, the direction of the current in the 2nd AC coil is opposite to that of the 1st AC coil (as shown in Figure 2). The insertion impedance in this device is approximately equal to the series combination of the air-core impedances of the 2 AC coils. In comparison, the fault impedance is dominated by the increased impedance of a single coil, as only one of the cores is de-saturated during each half cycle while the other remains saturated.

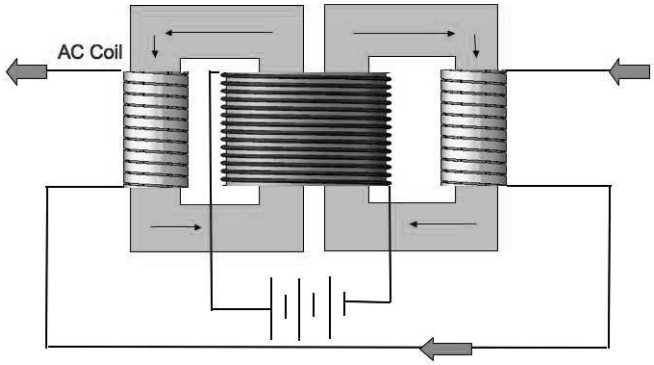

Figure 2. Single-Phase FCL Diagram

Figure 2 shows a single DC biasing winding used to saturate both cores. In a HTS saturated core FCL it is the DC biasing winding that is wound using the HTS material. While the first prototype of this device (detailed in [7] and [8]) used separate biasing coils for each core, a single winding simplifies the superconductor and cryogenic requirements. For this reason, the 3-phase device detailed throughout the remainder of this paper (which has 6 cores) uses a single DC biasing winding.

B. Design Optimisation

The key design criteria for an FCL device are the insertion impedance and the fault impedance. Typical industry requirements lead to general specifications of an insertion impedance of <1% of the bus base impedance and a fault impedance that results in at least 50% fault current reduction. Equations (1) and (2) describe these two specifications respectively.

$$\mathrm{X}_{ins} \leq 0.01\mathrm{X}_{base} \quad (1)$$

$$\mathrm{X}_{fault} \geq \mathrm{X}_{source} \quad (2)$$

As mentioned in Section II-A, the insertion impedance of a single-phase of a saturated core FCL is approximately equal to the series combination of the air-core impedances of the 2 AC coils. The air-core inductance of an ideal solenoidal coil (long and thin) is generally given by Equation (3), where: μ_0 is the permeability of air, N is the number of turns

in the coil, *A* is the area of the coil and *l* is the height of the coil. The inductance of a real coil is equivalent to Equation (3) multiplied by a correction factor (β), which is dependent on the actual geometry of the coil. Hence, the insertion impedance of a saturated core FCL can be approximated by Equation (4).

$$L = \frac{\mu_0 N^2 A}{l} \text{ H} \tag{3}$$

$$\mathrm{X}_{ins} \approx 2\omega \frac{\mu_0 N^2 A}{l} \beta \tag{4}$$

In determining an expression for the fault impedance, consider first the voltage induced in the AC coils during the positive half of the fault cycle. Equation (5) represents Faraday's law of induction for a tightly wound coil of N turns, where: ϕ is the total flux linking the coil. During the half fault cycle the core that remains saturated has negligible change in flux, so the induced coil voltage can also be considered negligible. In the core that de-saturates, the peak of the induced coil voltage is proportional to the peak flux change during the half cycle (via Faraday's law). If the system is designed such that the whole B-H loop is traversed during each half fault cycle, then the peak change in flux is equivalent to the area of the core (A_{core}) multiplied by twice the saturating flux density (B_{sat}). This leads to the expression for peak voltage given by Equation (6).

$$\mathrm{V} = N \frac{d\phi}{dt} \tag{5}$$

$$\begin{aligned} \mathrm{V}_{pk} &= N\omega\phi_{pk} \\ &= 2N\omega A_{core} B_{sat} \end{aligned} \tag{6}$$

The process of inducing voltages in each AC coil is identical during the negative half of the fault cycle, only with the roles of the 2 cores (and associated coils) reversed. Hence, the voltage across the 2 AC coils in series will approximate a sinusoid during one complete fault cycle. This leads to the approximate expression for fault impedance given by Equation (7), where: I_{fault} is the limited rms fault current.

$$\begin{aligned} \mathrm{X}_{fault} &\approx \frac{\mathrm{V}_{pk}}{\sqrt{2}\mathrm{I}_{fault}} \\ &\approx \frac{2N\omega A_{core} B_{sat}}{\sqrt{2}\mathrm{I}_{fault}} \end{aligned} \tag{7}$$

An examination of Equations (4) and (7) reveals that the insertion and fault impedances are related (with key system design parameters included in both expressions). Hence, the design of a saturated core FCL is a multi-variable optimisation problem, with the core design coupled to the high voltage AC coil design and the HTS DC coil design. The solution to this optimisation problem involves extensive characterisation of experimental cores and coils, iterative finite element analyses and electrical circuit simulation, with subsequent empirical modelling. This is the process that has been undertaken by the authors of this paper, with continual revisions being made to the active FCL design model.

One example that illustrates this design process is the developments that have been made in the core design between the first single-phase prototype device (detailed in [7] and [8]) and the 3-phase device described in this paper. Due to design constraints associated with the HTS DC biasing coil, and the corresponding cryogenic cooling system, the preferred position of each AC coil is on a separate limb to that of the DC coil (as illustrated in Figure 2). If the cross-sectional area is then uniform throughout the core, flux leakage renders it impossible to saturate the AC-side limb. Plots of the measured flux density versus magnetising force for both the AC and DC side limbs of the single-phase prototype device (which used cores of uniform cross-section) are shown in Figure 3.

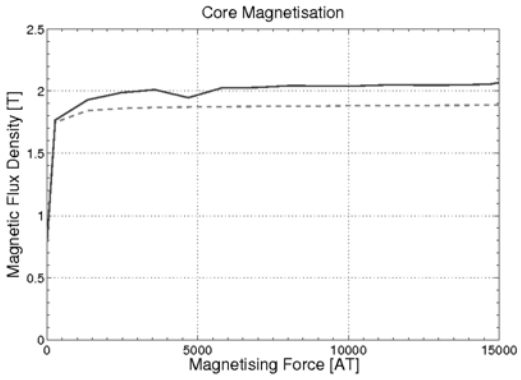

Figure 3. Core Magnetisation of Prototype Single-Phase FCL

It can be seen from Figure 3 that once the DC-side limb saturates (solid line), the AC-side limb also appears to saturate (dashed line) but at a lower flux density. In fact the AC-side limb is not really saturated, but rather leakage flux has limited the biasing effect of the DC winding. With this design, steady state load current in the AC coils would result in significant flux change in the AC-side limb and consequently, a higher than expected insertion impedance. To overcome this issue the improved design model employs a graded core, where the cross sectional area of the AC side limb is a fraction of the cross sectional area of the DC side limb. This graded core design approach was refined through extensive finite element analyses and testing of experimental cores.

Figure 4 shows an FEA generated snapshot of a fully saturated 3-phase core, where the cross-sectional area of the AC-side limbs is 60% that of the DC-side limbs. Although flux leakage in this core reduces the flux density of the yokes to around 1.8T, the graded core design ensures that the AC-side limbs still reach saturation (with the flux density of the AC-side limbs above 2T). Another benefit of the

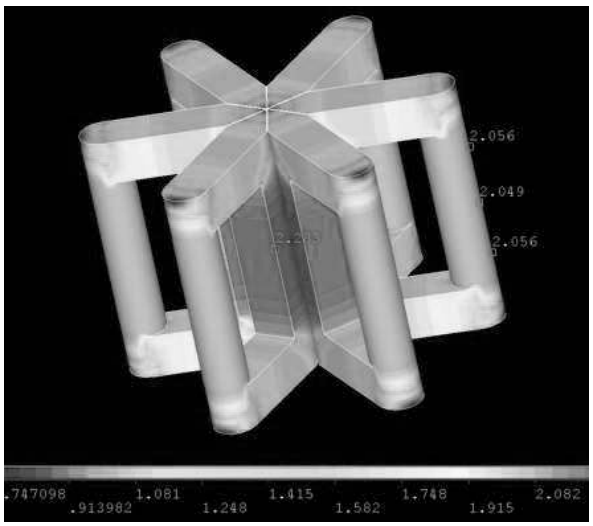

Figure 4. FEA Simulated Magnetisation

graded core design is that current flow in the AC coils results in a reduced change in flux density on the DC-side limbs (when compared with a core of uniform cross-section). This characteristic helps to reduce the induced voltages on the superconducting DC coil during a fault event. Figure 5 shows an FEA generated snapshot of the 3-phase core during a fault event. As can be seen, the AC-side limbs have de-saturated down to a flux density of 0.1T, while the DC-side limbs remain saturated at over 2T.

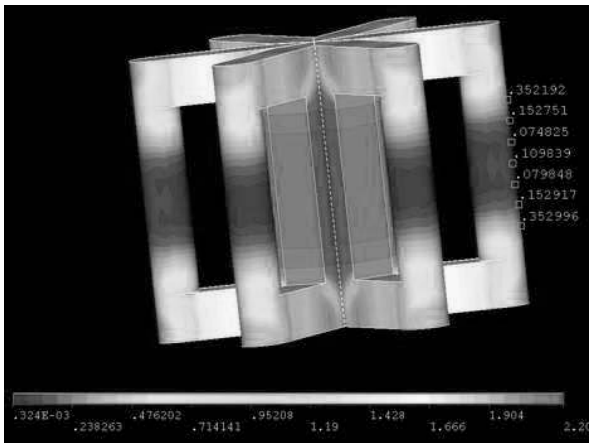

Figure 5. FEA Simulated De-Magnetisation

The core magnetisation and de-magnetisation behaviour illustrated in Figures 4 and 5 can be described by Equations (8) and (9) respectively. In both of these equations the magnetising forces on each limb are proportional, where the *core de-magnetisation factor* (α) is the constant of proportionality. The core de-magnetisation factor can be determined experimentally, and varies depending on the core design and relative positions of the AC and DC coils.

$$\mathrm{H}_{dc} = (\mathrm{H}_{sat} + \mathrm{H}_{ac})\,\alpha \tag{8}$$

$$N_{dc}\mathrm{I}_{dc} = \frac{N_{ac}\left(\sqrt{2}\mathrm{I}_{fault}\right)}{2}\alpha \tag{9}$$

III. Experimental Details

A small-scale prototype of the 3-phase device described in this paper was built specifically to test the validity of the current design model. The core of the prototype was designed to protect 3-phase sources of up to $400\mathrm{V}_{LL}$, with the AC-side limbs having a cross-sectional area of $6 \times 10^{-3}\mathrm{m}^2$ and the DC-side limbs having a cross-sectional area of $10 \times 10^{-3}\mathrm{m}^2$. The initial testing of this prototype was undertaken with a copper DC coil (with N = 102 Turns) so that all fault transients could be analysed, and appropriate protection circuits designed, before installing a HTS coil with complete cryogenic system. Initial AC coils were wound using $16\mathrm{mm}^2$ copper cable (with N = 20 Turns and l = 280mm), with the theoretical insertion reactance of these coils (via Equation (4)) equal to $6.9 \times 10^{-3}\Omega$. A photograph of the prototype system is shown in Figure 6.

Figure 6. Prototype 3-Phase FCL

To automate the prototype testing procedures, a complete control and data acquisition system was also constructed. A 96 kW resistive load bank was used to simulate normal steady state load conditions, with a 3-pole contactor used to short-circuit the load bank and simulate fault conditions. Voltages across the complete FCL were measured through an analogue input channel of a data acquisition board (after isolation and scaling) and fault currents were measured using a 4000A closed loop Hall effect current transducer. Integrating flux-meters were also used to measure the flux densities in each limb.

IV. RESULTS

Measurements of flux density versus magnetising force for one phase of the prototype device (for both AC and DC side limbs) are shown in Figure 7. As can be seen, the graded core design ensures that the AC-side limbs reach saturation. However, it can also be seen that once the AC-side limbs reach saturation, the rate of increase of flux density in the DC-side limbs reduces. This characteristic can result in a significant difference between the magnetising forces required to saturate each limb. This is an important design consideration as the DC bias point should be chosen such that both the AC and DC side limbs are saturated (to ensure that both the insertion impedance and any induced voltages on the DC bias coil are minimised).

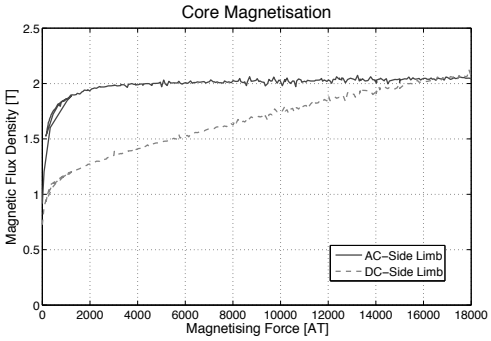

Figure 7. Core Magnetisation of 3-Phase FCL

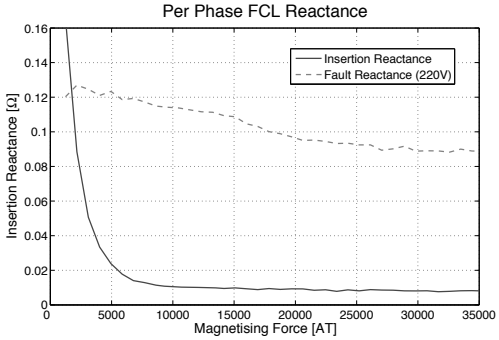

Figure 8. Per Phase Insertion Reactance of 3-Phase FCL

The actual per phase insertion impedance of the prototype device was measured at varying values of DC bias. The per phase fault impedance for a 380V$_{LL}$ source was also measured at the same DC bias values. Figure 8 shows plots of the resulting insertion and fault reactances (ie resistive components removed) against magnetising force. The measured insertion reactance was found to settle at the theoretical value of $6.9\times10^{-3}\Omega$ at approximately 18,000 AT. It is clear from Figure 8 that the fault impedance increases as the magnetising force reduces; however, the insertion impedance also increases (which will reduce the benefits of the saturated core FCL). Hence, the choice of DC bias point is an important factor in the overall design optimisation problem and should be chosen such that insertion impedance is minimised, while providing good fault reduction and minimal induced voltages on the DC biasing coil. For this prototype system a DC bias that produces approximately 18,000 AT of magnetising force best meets this criteria.

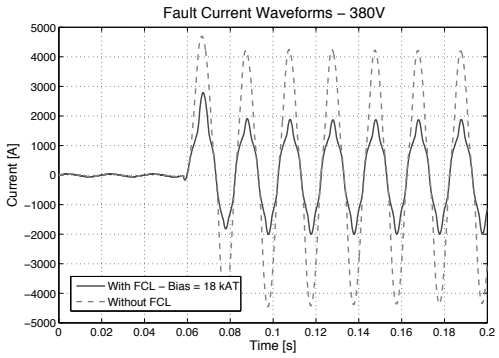

Figure 9. Fault Currents - 380V 3-Phase Source

Transient fault current measurements with and without the FCL in circuit are shown in Figures 9 and 10. For clarity reasons only one representative phase is shown in each of these figures; however, the actual faults were introduced on all three phases simultaneously. A 380V$_{LL}$ 3-phase source was used for the data shown in Figure 9, while a 170V$_{LL}$ 3-phase source was used for the data shown in Figure 10.

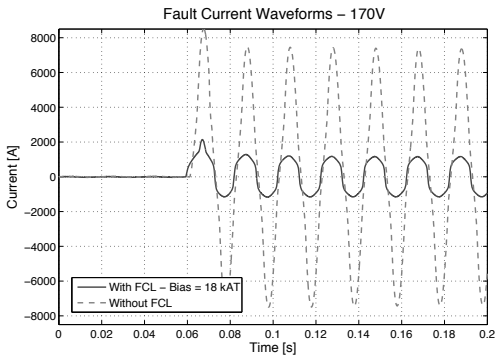

Figure 10. Fault Currents - 170V 3-Phase Source

A fault current reduction of 56% can be seen in Figure 9, while a fault current reduction of 82% can be seen in Figure 10. Both of these results exceed the minimal industry requirement of 50% fault current reduction. The reason that the reduction is much greater in Figure 10 is that the source impedance of the 170V$_{LL}$ source is much lower than that of the 380V$_{LL}$ source ($19m\Omega$ per phase, compared with $74m\Omega$ per phase). The actual fault impedance of the FCL is very similar in both cases. Note however that the FCL limited current for the 380V$_{LL}$ source is distorted (very peaky). This

result occurs whenever the flux density oscillation causes the cores to saturate in the third quadrant of the B-H loop.

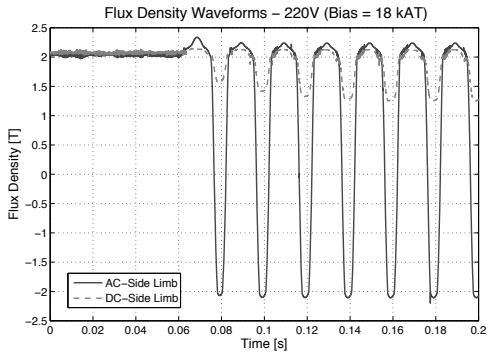

Figure 11. Flux Density - 380V 3-Phase Source

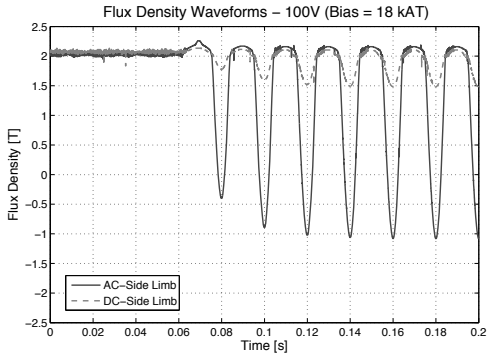

Figure 12. Flux Density - 170V 3-Phase Source

Transient flux density measurements for these two cases are shown in Figures 11 ($380V_{LL}$ source) and 12 ($170V_{LL}$ source). As can be seen the AC-side flux density in Figure 11 reaches below -2T during the fault, briefly saturating the limbs. For the $170V_{LL}$ case, shown in Figure 12, the flux density reaches -1T during the fault. The optimal performance of this prototype device would be in-between these two cases, where the flux density in the AC-side limbs would oscillate through the entire B-H loop without causing saturation in the third quadrant. Note finally that the flux density oscillation in the DC-side limbs, of both Figures 11 and 12, is much less than that of the respective AC-side limbs (as desired).

V. Conclusions

The design and development of 3-phase saturated core high temperature superconducting fault current limiters were discussed in this paper. The principles of operation of saturated core FCLs were outlined in Section II-A, with the practical benefits of using a single DC biasing winding (in simplifying the superconducting and cryogenic requirements) also addressed. The insertion and fault impedances were identified as key design criteria for FCL devices, and expressions that can be used to approximate these impedances (for a saturated core FCL) were derived in Section II-B. The successful design of saturated core FCLs was shown to be a multi-variable optimisation problem, with the insertion impedance, fault impedance and induced voltages on the DC bias coil shown to be dependent on similar aspects of the core design, AC coil design, DC coil design and DC bias point.

The successful design, construction and testing of a prototype 3-phase saturated core FCL was also detailed. This particular device incorporated a single DC bias coil and graded core design. The benefits of a graded core design were experimentally demonstrated. The prototype device was also tested in terms of steady state insertion impedance and fault current limiting ability. It was found that an insertion impedance equivalent to the air-core impedance of the 2 AC coils in series could be achieved with this device. The complete set of results showed that this device can achieve effective fault current clipping with a low steady state insertion impedance.

VI. Acknowledgement

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