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Jeffrey W. Moscrop
University of Wollongong, jeffm@uow.edu.au

Scott Hopkins
scott.hopkins@zenergypower.com

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Development and Performance Analysis of a Saturated Core High Temperature Superconducting Fault Current Limiter

Jeff Moscrop
Faculty of Engineering
University of Wollongong
NSW 2522 Australia

Scott Hopkins
Zenergy Power Pty Ltd
Lucas Heights
NSW 2234 Australia

Abstract—Recent international activity in the field of high voltage Fault Current Limiters (FCLs) has intensified since the North American blackout of 2003. A number of national and international peak body groups in the USA, Europe and Japan have been established to assess the need for FCLs and the issues associated with their design, specification, operation, protection and integration into the electricity grids. This paper details the development of a prototype 3-phase saturated core High Temperature Superconducting (HTS) FCL in Australia. Through experimental analysis, the performance of this device is characterised in terms of DC saturation, steady state performance, and fault current limiting ability.

I. INTRODUCTION

Both the occurrence of fault currents and the sensitivity of network equipment to fault currents have been increasing in modern power grids. The vulnerability of these electrical networks is evidenced by an increasing number of major power failures, such as those experienced in North America (2003), Malaysia (2005) and Sydney Australia (March, 2009). This vulnerability, which is predominately a result of increasing demands on grids and the introduction of newer technologies into grids, is predicted to increase as utilities transition to renewable energy generation and experience continued load growth [1], [2]. The costs associated with any power failure include the costs of damage to network hardware and the costs of network unavailability to consumers (which are often much higher). One result of the 2003 North American blackout, in particular, has been an increase in international activity in the field of high voltage Fault Current Limiters (FCLs). An FCL is a device that limits the peak current amplitude during a fault, hence providing the dual benefits of improving network availability and protecting sensitive network equipment from these high current peaks.

There are several different FCL technologies currently attracting research attention [3]. Some example technologies are solid state FCLs [4], superconducting resistive FCLs [5], [6] and saturated core superconducting FCLs [7], [8]. One important aspect of any FCL is that it should ideally impose negligible impedance to the network during the steady (un-faulted) state. Further, any other power losses associated with

normal operation of the FCL have major significance. Solid state FCLs use solid state switches (usually IGBTs) to control the fault current and have a very low un-faulted impedance; however, these devices suffer from high power losses during the un-faulted state (due to the power electronics). Superconducting resistive FCLs also provide very low un-faulted impedance. However, since these devices are driven out of the superconducting state by the fault current (thus increasing the impedance and providing fault current limiting), they suffer from very slow recovery and can be unreliable. In comparison, the saturated steel core superconducting FCL has negligible power losses during the un-faulted state and also provides instantaneous reaction and recovery.

The development of a prototype 3-phase saturated core High Temperature Superconducting (HTS) FCL is discussed in this paper. Details of the overall device design are presented, along with details of the automated test environment and data acquisition system. An experimental analysis is also presented, with the performance of the device characterised in terms of DC saturation, steady state performance and fault current limiting ability.

II. PRINCIPLES OF THE SATURATED CORE HTS FCL

The saturated steel core fault current limiter has existed as a concept for several years [9]. The requirement of simultaneously obtaining a low steady state un-faulted AC terminal impedance and a high transient fault impedance (for current limiting) is met through the change in permeability between saturated and unsaturated states of the steel core. This concept can be demonstrated through an analysis of the magnetisation properties of typical steel core material (experimentally measured magnetisation properties for M3 electrical steel are shown in Figure 1).

In a saturated core FCL an HTS DC winding is used to initially bias the core into saturation, with a separate winding used to carry the AC load current. Under normal un-faulted load conditions the magnetisation forces set up by the AC load current are not high enough to drive the core out of saturation and the FCL operates completely within the saturated region of

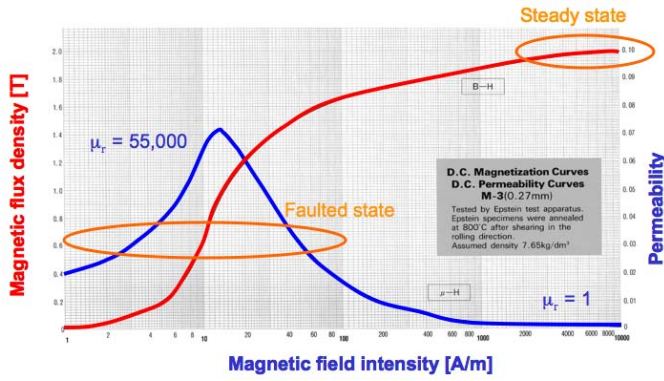


Figure 1. Material Properties of M3 Electrical Steel

the B-H curve (ie the region labelled “Steady state” in Figure 1). As can be seen in Figure 1, the permeability of the core in this steady state region is approximately equivalent to the permeability of air (ie $\mu_r = 1$). Hence, the AC winding approximates an air-cored inductor, resulting in a very low steady state impedance. During a fault event the rising current sets up magnetisation forces high enough to de-saturate the core and the FCL operates in a region of much higher permeability (for example, the relative permeability of the “Faulted state” region in Figure 1 is 55,000). Hence, the impedance of the AC winding increases during this faulted state and the peak amplitude of the fault current is subsequently limited.

One important aspect of a saturated core FCL is that only half of the AC cycle will set up magnetisation forces that oppose the initial saturating field and result in de-saturation of the core. The magnetisation forces set up during the other half of the AC cycle support the initial saturating field, resulting in negligible change to the core flux density. Hence, two separate “AC coil and core” sets are required to effectively limit both the positive and negative half cycles of a single-phase fault current. A diagram illustrating the fundamental layout of the two cores, and associated coils, of a single-phase saturated core FCL is shown in Figure 2. Note in Figure 2 that the direction of current flow in the 2nd AC coil is opposite to that of the 1st AC coil.

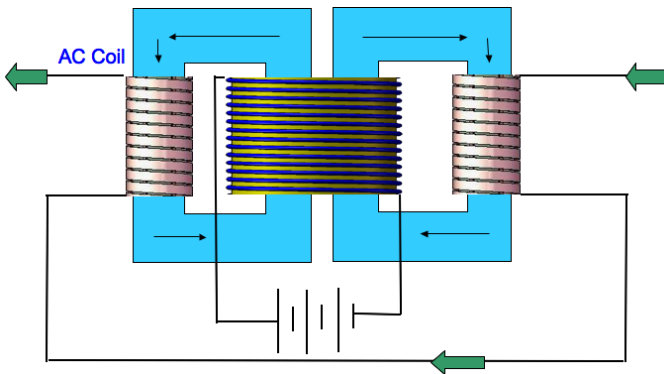


Figure 2. Single-Phase FCL Diagram

For the device shown in Figure 2, the impedance during the un-faulted state (*insertion impedance*) is approximately equal to the series combination of the air-core impedances of the 2 AC coils. An expression for this impedance is given in Equation (1) – where μ_0 is the permeability of air, N is the number of turns in each AC coil, A is the area of each coil, l is the height of each coil and β is a correction factor (note that β is dependent on the actual geometry of the AC coils).

$$X_{ins} \approx 2\omega \frac{\mu_0 N^2 A}{l} \beta \quad (1)$$

The impedance during a fault event (*fault impedance*) is non-constant; however, it is dominated by the increased impedance of a single AC coil (since only one core de-saturates during each half cycle of the fault current). An approximate expression for this fault impedance can be derived using Faraday’s law of induction. If it is assumed that the entire B-H loop is traversed during each half fault cycle, the fault impedance is approximated by the expression given in Equation (2) – where N is the number of turns in each AC coil, A_{core} is the cross-sectional area of the core, B_{sat} is the saturated flux density of the core material and I_{fault} is the limited rms fault current.

$$X_{fault} \approx \frac{2N\omega A_{core} B_{sat}}{\sqrt{2}I_{fault}} \quad (2)$$

It is worth noting that the FCL layout shown in Figure 2 employs a single DC biasing coil. This is an important design consideration, especially for 3-phase devices where 6 complete cores and associated AC coils are required. Although separate DC biasing coils can be used for each core, a single winding simplifies the superconductor and cryogenic requirements. For this reason, the 3-phase device detailed throughout the remainder of this paper uses a single DC biasing coil for all 6 cores.

III. THE PROTOTYPE DESIGN

A prototype 3-phase FCL has been designed and constructed by a combined team from the University of Wollongong and Zenergy Power. This prototype was specifically designed as a small-scale FCL test-bed and is limited to low voltages (up to $400V_{LL}$). The 6 cores of the prototype are arranged in a “pie” configuration, which allows for a single DC-biasing coil to be wound around the 6 limbs at the centre of the device. The AC load-carrying coils are wound around each of the 6 outer limbs. A photograph of the completed prototype device is shown in Figure 3.

The device shown in Figure 3 also employs a graded core design, where the cross-sectional area of each AC-side limb is 60% that of the DC-side limbs ($A_{AC} = 6 \times 10^{-3}m^2$ and $A_{DC} = 10 \times 10^{-3}m^2$). This graded core approach is necessary to achieve effective saturation of the AC-side limbs, as flux leakage inhibits the ability of a biasing coil to saturate the AC-side limbs when the cross-sectional area of the cores is uniform. The initial testing of this prototype



Figure 3. Prototype 3-Phase FCL

was undertaken with a copper DC biasing coil so that all fault transients could be analysed, and appropriate protection circuits designed, before installing a HTS coil with complete cryogenic system. The initial AC coils were wound directly onto the limbs using insulated copper cable (as can be seen in Figure 3). The specifications of the initial AC and DC side test coils are:

- DC coil material: 4mm × 14mm copper bar,
- Number of turns on DC coil: $N_{DC} = 102$,
- AC coil material: 16mm² insulated copper cable,
- Number of turns on each AC coil: $N_{AC} = 20$,
- Height of each AC coil: $l = 280\text{mm}$,
- Theoretical per phase insertion impedance of AC coils (via Equation (1)): $X_{ins} = 6.9 \times 10^{-3}\Omega$.

In order to characterise the performance of the prototype FCL an automated test environment and data acquisition system were also developed. A 96 kW resistive load bank was used to simulate normal steady state load conditions, with a 3-pole contactor used to short-circuit the load bank and simulate fault conditions. Overall supervisory control was handled by a standard PC running the LabView development suite. A National Instruments data acquisition board (model #: USB-6221) was used for collecting the experimental data and for interfacing the PC with the control hardware. A photograph illustrating the complete control centre for the characterisation tests is shown in Figure 4. As can be seen in Figure 4, the PC is mounted on a mobile desk with two enclosures used to house the major test-circuit control and data acquisition components. A small stack of safety beacons and the current transducer used for fault current measurement are also shown in Figure 4 (mounted on top of one of the enclosures).



Figure 4. Test System Control Centre



Figure 5. Test System DAQ and Sensor Enclosure



Figure 6. Test System Contactor Enclosure

The source voltage, FCL AC coil voltages and FCL DC coil voltage were all measured via analogue input channels on the data acquisition board (after isolation and scaling). Fault currents were measured using a closed loop Hall effect

current transducer with an 8000A peak measuring capability. Integrating flux-meters were also used to measure the flux densities in each limb. The National Instruments data acquisition board, DC-side current transducers and the voltage conditioning components are all housed inside one of the enclosures and are shown in in Figure 5. The contactors used for activating the main circuit and simulating fault conditions are housed in the other enclosure and are shown in Figure 6. The fault current transducer is mounted on top of one of the enclosures (as shown in Figure 4).

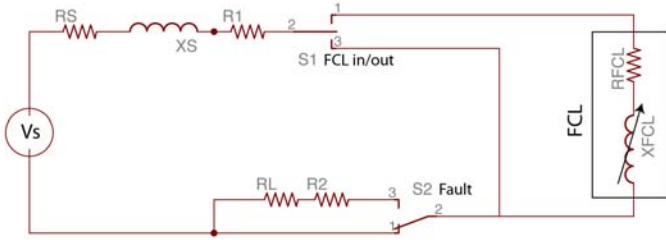


Figure 7. FCL Test Circuit

The per phase equivalent test circuit is shown in Figure 7. The components of the equivalent test circuit, along with their respective values (used during the characterisation tests) are listed in Table I.

Component	Description	Value
Vs	Voltage source	380 V _{LL}
RS + XS	Combined Source Impedance (per phase)	74 mΩ
R1	Cabling resistance: Source-FCL	3.41 mΩ
RFCL	Per phase FCL resistance (2 AC coils in series)	24 mΩ
XFCL	Per phase FCL reactance	Variable
RL	Load resistance	7.2 Ω
R2	Cabling resistance: fault contactor-load bank	1.32 mΩ
S1	Switch – FCL in/out of circuit	N/A
S2	Switch – fault contactor	N/A

Table I
TEST CIRCUIT COMPONENTS

IV. EXPERIMENTAL ANALYSIS

The performance of the 3-phase prototype device shown in Figure 3 has been characterised in terms of DC saturation, steady state performance, and fault current limiting ability. The DC saturation characteristics of the device are shown in Figure 8, where measured flux density is plotted against magnetising force for one phase of the device (for both AC and DC side limbs). As can be seen, the graded core design ensures that the AC-side limbs reach saturation. However, it can also be seen that once the AC-side limbs reach saturation, the rate of increase of flux density in the DC-side limbs reduces. This characteristic can result in a significant difference between the magnetising forces required to saturate each limb, which is an important design consideration as the DC bias point should be chosen such that both the AC and DC side limbs are saturated.

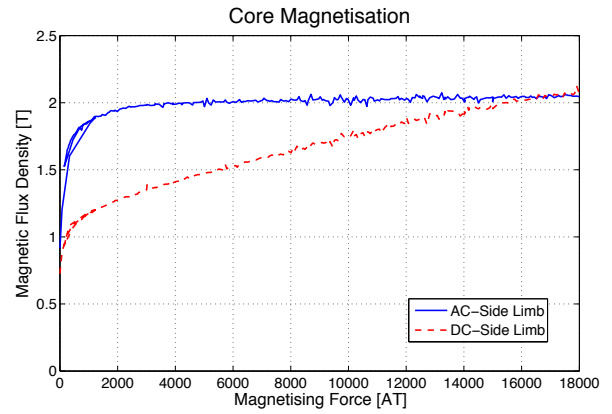


Figure 8. Core Magnetisation of 3-Phase FCL

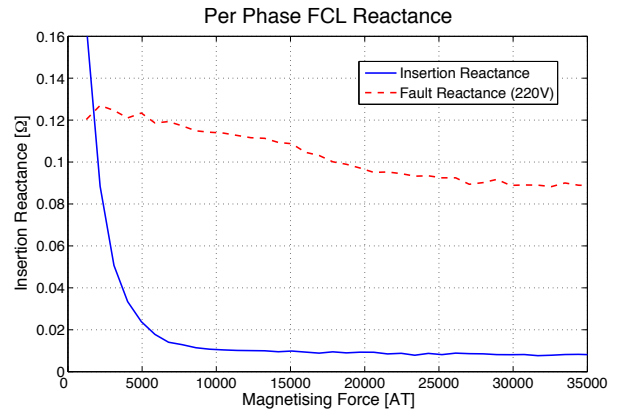


Figure 9. Per Phase Insertion Reactance of 3-Phase FCL

If the DC bias point is chosen such that only the AC-side limb saturates (for example at 10,000 AT in Figure 8), the insertion impedance will remain low, but induced voltages on the DC bias coil during a fault event will be significant.

The actual per phase insertion impedance of the prototype device was measured at varying values of DC bias, along with the per phase fault impedance for the 380V_{LL} source. Figure 9 shows plots of the resulting insertion and fault reactances (ie resistive components removed) against magnetising force. The measured insertion reactance was found to settle at the theoretical value of $6.9 \times 10^{-3} \Omega$ at approximately 18,000 AT. As the DC bias point increases and moves away from the AC-side knee point (shown in Figure 8), the effective fault current clipping reduces. Hence, magnetising forces above 18,000 AT on this device will result in reduced fault current clipping, with no significant improvement in insertion impedance.

Transient fault current tests at varied DC bias points were initially undertaken using a smaller 60V_{LL} source (as opposed to the 380V_{LL} source detailed in Table I). This approach allowed for the effects of bias point to be examined at lower fault current levels. The resulting transient fault current measurements for the prototype FCL are shown in Figures 10, 11 and 12. For clarity reasons only one representative phase is

shown in each of these figures; however, the actual faults were introduced on all three phases simultaneously. The transient fault current for the same system without the FCL in circuit is also shown in each figure (which reached a magnitude of approximately 2,500A before the circuit breaker on the supply transformer opened).

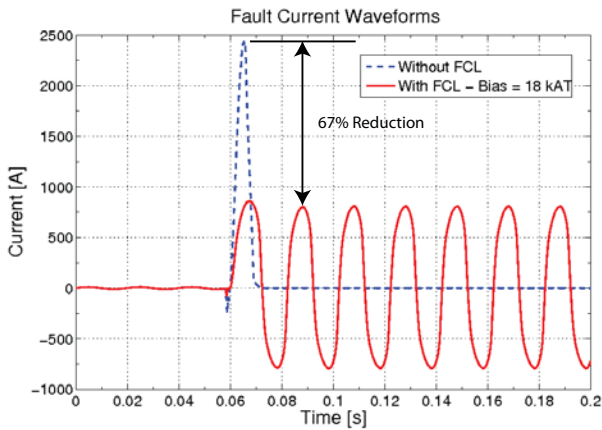


Figure 10. Fault Currents – 60V 3-Phase Source, 18 kAT Bias

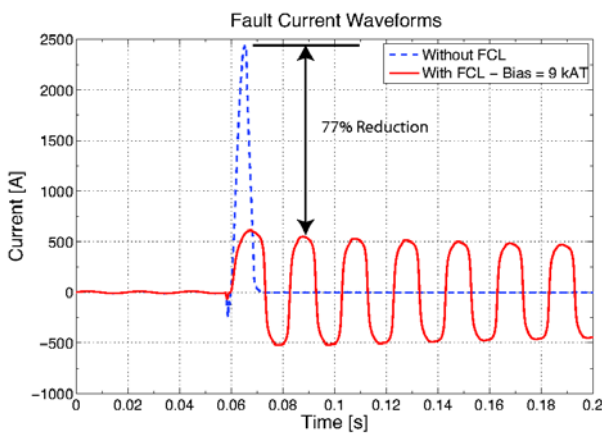


Figure 11. Fault Currents – 60V 3-Phase Source, 9 kAT Bias

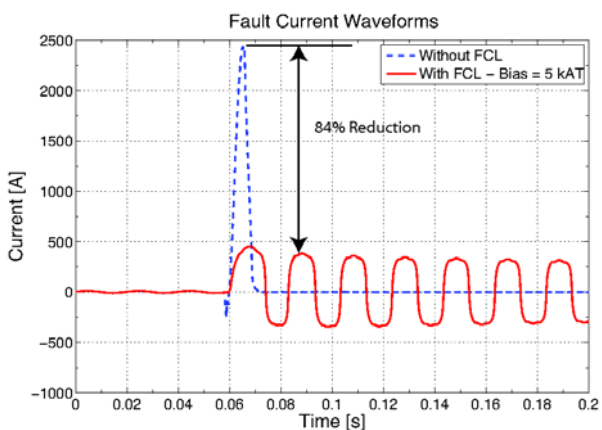


Figure 12. Fault Currents – 60V 3-Phase Source, 5 kAT Bias

A fault current reduction of 67% can be seen in Figure 10, where the magnetising force was 18,000 AT. The insertion reactance at this bias was measured to be $6.9 \times 10^{-3} \Omega$. Figure 11 shows a fault current reduction of 77% for a magnetising force of 9,000 AT. The measured insertion reactance at this bias was $9.3 \times 10^{-3} \Omega$. Figure 12 shows a fault current reduction of 84% for a magnetising force of 5,000 AT. The measured insertion reactance at this bias was $13 \times 10^{-3} \Omega$. These results show that although the fault impedance increases as the DC bias is reduced (thus improving the current clipping), the insertion impedance also increases (which reduces the benefits of the saturated core FCL).

The combined magnetisation, insertion impedance and transient fault results, shown in Figures 8 to 12, illustrate the importance of choosing an optimal DC bias point. Hence, the DC bias point is an important factor in the overall design optimisation problem and should be chosen such that insertion impedance is minimised, while still providing good fault reduction and minimal induced voltages on the DC biasing coil. From the results presented for the prototype system (in Figures 8 to 12), a DC bias that produces approximately 18,000 AT of magnetising force best meets this criteria.

In order to test the limits of operation of the prototype FCL, a transient fault current test was also undertaken using the 380V_{LL} source at the optimal bias of 18,000 AT. The resulting fault current measurements, with and without the FCL in circuit, are shown in Figure 13. A fault current reduction of 56% can be seen, which exceeds the minimum industry requirement of a 50% fault current reduction. However, there is also visible distortion at the peaks of the FCL limited current waveform. This result is due to the flux density of the cores traversing the B-H loop all the way into the saturation region of the third quadrant. Hence, the combination of voltage level and source impedance of the 380V_{LL} source is slightly above the optimal limits of this prototype device. The device performs optimally when the flux density in the AC-side limbs traverses the B-H loop right down to the knee-point in the third quadrant, but without continuing into the saturation region.

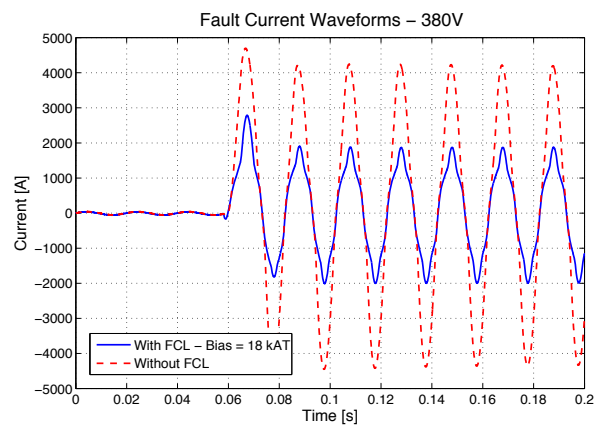


Figure 13. Fault Currents – 380V 3-Phase Source, 18 kAT Bias

The recovery characteristics of the prototype FCL were also tested. For this test the control software was configured to simulate circuit-breaker auto re-closing logic. After 10 cycles of an initial fault the circuit breaker was opened for a period of 1s and then re-closed, with the fault still present. A further 10 cycles of fault were allowed before the circuit breaker was again opened and then re-closed after a period of 3s (again with the fault still present). The results of this test, using the $380V_{LL}$ source, are shown in Figure 14. As can be seen, the prototype FCL demonstrated instantaneous reaction and recovery, with the fault current peaks limited to under 2000 A (which is the same 56% reduction demonstrated in Figure 13) each time the circuit breaker was re-closed.

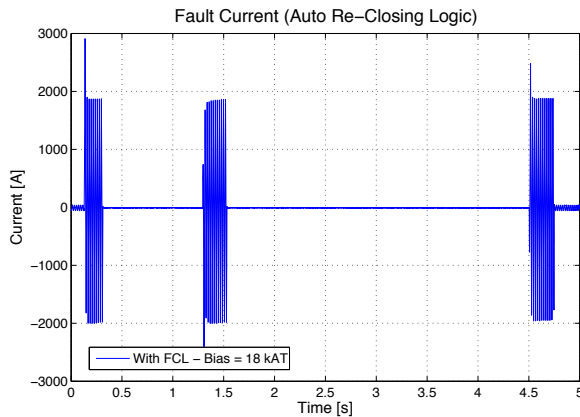


Figure 14. FCL Recovery Transient

V. CONCLUSIONS

Design aspects of saturated core high temperature superconducting fault current limiters were discussed in this paper, with the development of a prototype 3-phase FCL described. The basic principles of operation of saturated core FCLs were outlined in Section II, with the use of a single DC biasing winding identified as providing practical benefits in simplifying the superconducting and cryogenic requirements.

The design and construction of a prototype 3-phase FCL was detailed in Section III. This device consisted of 6 complete cores arranged in a pie configuration, and also incorporated a single DC bias coil and graded core design. The problem of leakage flux and the associated difficulties in effectively saturating the AC-side limbs in cores of uniform cross-section were described. The graded core design was shown to provide considerable benefits in reducing these problems. The development of an automated test environment and data acquisition system for characterising the prototype FCL was also detailed in Section III.

Characterisation tests on the prototype device were presented in Section IV. It was found that a per-phase insertion

impedance equivalent to the air-core impedance of 2 AC coils in series could be achieved with this device. It was also found that effective fault current clipping, above the minimum industry requirement of 50%, could be achieved while maintaining this low insertion impedance. Further testing showed that improved fault current clipping was possible; however, this was at the expense of a higher insertion impedance. The instantaneous reaction and recovery of this device was also experimentally demonstrated.

The complete set of results showed the importance of optimising the design of a saturated core FCL for the intended source. An optimally designed device should result in the flux density of the AC-side limbs traversing the B-H loop right down to the knee-point of the the third quadrant during a fault, without continuing into the saturation region. The choice of DC bias point was also shown to be an important factor to be considered in the overall design optimisation problem, with the insertion impedance, fault impedance and induced voltages on the DC bias coil all affected by the choice of DC bias point.

VI. ACKNOWLEDGEMENT

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REFERENCES

- [1] P. M. Duggan, "Integration issues for fault current limiters and other new technologies - a utility perspective," in *IEEE Power Engineering Society General Meeting*, pp. 1-3, 2006.
- [2] P. M. Duggan, "Utility perspective on fault current limiters and expected synergies from integrating fault current limiters with superconducting cables," in *IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, pp. 1-2, 2008.
- [3] H. Schmitt, "Fault current limiters - application, principles and experience," in *CIGRE SC A3 and B3 Joint Colloquium*, (Tokyo, Japan), 2005.
- [4] EPRI, "Progress report on medium voltage solid-state current limiter," Tech. Rep. 1002117, Electric Power Research Institute, USA, 2004.
- [5] T. Kataoka and H. Yamaguchi, "Comparative study of transformer-type superconducting fault current limiters considering magnetic saturation of iron core," *IEEE Transactions on Magnetics*, vol. 42, pp. 3386-3388, 2006.
- [6] L. Kovalsky, X. Yua, K. Tekletsadik, A. Keri, J. Bock, and F. Breuer, "Applications of superconducting fault current limiters in electric power transmission systems," *IEEE Transactions on Applied Superconductivity*, vol. 15, pp. 2130-2133, 2005.
- [7] F. Darmann and T. Beales, "New fault current limiters for utility substations - design, analysis, construction and testing," in *TechCon Asia-Pacific Conference*, (Sydney, Australia), 2003.
- [8] C. J. Hawley, F. Darmann, and T. P. Beales, "Performance of a 1 mv a high temperature superconductors-enabled saturable magnetic core-type fault current limiter," *Superconductor Science and Technology*, vol. 18, pp. 255-259, 2005.
- [9] B. P. Raju, K. C. Parton, and T. C. Bartram, "A current limiting device using superconducting d.c. bias - applications and prospects," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-101, pp. 3173-3177, 1982.