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Abstract

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Keywords

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Seven-Level Cascaded ANPC-Based Multilevel Converter

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***Abstract*—A seven-level converter based on the cascaded connection of a three-level active neutral-point-clamped (ANPC) converter and individual H-bridge cells per phase is presented in this paper. This converter only requires a single DC source for all three phases and extends the amplitude of output voltage of the converter with similar DC-link voltage. The operation principles and control strategies based on a fundamental frequency harmonic elimination PWM are discussed. The regulation of FC voltage depends on the positions of switching angles over a quarter period in the available solutions and on the load power factor. In order to extend the regulation of the FC voltage into higher modulation indices an additional switching in the top voltage level is also considered. Experimental results taken from a low-power single-phase laboratory setup that verify the theoretical considerations and simulation results are presented.**

***Index Terms*—Active neutral-point-clamped, multilevel converter, selective harmonic elimination, pulse-width modulation, flying capacitor voltage control**

I. Introduction

Multilevel converters provide significant advantages over the typical two-level converter, such as lower harmonic distortion and lower electro-magnetic interference (EMI) and reduced stressed of the semiconductor switching devices. However an increase in the number of levels of the conventional multilevel converters such as the neutral point clamped (NPC), flying capacitor (FC) and the cascaded H-bridge (CHB) multilevel converters [1] increases, the complexity to control the voltage across DC-link capacitors of the NPC converter, the stored energy components of the FC converter and the number of isolated power supplies of the CHB converter. This increase in the complexity together with the additional components required affects the reliability and the efficiency of the converter [2]

Another drawback of the NPC converter is the uneven distribution of losses among the semiconductor devices. In order to overcome this disadvantage, a three-level active neutral-point-clamped (ANPC) converter was proposed by adding active switches to the clamping diodes. The switch connected anti-parallel to the clamping creates redundancy in the zero-voltage level switching states. These properties make it a particularly attractive topology in applications such as motor drives [3], advanced static-compensators (STATCOMs) [4], high-power high-voltage direct-current (HVDC) power transmission [5], grid connected photovoltaic (PV) systems [6], etc.

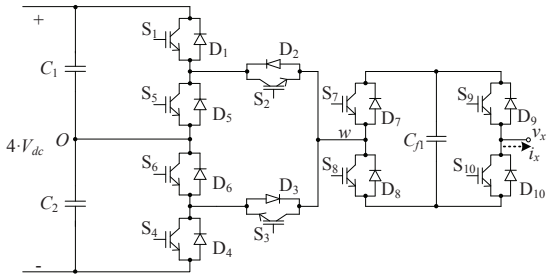

Fig. 1. Phase-leg of seven-level cascaded ANPC based multilevel (CAM) converter

To eliminate the need for individual DC sources for every level, hybrid converter topologies with H-bridge cells have been proposed. These include the five-level topology based on the cascaded interconnection of a two-level inverter with individual H-bridge cells for each phase [7], [8]. An asymmetrical converter based on the cascaded connection of the three-level NPC converter and H-bridge cell for medium drive applications using model predictive control was also proposed in [2]. A carrier based PWM control was implemented to control the voltage across FCs in cascaded connection of the three-level NPC converter and H-bridge cells [9], [10]. This converter only requires a single DC source for all the three-phases. The cascaded connection of the three-level NPC converter and H-bridge cell was proposed for current waveform conditioning in [11].

This paper discusses the operation of a multilevel inverter based on the cascaded interconnection of a three-level ANPC converter and individual H-bridges for each phase with a single DC source for the overall converter, as shown in Fig. 1, under fundamental harmonic elimination PWM. The voltages of the FCs of the H-bridges are maintained to one quarter of the DC-link voltage resulting in a seven-level output voltage waveform. Higher number of output voltage levels can also be achieved by varying the ratio of DC-link voltage to the voltage across the FC. An increase, however, in the number of the output voltage levels decreases the available redundancies

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TABLE I
SWITCHING STATES OF THE SEVEN-LEVEL CAM CONVERTER

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_{y2}	S_9	S_{10}
V_1							0	1	1	0
V_2	1	1	0	0	0	1	1	0	1	0
V_3							0	1	0	1
V_4							1	0	0	1
V_5							0	1	1	0
V_6	0	1	0	1	1	0	1	0	1	0
V_7							0	1	0	1
V_8							1	0	0	1
V_9							0	1	1	0
V_{10}	1	0	1	0	0	1	1	0	1	0
V_{11}							0	1	0	1
V_{12}							1	0	0	1
V_{13}							0	1	1	0
V_{14}	0	1	0	0	1	0	1	0	1	1
V_{15}							0	1	0	1
V_{16}							1	0	0	1
V_{17}							0	1	1	0
V_{18}	0	0	1	0	0	1	1	0	1	0
V_{19}							0	1	0	1
V_{20}							1	0	0	1
V_{21}							0	1	1	0
V_{22}	0	0	1	1	1	0	1	0	1	0
V_{23}							0	1	0	1
V_{24}							1	0	0	1

in the switching states to obtain specific output voltage levels which affect the loss balancing of the semiconductor devices. While regulating the FC voltage at its reference level, the fundamental component of the output voltage of the converter can achieve larger values than the three-level ANPC converter for the same DC-link voltage values, hence providing a voltage boost feature to the topology.

The paper is organized as follows. Section II analyzes the operation principles and control strategies of the converter. Section III discusses the harmonic elimination modulation method and Section IV discusses the FC voltage regulation control. Section V presents simulation results and Section VI presents experimental results based on a laboratory prototype converter. The work will be summarized in Section VII.

II. OPERATION PRINCIPLES

The cascaded ANPC based multilevel (CAM) converter is an arrangement of the three-level ANPC converter and the H-bridge cell which are connected in series as shown in Fig. 1. The DC-link consists of capacitors C_1 and C_2 providing the mid-point of the three-level ANPC converter. For a DC-link voltage of $4V_{dc}$, each DC-link capacitor voltage is ideally $2V_{dc}$ and FC (C_f) voltage is V_{dc}. In the three-level NPC converter, the upper or lower NPC path utilization is determined by the direction of the output current. The active switches S_5 and S_6 of the ANPC converter clamped to the neutral point would ensure the equal voltage sharing between the switches and

TABLE II
EFFECT ON FC DURING DIFFERENT SWITCHING STATES

Switching States	Effect on C_f	
	$i_x > 0$	$i_x < 0$
$V_1, V_5, V_9, V_{13}, V_{17}, V_{21}$	Discharge	Charge
$V_4, V_8, V_{12}, V_{16}, V_{20}, V_{24}$	Charge	Discharge

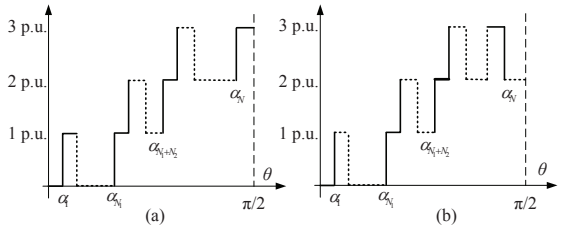

Fig. 2. Seven-level waveforms, (a) odd number of angles, (b) even number of angle

also create additional zero voltage level switching states which are utilized in order to distribute the losses in the three-level ANPC converter.

The CAM converter has twenty four switching states as shown in Table I. These switching states generate the seven different voltage levels, namely, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$. These switching states are the combination of the six switching states of the three-level ANPC converter and four switching states of the H-bridge cell. The voltage across the C_f is affected when the output terminal is connected through C_f to one of the DC-link terminals (positive DC rail, neutral point ('O'), negative DC-rail). This occurs when the output voltage levels are $3V_{dc}$, V_{dc}, $-V_{dc}$, and $-3V_{dc}$ levels. The output voltage levels $3V_{dc}$ and $-3V_{dc}$ are generated by V_1 and V_{24} respectively. Since there are no redundant states for these output levels, the voltage across the FC is determined by the direction of the output current and voltage regulation is not possible. The voltage across the C_f can be regulated at its reference voltage level using the redundant switching states that generate the output voltage levels V_{dc} and $-V_{dc}$. During the switching states V_5, V_8, V_9, V_{12}, V_{13}, V_{16}, V_{17}, and V_{20} the neutral point ('O') is connected to output terminal through C_f which influence the neutral point voltage of the converter. The charging and discharging of the C_f depends on the load and the effect on the FC voltage during the different switching states is summarized in Table II.

III. FUNDAMENTAL FREQUENCY HARMONIC ELIMINATION PWM

A harmonic elimination modulation strategy is considered, assuming a quarter-wave symmetry [12]. The angles are distributed to the three level transitions of the first quarter period. Assuming a generalized formulation (Fig. 2(a) and (b)), that the number of switchings between the zero and first level, first level and second level, and second level and third level

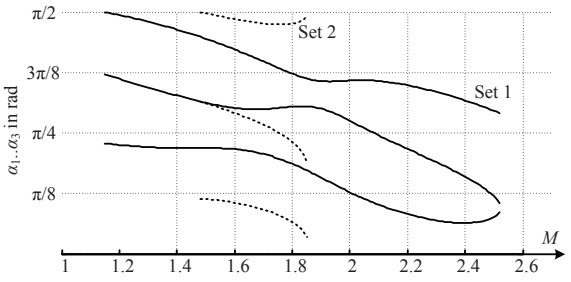

Fig. 3. Switching angles vs. modulation index for three angles per quarter period

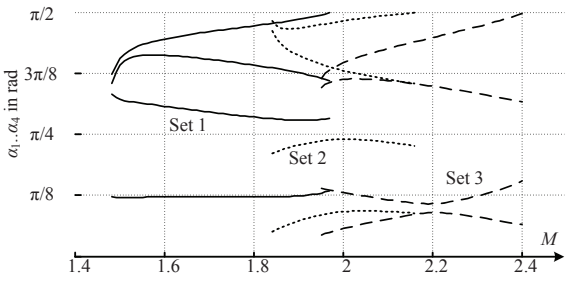

Fig. 4. Switching angles vs. modulation index for four angles per quarter period

are N_1, N_2, and N_3 respectively where N_1 and N_2 are always odd numbers. The total number of switchings is equal to N and the equations describing the harmonic elimination PWM are given in (1)–(2).

$$\sum_{i=1}^{N_1}(-1)^{i+1}\cos(a_i)+\sum_{i=N_1+1}^{N_1+N_2}(-1)^{i}\cos(a_i) + \sum_{i=N_1+N_2+1}^{N}(-1)^{i+1}\cos(a_i)=M \tag{1}$$

$$\sum_{i=1}^{N_1}(-1)^{i+1}\cos(na_i)+\sum_{i=N_1+1}^{N_1+N_2}(-1)^{i}\cos(na_i) + \sum_{i=N_1+N_2+1}^{N}(-1)^{i+1}\cos(na_i)=0 \tag{2}$$

where

$$0 \le M \le 3 \tag{3}$$

$$0 < a_1 < a_2 < \ldots < a_N < \frac{\pi}{2} \tag{4}$$

and the amplitude of the fundamental component is:

$$\hat{V_1} = \frac{4 \cdot M}{\pi} \cdot V_{dc} \tag{5}$$

In this paper a fundamental frequency switching pattern is considered meaning that three and four angles per quarter period need to be calculated. For three angles per quarter period, elimination of the first two odd and non-triplen harmonics can be achieved while controlling the fundamental component at the required level. Similarly, three harmonics can be eliminated by using four angles per quarter period, in a switching pattern similar to the triplen harmonic injection discussed later.

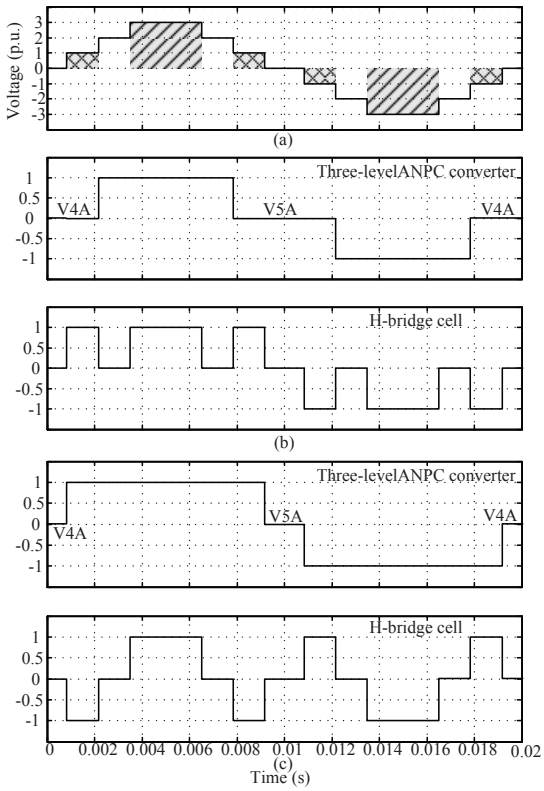

Fig. 5. (a) Output voltage, (b) Switching function (S_{f1}), (c) Switching function (S_{f2})

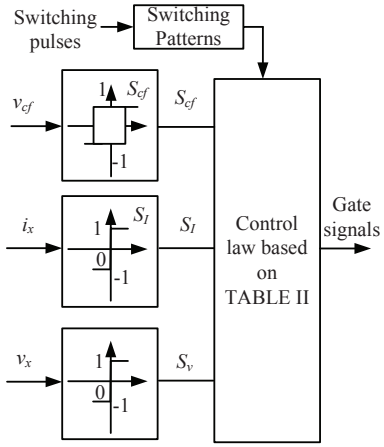

Fig. 6. Block diagram of the FC voltage controller

IV. Flying Capacitor Voltage Control

The regulation of the C_f takes place at output voltage levels $+V_{dc}$ and $-V_{dc}$ and depends upon the polarity of the

TABLE III
SELECTION OF SWITCHING FUNCTIONS

System State		Switching Functions		Effect on C_f
		positive v_x	negative v_x	
$i_x > 0$	$v_{cf} > V_{dc} + h$	S_{f1}	S_{f2}	Discharging
	$v_{cf} < V_{dc} - h$	S_{f2}	S_{f1}	Charging
$i_x < 0$	$v_{cf} > V_{dc} + h$	S_{f2}	S_{f1}	Discharging
	$v_{cf} < V_{dc} - h$	S_{f1}	S_{f2}	Charging

output current. The voltage across the C_f which it is affected by the selection of switching states as mentioned above and regulated through the use of redundant switching states should be maintained at V_{dc}. From Table II, it is observed that the charging and discharging of the C_f depends on the two switching states of the switches of H-bridge cell that connect the capacitor to the output terminal. Assuming the a positive output current, when the switches S_7 and S_{10} are turned on, irrespective of the state of the ANPC converter, C_f charges. When the switches S_8 and S_9 are turned on, C_f discharges. Based on this observation two patterns of switching functions (S_{f1} and S_{f2}) of the three-level ANPC converter and H-bridge cell are evolved which generates same seven-level output voltage, as shown in Fig. 5 and Fig. 7. These patterns are selected in order to regulate the voltage across C_f at its reference level based on the polarity of the output current, polarity of the output voltage and the voltage across C_f.

The block diagram of the FC voltage controller is shown in Fig. 6. The voltage across C_f is compared in a hysteresis comparator and the band of the hysteresis controller defines the switching frequency of each switch. The reference voltage level of C_f is one-quarter of the DC-link voltage. If the FC voltage is higher than upper band limit the state S_{cf} is 1, which implies that the C_f needs to be discharged. If it is less than lower band limit S_{cf} is -1, which implies C_f needs to be charged. The polarity of the output current determines the status (S_I), the comparator generates 1 for positive output current and -1 for negative output current and similarly the polarity of the output voltage determines the status (S_v), the comparator generates 1 for positive output voltage and -1 for negative negative for output voltage. Depending upon the FC voltage, the polarity of the output current and the polarity of the output voltage a suitable switching function is chosen from Table III.

V. SIMULATION RESULTS

The seven-level CAM converter under harmonic elimination modulation control is simulated in MATLAB/SIMULINK [13]. The parameters used in the simulations are similar to those used in the laboratory setup and they are shown in Table IV. Three different loading conditions are investigated and their characteristics are also shown in Table IV with two DC sources of 40V each are connected across the DC-link capacitors. The charging and discharging periods of the FC are shown as shaded region in Fig. 5(a) and Fig. 7(a).

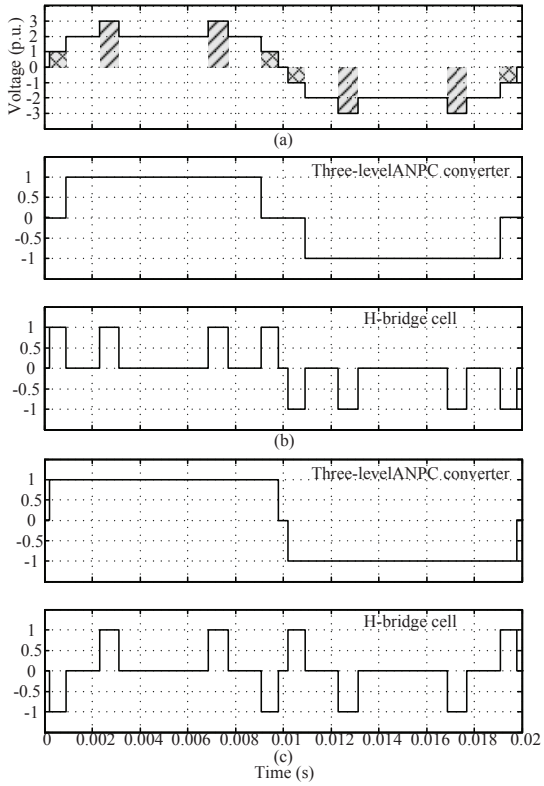

Fig. 7. (a) Output voltage (b) Switching function (S_{f1}) (c) Switching function (S_{f2})

TABLE IV
SIMULATION AND EXPERIMENTAL PARAMETERS

DC-link Voltage	80 V
Flying Capacitor	1000 μ F
DC-link Capacitors	3300 μ F
Band limits for 3 Angles ($\pm h$)	$\pm$0.5 V
Band limits for 3 Angles ($\pm h$)	$\pm$1 V
Load A	R=22Ω, L=30mH
Load B	R=11Ω, L=30mH
Load C	R=11Ω, L=125mH

The voltage across the FC can therefore be maintained to the required level if the overall amount of charge of the FC is at least equal to the discharge amount of the FC over a fundamental period. Since the only states that can be used for regulation of the voltage of the FC are those of the ± 1 p.u. voltage level, the condition can be simplified for the charging and discharging over the half period. This restriction can be rewritten in terms of the load current as shown in eqn. 6.

$$\int_0^{\pi} |i_{charging}|\, d\theta - \int_0^{\pi} |i_{discharging}|\, d\theta > 0 \qquad (6)$$

where $i_{charging}$ is the part of the load current charging the FC and $i_{discharging}$ discharging the FC.

In the first case, three angles are considered over the quarter-

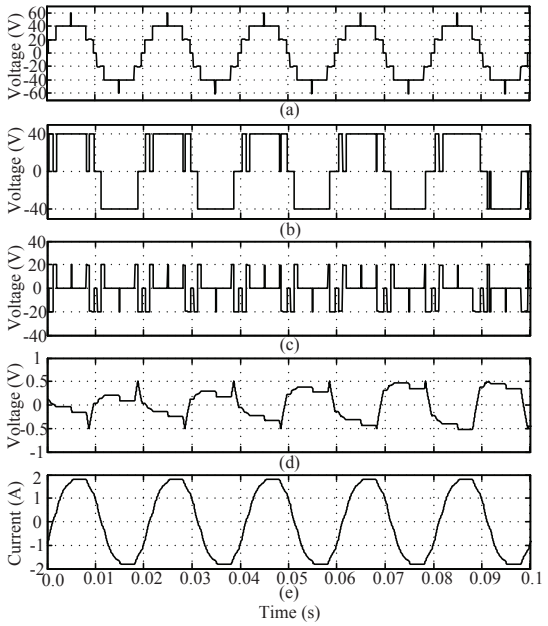

Fig. 8. Simulation results for M = 1.85 and case A load (a) output voltage v_{xO}, (b) three-level ANPC output voltage v_{wO}, (c) H-bridge output voltage v_{xw}, (d) voltage ripple across FC, (e) output current

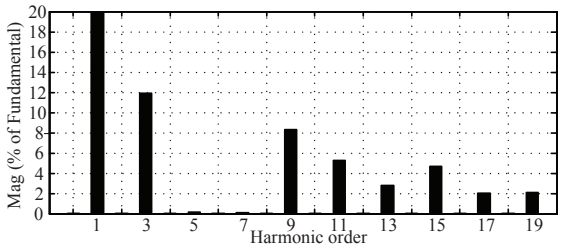

Fig. 9. Harmonic spectrum of output voltage (v_{xO})

period for the $R-L$ load of case A. As shown in Fig. 5(b) and (c), there are two switching functions of the three-level ANPC converter. The selection of the zero voltage level switching states of the three-level ANPC converter is arbitrary and considered as shown in Fig. 5 (b). As shown in Fig. 3 there exist two set of solutions and as the charging and discharging of FC depends on the switching angles and time periods, the voltage across FC cannot be regulated at its reference level for all available solution sets obtained.

The range of M for set 1 is from 1.16 to 2.53 and the voltage across the FC can be regulated up to 1.48. For solution set 2 the range of M is from 1.49 to 1.86 and the voltage across FC can be regulated for the whole modulation index range. Since the regulation of the FC voltage also depends on the load power factor, different limits can be reached for different loads. For load case B and case C, the voltage across the FC can be regulated for whole range of the modulation indices in set 2. However for case B and case C loads and for solution

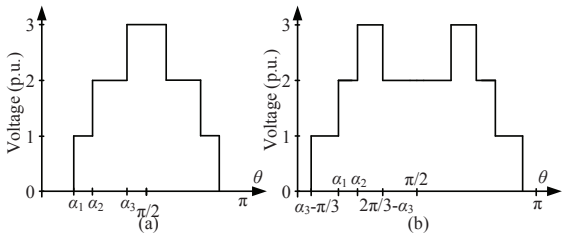

Fig. 10. Output voltage waveform with (a) three-angles per quarter period and (b) third harmonic injection

set 1, the voltage across the FC is regulated up to 1.54 and 2.48 respectively. The simulation results for M=1.85 from set 2 and case A load are shown in Fig. 8. Fig. 8(a)-(c) shows the output voltage v_{xO}, the three-level ANPC output voltage v_{wO}, and the H-bridge output voltage v_{xw} respectively. It is seen in Fig. 8(d) that the FC voltage is regulated at reference voltage level and within the band limits. Different switching functions are selected to regulate of FC voltage, due to which the v_{wO} is asymmetrical over quarter of the period. In order to distribute the losses among the semiconductor devices the influence of FC voltage control need to be considered. Fig. 8 (e) shows the output current. The harmonic spectrum of the output voltage is shown in Fig. 9 where it is seen that the first two non-triplen harmonics (5th and 7th) are eliminated from the output voltage.

In order to increase the charging period and decrease the discharging period during the top and bottom level (V_1 and V_{24}) the number of switching transitions from the second level to the third level are increased to $N_3 = 2$. Such a modification in the output waveform means that higher modulation indices can be achieved also depending on the load power factor.

In the second case, the four switching angles per quarter period are obtained by solving (1)–(2) where one additional harmonics is controlled or by using triplen harmonic voltage injection method [14], where the number of harmonics eliminated from the output voltage spectrum remains similar to the three-angle case. The triplen harmonic injected to the output waveform is given by:

$$V_{triplen}(\theta) = \sum_{n=1,3,5\ldots}^{\infty} \frac{2V_{dc}}{n\pi} \cos(n\alpha_3) \sin(3n\theta) \qquad (7)$$

Here case A and case B loads are considered to investigate for higher modulation indices. Considering third harmonic injection for case A and case B loads, the FC voltage can be regulated up to M=2.07 and M=2.16 respectively. The simulation results for M=2.06 and case B load are shown in Fig. 11. Fig. 11(a)–(c) shows output voltage v_{xO}, v_{wO} and v_{xw} respectively. The band limits considered are shown in Table IV. It is seen in Fig. 11(d) that the FC voltage is regulated at reference voltage level but the voltage also drops lower than the lower band limit. In this case, when the FC voltage is less than the lower band limit, the control commands to change the switching function, however that does not change the discharging behavior of the capacitor. It deviates beyond

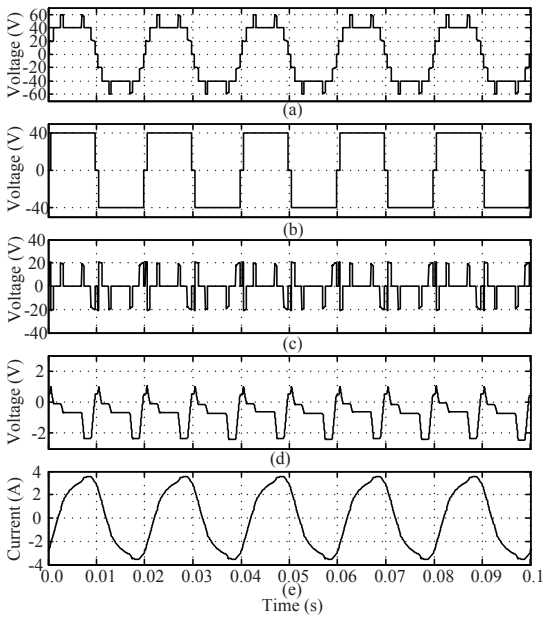

Fig. 11. Simulation results for M = 2.06 and case B load (a) output voltage v_{xO}, (b) three-level ANPC output voltage v_{wO}, (c) H-bridge output voltage v_{xw}, (d) voltage ripple across FC, (e) output current

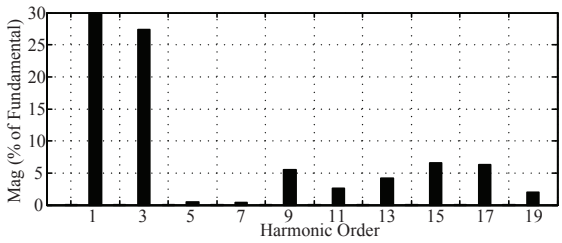

Fig. 12. Harmonic spectrum of output voltage (v_{xO})

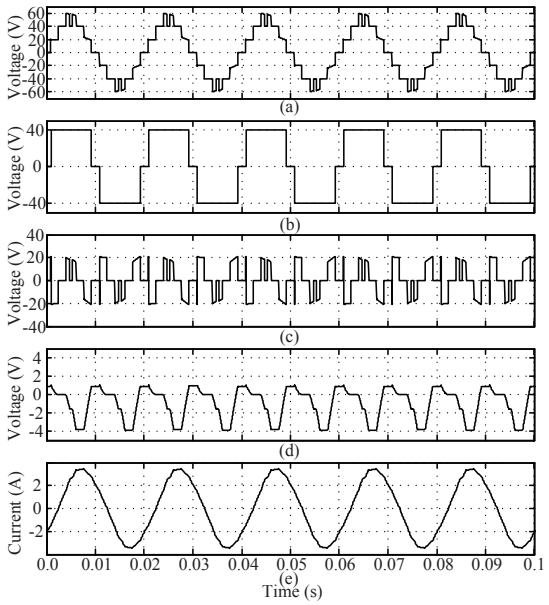

Fig. 13. Simulation results for M = 1.94 and case B load (a) output voltage v_{xO}, (b) three-level ANPC output voltage v_{wO}, (c) H-bridge output voltage v_{xw}, (d) voltage ripple across FC, (e) output current

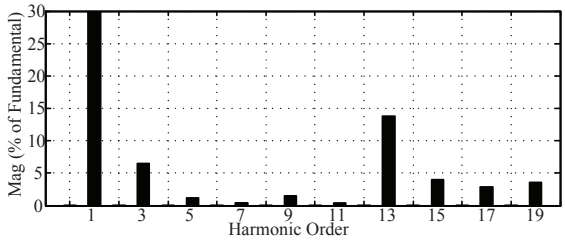

Fig. 14. Harmonic spectrum of output voltage (v_{xO})

the specified band limit and this variation depends upon the magnitude of the output current. This effect can be minimized by increasing the capacitance of FC or increasing number of angles in voltage levels of the output voltage level. Fig. 11(e) shows the output current. The harmonic spectrum of the output voltage is shown in Fig. 12 where it is seen that the first two non-triplen harmonics (5th and 7th) are eliminated from v_{xO}.

Considering four angles per quarter period, for case A and case B loads, the FC voltage can be regulated until M=2.01 and M=2.05 respectively. The simulation results for M=1.94 and case B load are shown in Fig. 13. Fig. 13(a)–(c) shows output voltage v_{xO}, v_{wO} and v_{xw} respectively. The band limits of the hysteresis comparator considered are shown in Table IV. Again the capacitor voltage assumes values less than the lower band voltage because of the inability to control the voltage during the $+3V_{dc}$ and $-3V_{dc}$ voltage levels. The harmonic spectrum of the output voltage is shown in Fig. 14 where it is seen that the first three non-triplen harmonics (5th, 7th and 11th) are eliminated but for the effect of the unbalance in the FC voltage.

VI. Experimental Results

A single-phase seven-level CAM converter system was built in the laboratory to validate the presented FC control strategy. The laboratory setup employed two DC supplies to connect across each DC-link capacitors. The control strategy with switching angles considered above was implemented with dead time of 4μs between the complementary switching signals. The closed loop control strategy was implemented on a dSPACE DS1104 board [15].

Fig. 15 shows the results for three angles per quarter period with M=1.85 and case A load. The voltages v_{xO}, v_{wO} and v_{xw} are shown in Fig. 15 (a) and (b) respectively. Fig. 15 (c) depicts the output current and Fig. 15(d) shows the FC voltage which is regulated at its reference voltage level. In accordance with the simulation results, the first two non-triplen harmonics in the output voltage are eliminated as shown in Fig. 16.

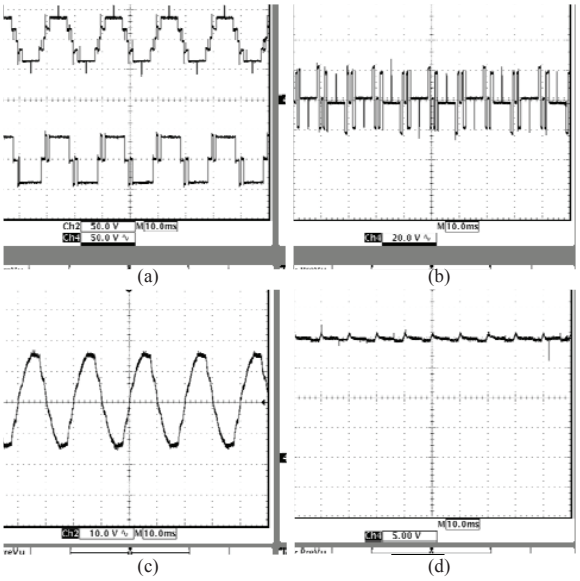

Fig. 15. Experimental results for M = 1.85 with case A load (a) output voltage v_{xO} (top) and three-level ANPC output voltage v_{wO} (bottom) (b) H-bridge output voltage v_{xw} (c) output current and (d) voltage across FC

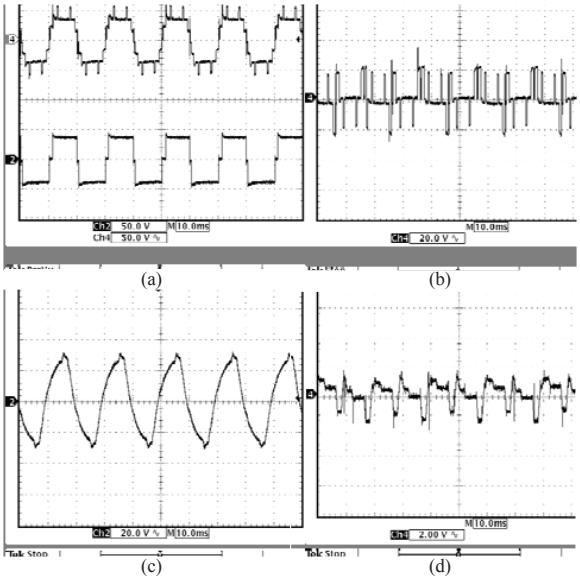

Fig. 17. Experimental results for M = 2.06 with case A load (a) output voltage v_{xO} (top) and three-level ANPC output voltage v_{wO} (bottom) (b) H-bridge output voltage v_{xw} (c) output current and (d) voltage ripple across FC

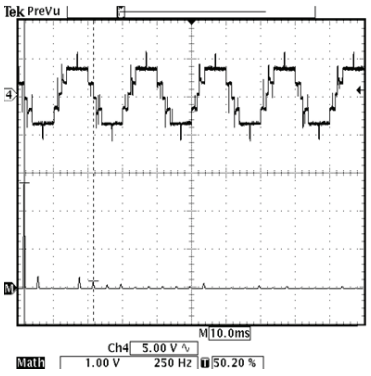

Fig. 16. Measured output voltage (v_{xO}) for M = 1.85 with case A load and its associated harmonic spectrum

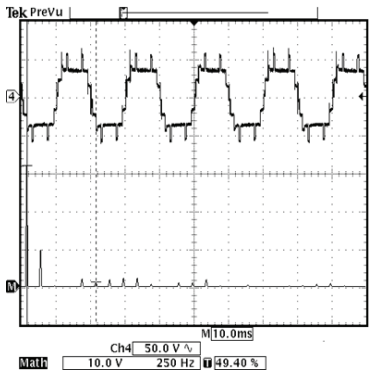

Fig. 18. Measured output voltage (v_{xO}) for M = 2.06 with case B load and its associated harmonic spectrum

In order to extend FC voltage regulation to higher modulation indices both the triplen harmonic injection method and the four angles per quarter period ($N_3 = 2$) are verified for both case A and B loads experimentally. In Fig. 17(a) and (b), the voltages v_{xO}, v_{wO} and v_{xw} are shown for M=2.06 and case B load using the triplen harmonic injection method. Fig. 17(d) shows the FC voltage which is regulated at its reference voltage level. Fig. 17 shows v_{xO} and corresponding spectrum using the triplen harmonic injection method for M=2.06 and case B load. In accordance with the simulation results, the first two non-triplen harmonics in the output voltage are eliminated.

In case B load, the magnitude of the output current is high due to which the rate of discharge in FC is more. In Fig. 19 (a) and (b), the voltages v_{xO}, v_{wO} and v_{xw} are shown for M=1.94 and case B load. Fig. 19(d) shows the FC voltage which is regulated at its reference. Fig. 20 shows the v_{xO} and corresponding spectrum for M=1.96 and case B load. In accordance with the simulation results, the first three non-triplen harmonics in the output voltage are eliminated as shown. Using four angles per quarter period both the extension in FC voltage control at higher modulation indices and increase in bandwidth of the output voltage are achieved.

VII. Conclusions

A seven-level converter based on the cascaded connection of a three-level ANPC converter and individual H-bridge cell for each phase is investigated using fundamental frequency harmonic elimination PWM. The topology only requires a single DC source and extends the operation range of converters with similar DC-link voltage providing an boost feature. The FC voltage control for various load characteristics and switching angles distribution over quarter period are investigated where

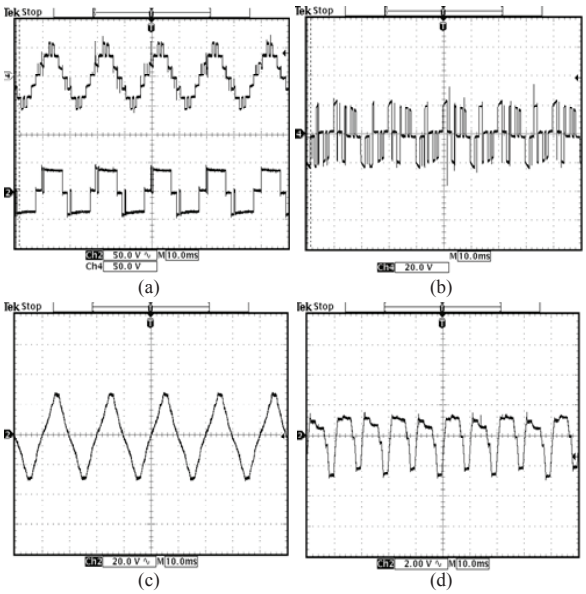

Fig. 19. Experimental results for M = 1.94 with case A load (a) output voltage v_{xO} (top) and three-level ANPC output voltage v_{wO} (bottom) (b) H-bridge output voltage v_{xw} (c) output current and (d) voltage across FC

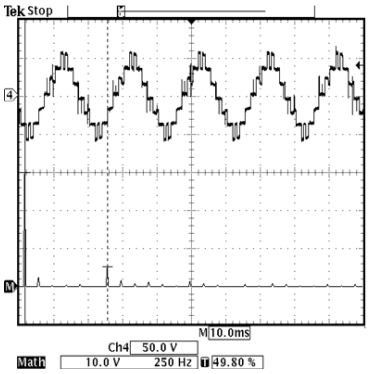

Fig. 20. Measured output voltage (v_{xO}) for M = 1.94 with case B load and its associated harmonic spectrum

it is observed that for more inductive loads the FC voltage regulation can be achieved for higher modulation indices. This behavior makes the converter with fundamental frequency harmonic elimination modulation control more suitable for reactive power compensation. The use of the ANPC converter over the NPC one can improves the loss distribution among each phase semiconductor devices. The performance of the presented control strategy using harmonic elimination modulation method has been validated by simulation and experimental results.

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