An n-level flying capacitor based active neutral-point-clamped converter

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An n-level flying capacitor (FC) based active neutral point clamped (ANPC) converter is discussed in this paper. The converter is based on an arrangement of a three-level ANPC converter and a number of two-level cells creating an n-level line-to-neutral waveform. The converter is operated under a phase-shifted carrier pulse-width modulation (PWM). The mathematical model for the DC-link capacitors voltage behavior of a three-phase arrangement is also presented. It is shown through simulations and experimental work that the voltage of flying capacitors can naturally balance to the required level in order to generate multilevel waveform. Simulations and experimental work of a single-phase seven-level ANPC converter prototype are also presented.

Keywords
active, capacitor, flying, n, level, converter, clamped, point, neutral

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An n-Level Flying Capacitor based Active Neutral-Point-Clamped Converter

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Abstract—An n-level flying capacitor (FC) based active neutral point clamped (ANPC) converter is discussed in this paper. The converter is based on an arrangement of a three-level ANPC converter and a number of two-level cells creating an n-level line-to-neutral waveform. The converter is operated under a phase-shifted carrier pulse-width modulation (PWM). The mathematical model for the DC-link capacitors voltage behavior of a three-phase arrangement is also presented. It is shown through simulations and experimental work that the voltage of flying capacitors can naturally balance to the required level in order to generate multilevel waveform. Simulations and experimental work of a single-phase seven-level ANPC converter prototype are also presented.

Index Terms—Active neutral point clamped converter, carrier based pulse-width modulation, flying capacitor converter, multilevel converter

I. INTRODUCTION

Multilevel converters have become popular in recent years due to their high-voltage and high-power capability [1]. They have numerous advantages such as lower harmonic distortion and lower electro-magnetic interference (EMI) and reduced stress of the semiconductor switching devices when compared with the conventional two-level converter. These advantages have made them particularly attractive for industrial applications such as motor drives [2], advanced static compensators (STATCOMs) [3], high-power high-voltage direct-current (HVDC) power transmission [4], etc.

The main multilevel converter topologies are the neutral-point clamped (NPC), the flying capacitor (FC) converter and the cascaded H-bridge (CHB) converters [1]. As the number of levels in the output voltage of a multilevel converter increases, the complexity of the neutral point voltage control of the NPC converter, the stored energy components of the FC converter and the number of isolated power supplies of the cascaded H-bridge converter increases. This increase in complexity together with the increase in the number of components affects the reliability and the efficiency of the converter [5].

In recent years, hybrid multilevel converters using different arrangements of conventional multilevel topologies have been introduced. These include the three-level active neutral point clamped converter (ANPC) converter [6] with a FC converter generating a five-level (5L) output waveform, the two-level converter with an H-bridge cell which generates a five-level output waveform and the three-level NPC converter with an H-bridge cell [5] which generates a seven-level (7L) output waveform.

Based on the hybrid configuration of a 3L-ANPC converter [6] and a 3L FC converter, a 5L-FC based ANPC converter was developed for motor drive applications [7]. In [8], the experimental validation of the 5L-FC based ANPC converter using carrier based disposition (CBD) pulse-width modulation (PWM) to control the neutral point voltage and FC voltage were presented. In [9], a 5L-FC based ANPC converter for STATCOM application with phase shifted carrier (PSC) PWM using simulation results is verified.

Hybrid configurations also provide the advantage of combining high-volume semiconductors such as the integrated gate-commutated thyristor (IGCT) and insulated gate bipolar thyristor (IGBT) in order to decrease the conduction losses [10]. Optimized pulse patterns with low switching frequency to deal with voltage balancing and switching frequency issues were presented in [11] and the control under selective harmonic elimination PWM was proposed in [12].

The objective of this paper is to discuss a generalized n-level FC-based ANPC converter operated with PSC-PWM. The PSC-PWM provides natural balancing of FCs [13] and under this modulation scheme both FCs and DC-link capacitors of this converter topology balances to required voltage level. The DC-link capacitors behavior is mathematically derived for three-phase arrangement where the average value of neutral point current over fundamental period is zero when the voltage across the DC-link capacitors and FCs naturally balance.

The paper is organized in the following way. Section II describes the topology and operating principles of the n-level FC based ANPC converter. Section III discusses the phase-shifted carrier based modulation technique and the mathematical model of the DC-link capacitors voltage behavior. Section IV provides simulation results and Section V presents experimental results from a single-phase low-power seven-level laboratory setup. Finally, the conclusions are summarized in Section VI.

II. TOPOLOGY AND OPERATION PRINCIPLES

Fig. 1(a) presents the phase leg of the n-level (FC) based ANPC converter topology. It is the arrangement of a 3L-ANPC converter and z number of two-level cells. The number of output voltage levels in the line-to-neutral waveform is equal to $n = 2z + 3$ where n is an odd number. The n-level FC
ANPC converter and the two switching states of each of the two-level cells resulting in a total of \(4 \cdot 2^n\) switching states which generate the \(n\) different voltage levels at the output. The output phase voltage, \(v_{rxO}\), where \(x\) is the phase (\(a, b\) or \(c\)) is given by:

\[
v_{rxO} = V_{dc} \left[ \frac{(n-1)}{2} (S_{z5} - 1) + (S_{x3} + S_{xy(n-4)} + \ldots + S_{xy1}) \right]
\]

The voltage ripple across the FC depends on the amplitude of the load current and the switching frequency of the switches \(S_{z3}, S_{z4}\) and the switches of two-level cells [10]. The current through the FC \(C_{f,xy(n-6)}\) can then be expressed as:

\[
I_{Cf,xy(n-6)} = (S_{xy(n-4)} - S_{xy(n-6)}) \cdot i_{rx}
\]

The required capacitance of the flying capacitor for a peak output current of \(I_p\) allowed voltage ripple \(\Delta V_{Cf}\) and carrier frequency of \(f_s\) is given by eqn. 3 [9].

\[
C_f = \frac{I_p}{\Delta V_{Cf}} \cdot \frac{1}{f_s}
\]

The energy stored per-phase-leg of the \(n\)-level FC based ANPC converter is also presented in [8]. As the number of levels increases, the energy stored in the flying capacitors increases linearly. In order to decrease the energy stored in FCs as the number of levels increases, a higher switching frequency can be utilized. This, however, increases the switching losses and the trade-off between the switching losses and the energy storage of the capacitors has to be made.

III. PHASE-SHIFTED CARRIER PWM

A. Modulation Strategy

The modulation of the \(n\)-level FC based ANPC converter is based on a PSC PWM. The PSC-PWM provides natural balancing of the FC converters [13] and can be readily applied to the topology under discussion. Since additional number of levels can be acquired by the fundamental frequency switching of the 3L-ANPC, only \(\frac{n-1}{2}\) triangular carrier signals are required. The phase shift between these triangular carrier signals is \(\frac{720}{n}\) degrees, or double the phase shift for an equal level FC or CHB topology. The harmonics are positioned as sidebands around \(\frac{(n-1)}{2}f_s\). This modulation technique fulfills the two basic requirements set in [8] as the voltage balancing of the flying capacitors is provided by the PSC-PWM and the switching frequency of the outer switches of the topology is equal to the fundamental frequency of the output voltage.

The modulating signal for the converter is a function of both the desired output voltage and the switching function of the switch \(S_{z5}\) [9] and is given by eqn. (4).

\[
v_{rx} = 2 \cdot m_a \cdot \sin(\omega_0 t) - \left( \frac{A}{\pi} \sum_{n=1,5,\ldots}^{\infty} \frac{1}{n} \sin n\omega_0 t \right)
\]

where \(m_a\) is the amplitude modulation index and \(\omega_0\) is the angular frequency of the fundamental component. The
modulating signal and a triangular carrier waveform are shown in Fig. 2. The value of \( m_a \) is normalized with the overall number of levels and it ranges between 0 and 1 for any \( n \). The number of levels in the output voltage waveform also depends on the amplitude modulation index and for every \( \frac{1}{n-1} \) decrease in \( m_a \), the number of levels in the output waveform decreases by two.

**B. Mathematical modeling of the DC-link capacitor voltage behavior for three-phase converter arrangement**

The analysis of the DC-link capacitor voltage behavior for the \( n \)-level FC based ANPC converter using PSC-PWM is discussed in this section. The switching functions of the switches, determine the relation between the AC- and DC-side variables. Voltages of the AC-side of the ANPC converter are given by eq. (1):

\[
\begin{align*}
v_{raO} & = V_d \left[ \frac{(n-1)}{2} (S_{a5} - 1) + (S_{a3} + \ldots + S_{a91}) \right] \\
v_{rbO} & = V_d \left[ \frac{(n-1)}{2} (S_{b5} - 1) + (S_{b3} + \ldots + S_{b91}) \right] \\
v_{rcO} & = V_d \left[ \frac{(n-1)}{2} (S_{c5} - 1) + (S_{c3} + \ldots + S_{c91}) \right]
\end{align*}
\]

(5)

(6)

(7)

Considering the AC-side three-phase currents as:

\[
\begin{align*}
i_a(t) & = I_p \sin(\omega_0 t + \phi) \\
i_b(t) & = I_p \sin(\omega_0 t + \phi - \frac{2\pi}{3}) \\
i_c(t) & = I_p \sin(\omega_0 t + \phi + \frac{2\pi}{3})
\end{align*}
\]

(8)

(9)

(10)

The currents of the DC-side of the converter are given by

\[
\begin{align*}
i_1 & = i_a \cdot S_{a5} \cdot S_{a3} + i_a \cdot S_{b5} \cdot S_{b3} + i_a \cdot S_{c5} \cdot S_{c3} \\
i_0 & = i_a (S_{a5} + S_{a3}(1 - 2S_{a5})) + i_b (S_{b5} + S_{b3}(1 - 2S_{b5})) + i_c (S_{c5} + S_{c3}(1 - 2S_{c5})) \\
i_2 & = i_a \cdot S_{a8} \cdot S_{a4} + i_a \cdot S_{b8} \cdot S_{b4} + i_a \cdot S_{c8} \cdot S_{c4}
\end{align*}
\]

(11)

(12)

(13)

At any given time, the switching function can be approximated by the instantaneous value of the modulating waveform, given that carrier frequency is much larger than converter output frequency. The continuous switching functions for switches of phase \( a \) are

\[
\begin{align*}
\hat{S}_{a3} & = 1 + m_a \sin(\omega_0 t) - 1 + \frac{4}{n} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\omega_0 t) \\
\hat{S}_{a4} & = m_a \sin(\omega_0 t) - 1 + \frac{4}{n} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\omega_0 t) \\
\hat{S}_{a5} & = \left\{ \begin{array}{ll}
1 + \frac{4}{n} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\omega_0 t) & 0 \leq \omega_0 t \leq \pi \\
0 & \pi \leq \omega_0 t \leq 2\pi
\end{array} \right.
\end{align*}
\]

(14)

(15)

(16)

(17)

Thus the average value of current \( i_1 \) over one cycle of modulating waveform is given as

\[
\bar{i}_1 = \frac{1}{2\pi} \int_0^{2\pi} (i_a \cdot S_{a5} \cdot S_{a3} + i_a \cdot S_{b5} \cdot S_{b3} + i_a \cdot S_{c5} \cdot S_{c3}) d(\omega_0 t)
\]

(18)

\[
\bar{i}_1 = \frac{3m_a I_p \cos(\phi)}{4}
\]

(19)

Similarly from the integration of eqn. (12)

\[
\bar{i}_0 = 0
\]

(20)

and from eqn. (13)

\[
\bar{i}_2 = \frac{1}{2\pi} \int_0^{2\pi} (i_a \cdot S_{a8} \cdot S_{a4} + i_a \cdot S_{b8} \cdot S_{b4} + i_a \cdot S_{c8} \cdot S_{c4}) d(\omega_0 t)
\]

(21)

\[
\bar{i}_2 = \frac{3m_a I_p \cos(\phi)}{4}
\]

(22)

Considering the power balance equation between the DC and the AC-side of the \( n \)-level ANPC converter, the following are obtained

\[
V_{dc} \bar{i}_{dc} = \frac{1}{2\pi} \int_0^{2\pi} (v_{ra} + v_{rb} + v_{rc}) d(\omega_0 t)
\]

(23)

\[
\bar{i}_{dc} = \frac{3mI_p \cos(\phi)}{4}
\]

(24)

\( \bar{i}_{dc} \) is the average value of \( i_{dc} \) over one cycle of the modulating waveform. Using the above deduced equations the following are obtained

\[
\bar{i}_{C1} = \bar{i}_{dc} - \bar{i}_1 = 0
\]

(25)

\[
\bar{i}_{C2} = \bar{i}_{C1} - \bar{i}_0 = 0
\]

(26)

When the voltage across the capacitors naturally balances using PSC-PWM, the average value of the DC-link capacitors current and neutral point current is zero.
IV. Simulation Results

Simulations have been performed based on a seven-level topology (Fig. 3). In this case, charging and discharging of the two flying capacitors $C_{f,y3}$ and $C_{f,y1}$ takes place at 1 p.u and 2 p.u of the output line-to-neutral voltage and depends upon the direction of the output phase current. The switching states for the case of the seven-level topology are shown in Table I. During the switching states $V_2$, $V_7$, $V_{11}$ and $V_{14}$ both the FCs are connected to the load and one of the capacitors charges while the other discharges. In the remaining states that provide 1 p.u or 2 p.u voltage levels, only one of the two FCs is connected to the output. Also during switching states, $V_7$ and $V_{14}$ the neutral point $O$ is connected to the load through the FCs.

The switching signals and the intervals where either or both the FCs are connected to the load during a fundamental period are shown in Fig. 4. The system parameters and load configurations for both the simulation and experimental results are summarized in Table II. The behavior of the topology and especially the voltage balancing of the flying capacitors is investigated not only under steady-state operation but also during changes in the DC voltage. Fig. 5 shows the phase output voltage and the voltage across the flying and DC-link capacitors and Fig. 6 shows the load current and current through the flying capacitors of the seven-level topology.

The dynamic behavior of the converter for a step change in the DC-link voltage is also simulated for the two possible arrangements of the triangular carrier waveforms (leading and lagging). The simulated results are shown in Fig. 7(a) and (b) for leading and lagging arrangements respectively. As expected the leading carrier arrangement results in a faster response from capacitor $C_{f,y1}$ and the lagging carrier arrangement results in an initial dip in the voltage of capacitor $C_{f,y1}$ and a faster response to the transient change from capacitor $C_{f,y3}$. These results are in accordance with the behavior of a flying capacitor converter under similar changes in the DC-link voltage [13].

<table>
<thead>
<tr>
<th>Table I</th>
<th>Switching States of Seven-Level FC Based ANPC Converter</th>
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<tbody>
<tr>
<td>$S_3$</td>
<td>$S_4$</td>
</tr>
<tr>
<td>$V_1$</td>
<td>1</td>
</tr>
<tr>
<td>$V_2$</td>
<td>1</td>
</tr>
<tr>
<td>$V_3$</td>
<td>0</td>
</tr>
<tr>
<td>$V_4$</td>
<td>0</td>
</tr>
<tr>
<td>$V_5$</td>
<td>1</td>
</tr>
<tr>
<td>$V_6$</td>
<td>0</td>
</tr>
<tr>
<td>$V_7$</td>
<td>0</td>
</tr>
<tr>
<td>$V_8$</td>
<td>0</td>
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<tr>
<td>$V_9$</td>
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<tr>
<td>$V_{10}$</td>
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</tr>
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<td>$V_{11}$</td>
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<td>$V_{13}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_{14}$</td>
<td>1</td>
</tr>
<tr>
<td>$V_{15}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_{16}$</td>
<td>0</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Table II</th>
<th>Simulation and Circuit Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-link voltage</td>
<td>300V</td>
</tr>
<tr>
<td>DC-link capacitors $C_1$ and $C_2$</td>
<td>4700μF</td>
</tr>
<tr>
<td>Flying capacitors</td>
<td>1000μF</td>
</tr>
<tr>
<td>Carrier Frequency</td>
<td>1500Hz</td>
</tr>
<tr>
<td>Fundamental Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>22 Ω</td>
</tr>
<tr>
<td>Load Inductance</td>
<td>7mH</td>
</tr>
</tbody>
</table>

V. Experimental Results

A single-phase laboratory prototype of a seven-level FC based ANPC converter was used to verify the natural balancing
phenomenon of the FCs using PSC-PWM. The converter is built using the FUJI 2MBI100TA-060 and a dSPACE 1104 R&D DSP board. The laboratory setup employed a controllable DC-supply attained from a three-phase passive front end rectifier and a transformer to maintain the DC-link voltage.

The steady state performance of the topology is initially investigated. Fig. 8 shows the line-to-neutral phase output of and the corresponding harmonic spectrum of the single-phase circuit for an amplitude modulation index of 0.85. The measured load current and currents through the two flying capacitors are also shown in Fig. 9. Finally, Fig. 10 shows the DC-link voltage and the voltage of the flying capacitors over 10 fundamental periods (0.4 sec). The natural balancing of the flying capacitors due to the PSC-PWM method and their corresponding voltage ripple due to the load current can also be observed.

The behavior of the single-phase circuit under a step change in the DC-link voltage of 100V (i.e. from 200V to 300V) is also investigated for both leading and lagging carrier waveforms. The transient responses for the case of the leading and lagging carrier arrangement are shown in Figs. 11 and 12 respectively. Due to the PSC-PWM of the flying cells of the topology and the fundamental frequency switching of the outer switches, which result in a circuit as shown in Fig. 1(b) and (c), the transient behavior of the topology for both carrier arrangements is similar to that of a FC converter. The experimental results appear to be over-damped when compared to the simulation results possibly because of the non-linear nature of the load inductance for the specific current range and the variation of the load resistance with frequency.

VI. CONCLUSION

The topology, operational principles and theoretical considerations of a generalized \( n \)-level flying capacitor based, active neutral-point clamped converter has been discussed in this paper. The converter is operated with PSC-PWM providing fundamental frequency switching of the outer switches and voltage balancing of the flying capacitors through the natural balancing property. Simulations results and closely matched experimental results are also provided that verify the operational principles of the topology.

REFERENCES


**Fig. 8.** Measured output phase voltage and corresponding harmonic spectrum

**Fig. 9.** Measured load and floating capacitor currents

**Fig. 10.** Measured DC-Link and flying capacitor voltages and flying capacitor voltage ripple

**Fig. 11.** Dynamic response to a 100V step change in the DC-link voltage, leading carrier arrangement

**Fig. 12.** Dynamic response to a 100V step change in the DC-link voltage, lagging carrier arrangement

**Fig. 13.** Leading carrier arrangement

**Fig. 14.** Lagging carrier arrangement


