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Abstract

Self-mixing interferometry (SMI) signals are observed from a sensing system consisting of a laser diode with external optical feedbacks. SMI signals carry the information associated to both of the displacement and parameters of the SL. To retrieve the information precisely, pre-processing of SMI signals is the first key step. For achieving real-time, and high quality sensing, this paper proposes a Field-programmable gate arrays (FPGA) based filtering and normalizing processing for SMI signals. According to the noise features contained in SMI signal, a median filter and a wavelet transform based filter are combined for our design. Hardware co-simulation verified that the performance for this FPGA used filter design.

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FPGA based Filter Design for Self-mixing Interferometry Signals

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ABSTRACT

Self-mixing interferometry (SMI) signals are observed from a sensing system consisting of a laser diode with external optical feedbacks. SMI signals carry the information associated to both of the displacement and parameters of the SL. To retrieve the information precisely, pre-processing of SMI signals is the first key step. For achieving real-time, and high quality sensing, this paper proposes a Field-programmable gate arrays (FPGA) based filtering and normalizing processing for SMI signals. According to the noise features contained in SMI signal, a median filter and a wavelet transform based filter are combined for our design. Hardware co-simulation verified that the performance for this FPGA used filter design.

Keywords: self-mixing interferometry, pre-processing, field programmable gate arrays, wavelet transform, normalization

1. INTRODUCTION

The optical feedback self-mixing interferometry (SMI) technique has been an attractive research field in the last two decades[1]. Sensors based on this effect are extensively used to measure distance[2], displacement and vibrations[3-5]. The SMI effect happens when the reflected or backscattered laser light from a distant target ahead of the laser, re-enters the laser cavity, resulting in the variance of both the amplitude and the frequency of the lasing field. The modulated laser power, called SMI signal, is detected by a photodiode (PD). SMI signals carry the information associated to both the displacement[4] and parameters of SLs[7-9].

To retrieve the information precisely, pre-processing of SMI signals is an important step. In 2007, according to noise features, Yu et.al proposed a filtering method combined by a median filter and a band-pass filter based on Kaiser window function[6]. And Wei presented a neural network interpolation technique for the noise elimination of SMI signals[10]. However, both of the two methods can change the positions of sharp transitions of SMI signals and this change can decrease SMI sensing accuracy. And our recent work proposes a wavelet transform based filtering method which can solve above problem[24]. This algorithm[24] was implemented using Matlab.

As for real-time high-quality sensing in industrial applications, a compact SMI system is important. That is a small-size high-integration chip is needed to replace a PC for signal processing. Recent years, digital signal processing accomplished on Field-programmable gate arrays (FPGAs) is widely used for high-speed, real-time signal processing, because FPGAs are advantageous on merging digital signal processing algorithms with other control logic. It can provide a feasible processing without scarifying accuracy or suffering extra communication latency[11].Therefore, combining FPGA with SMI system is a good solution for the real-time sensing.

This paper proposes a FPGA based filtering and normalizing processing for SMI signals. The sensing signal acquired from the SMI system is sent into the FPGA board and processed. This FPGA based SMI system is demonstrated in Figure 1. This paper is organized as following. Basic theory of SMI effect is presented in Section 2. Section 3 depicts the FPGA design for the filters and the normalization unit. Section 4 shows the real-time simulation implemented by co-hardware simulation method. Conclusion is given in Section 5.

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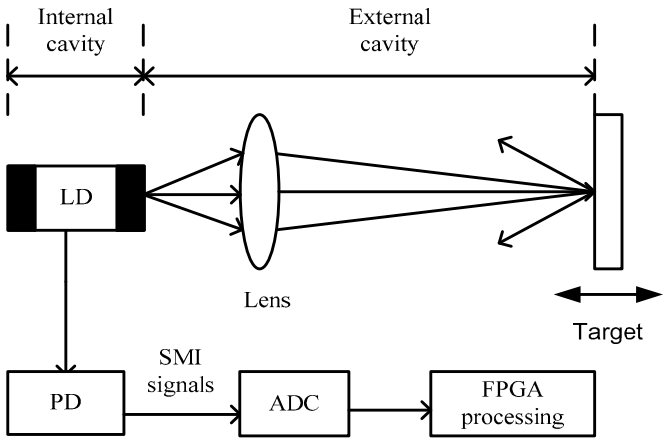

Figure 1. Basic structure of the FPGA based SMI system

2. BASIC THEORY

The basic theoretical model for SMI systems is developed from Lang and Kobayashi[15], and this model is re-presented as the following equations [3, 4, 9-11]:

$$\phi_F[n] = \phi_0[n] - C\sin(\phi_F[n] + \arctan[\alpha]) \quad (1)$$

$$P[n] = P_0(1 + m \times g[n]) \quad (2)$$

$$g(n) = \cos(\phi_F(n)) \quad (3)$$

$$\phi_0(n) = 4\pi L(n)/\lambda_0 \quad (4)$$

n	discrete time index
ϕ_F	external light phase of a LD with feedback
ϕ_0	external light phase of a free running LD
$P[n]$	laser intensity with feedback
P_0	laser intensity without feedback
m	modulation index
$g[n]$	an SMI signal
C	feedback level factor
α	linewidth enhance factor
$L[n]$	external cavity length
λ_0	emitted laser wavelength without feedback

Table 1. Meanings of parameters in Equations (1)-(4)

SMI signals, which have a fringe pattern similar to the traditional interference signals, have been widely studied on in depth[4, 12-13]. When feedback level is increasing, the behavior of SLs can be classified into different feedback regimes[14]. The waveforms of the SMI signals are sinusoid-like, in weak optical feedback regime, while the signals exhibit hysteresis and the waveforms are saw-tooth shaped in both the moderate and strong feedback regimes. For the convenience of the description for FPGA design, we plot a simulated SMI signal waveform using Equations (1)-(4) with C =3, α =3 based on this model in Figure 2. There are characteristic points in the SMI signal waveform, such as sharp transitions, zero-crossing points and peak points, which include information related to the parameters of LDs[9] and the moving information of the external target[16]. According to Equation (3), a normalized SMI signal varies in the range of [-1, 1]. All those characteristic points in SMI signals should be accurately selected so that a high-quality sensing can be achieved[9]. However, due to inevitable noise existing in a practical SMI system, these important points are contaminated.

In our recent work[24], we proposed a wavelet transform based method which is able to effectively remove the noise affection on these points. In Section 3, we implement this method based on FPGA design.

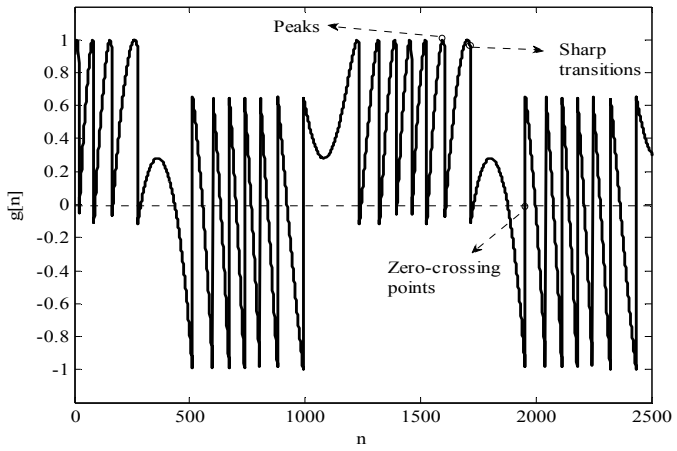

Figure 2. A simulated SMI signal with C =3, α =3 in the moderate optical feedback regime.

3. FPGA DESIGN

The FPGA based pre-processing unit contains two parts, a de-noising part and a normalization part. The de-noising method[24] is employed for the FPGA design. The basic structure is as shown in Figure 3. The FPGA based SMI system is shown as in Figure 3. Since the values of the SMI signal power detected from the sensing system are always signed real numbers and main part of the algorithm is digital processing, system generator for Digital Signal Processing (DSP) is utilized for the design for convenience. This tool is a leading high-level tool for designing high-performance DSP systems using FPGAs, whose key feature is DSP modeling: build and debug a high-performance DSP system in Simulink using the Xilinx Blockset[22]. This filtration system is built in Simulink and some blocks that Xilinx does not provide are implemented using Blackbox, which is an interface between source Hardware Description Language (HDL) codes and Simulimk models. After the completion of the design, it is converted to Verilog HDL codes and can be operated in Xilinx ISE.

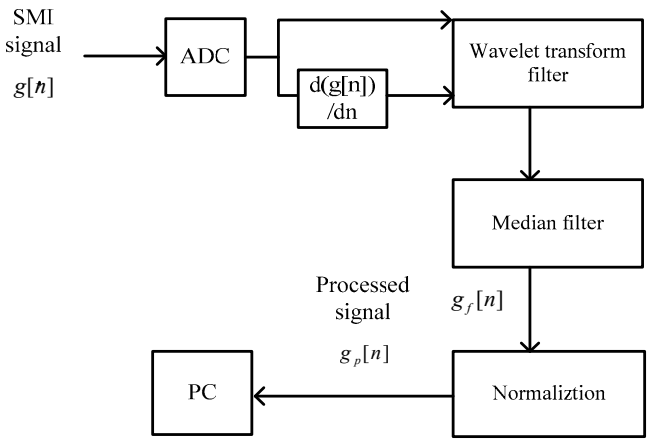

Figure 3. Basic structure of FPGA based SMI signal pre-processing

3.1 Median filter FPGA based design

The length of the sparkles in these SMI signal obtained in our experiment set-up is usually no more than 5 sampling points, so a 5-points median filter is applied. Before passing data into a median filter, a data acquisition block is needed to import 5 subsequent data points, and 5 registers can be used for this. The flow chart of a median filter is shown as

below in Figure 4. R_{ij} represents registers and C_{ij} denotes compare-swappers. The basic principle of this median filter is to sort the 5 points and pick the median value to replace the current processed point. The five points obtained from the acquisition block are sent into C_{11} and C_{12} in pairs and R_{11} at the first level. The compare-swappers compare their values and send the smaller output into the comparison block below at the next level, the larger one into the comparison block above, just as that C_{11} puts its smaller output into C_{21} and the other one into C_{22}. After 5 level's comparison, the 5 points is being descended and the median value is easily picked out.

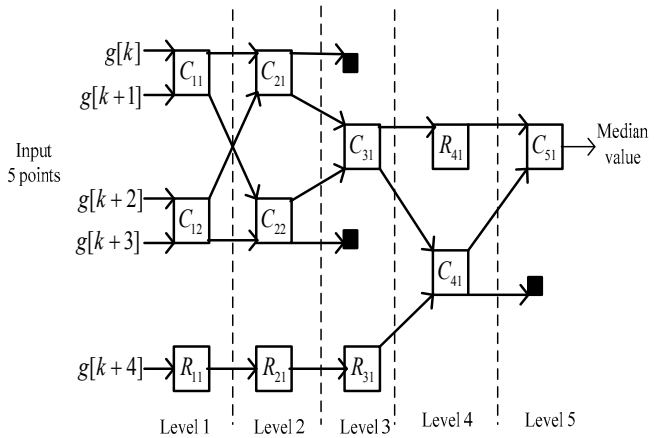

Figure 4. The flow chart of the design of the median filter, g[k] is a data point in SMI signals.

3.2 Wavelet transform filter realization FPGA based design

This part describes the FPGA implementation of the wavelet transform based filter proposed in our recent work[24]. For the convenience of depicting the design, the process of this wavelet transform based filtering method is simply summarized as following steps:

1. Discrete wavelet transform is applied on SMI signals;
2. Single level reconstruction is applied on each frequency component;
3. High frequency content is spatially filtered with the positions of sharp transitions detected by a differential unit. In this step, the transitions in the high frequency content are preserved and noise is filtered.
4. Filtered high frequency component is combined with low frequency component to reconstruct a processed SMI signal.

The core blocks of the wavelet transform based filter, low- and high-pass filters, are accomplished using Distribute Arithmetic (DA). An output of an N-order FIR can be derived as linear convolution:

$$y[n] = \sum_{k=0}^{N-1} H[k]g[n-k] \tag{5}$$

and where $g[n]$ is an input signal and $H[k]$ are the coefficients of a FIR filter. A hardware realization using traditional multiplier-accumulator (MAC) costs N multiplication and (N-1) addition. It is a waste of both of resources and time. DA is an efficient algorithm to realize sum of products which has a parallel processing structure. And this equation can be redistributed as below according to DA[23]:

$$y[n] = -2^{B-1}\sum_{k=0}^{N-1} H[k]g_{B-1}[n-k] + \sum_{b=0}^{B-2} 2^b \sum_{k=0}^{N-1} H[k]g_b[n-k] \tag{6}$$

where $g_b[n-k]$ represents the b_{th} bit position of the number's binary representation. The key is to realize that the second summation can be mapped to a Look Up Table (LUT). The coefficients are known and the values are either 1 or 0 then each multiplication is just a combination of the coefficients for which a true table can be constructed.

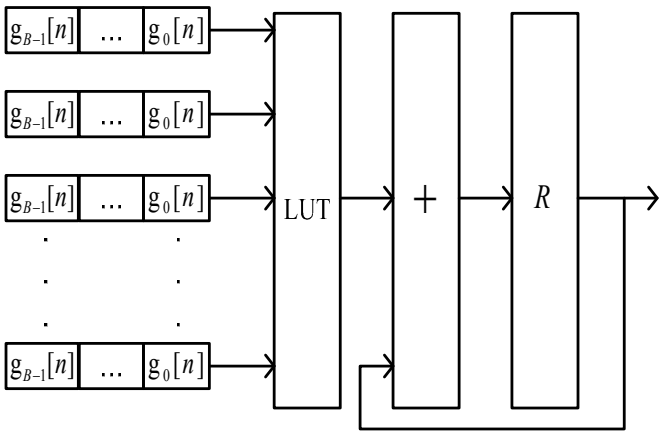

Figure 5. DA for low- and high-pass filter.

After passing the low- and high-pass filters, down- and up-sampling are applied to all frequency parts to reconstruct the frequency component at different scales. This down-sampling operation is to discard odd terms, and up-sampling can be completed by interpolating zeros between two adjacent terms in the down-sampled frequency content. Since an operation of up-sampling is taken just after the down-sampling, these two operations can be accomplished by using the same first-in-first-out (FIFO) Intellectual Property (IP) core provided by Xilinx. The design of this part is shown in Figure 6. After the data obtained from an FIFO block, a multiplexer (MUX) is employed to make the oven terms been kept and odd terms changed into zeros, which accomplishes down- and up-sampling at the same time. The MUX is controlled by a counter which only has two states, 0 or 1, to select to pass the terms or make them as zeros.

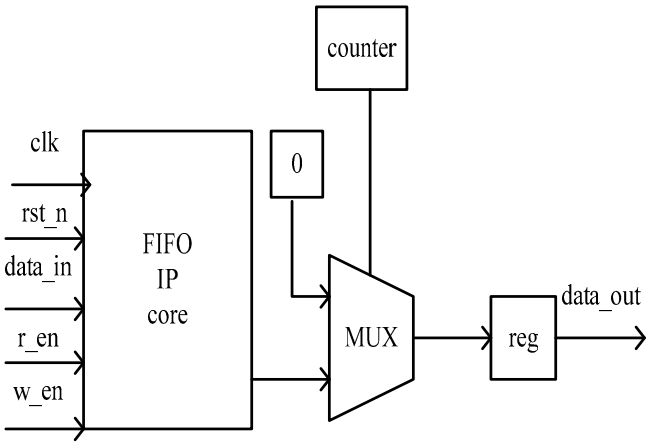

Figure 6. Design of down- and up-sampling using FIFO. Meanings of ports and blocks in this design: clk, clock of this part; rst_n, reset signal; data_in, input of data; r_en and w_en are the reading and writing enable pin, respectively.

A sharp detection block is the key to this filter. A differential unit is employed to detect the positions of sharp transitions in SMI signals. This detection block is simply realized by subtractions between two adjacent points in SMI signals. A pulse train is obtained after this detection, which contains the information of sharp transitions. However, this pulse train has varying magnitude. Thus, a threshold should be pre-set. Considering the difference of the magnitudes between pulses and noises, half of the magnitude of the first pulse is set as a threshold and is stored in a register. The following magnitudes of each differential value should be compared with this threshold. The ones bigger than the threshold are seen as transitions and others are seen as noise. Combining this information with the reconstructed high frequency component, the signals are processed.

3.3 Normalization FPGA based design

After filtering SMI signals, their normalization is no longer affected by the sparkle-like noise. In this situation, the key to normalization is to remove the direct current component. This normalization can be derived from the following equations:

$$g_p[n] = ((g_f[n] - \min(g_f[n])) / (\max(g_f[n]) - \min(g_f[n])) - 0.5) \times 2 \quad (7)$$

In Equation (7), $g_f[n]$ is a filtered SMI signal and $g_p[n]$ represents the normalized signal. $\min(g_f[n])$ and $\max(g_f[n])$ are the minimum and the maximum values of $g_p[n]$, respectively. Maximum and minimum values can be found out using a register. The first come-in value of a segment in $g_f[n]$ is stored as an extreme value, and the next value compares with the stored one. The next point replaces the stored extreme value if it is larger than the maximum value or smaller than the minimum value.

4. CO-SIMULATION OF THE DESIGN

This whole design of pre-processing unit is implemented on a Xilinx ® Spartan-3E FPGA (XC3S500E-4FG320C) Development Board. The main features of this board is listed as following[22]: 10478 logic elements (LEs); 232 maximum user I/O pins; 20 multiplier; 2-input serial peripheral interface (SPI) based Analog-to-Digital Converter (ADC) and 4-output SPI-based Digital-to-Analog Converter (DAC); on-board Universal Serial Bus (USB) based download/debug interface.

The design proposed in Section 3 is completed in System Generator and converted into Verilog HDL code. The Verilog code is synthesized and downloaded into the FPGA board. Then hardware co-simulation is carried out and processed data is exported into Matlab and plotted as in Figure 7. An experimental SMI signal is as shown in Figure 7(a). Figure 7 (b) demonstrates the signal de-noised by a median filter and a wavelet transform based filter. The filtered signal after normalization is illustrated in Figure 7(c). From this diagram, it can be seen that the FPGA based pre-processing works well for SMI signals.

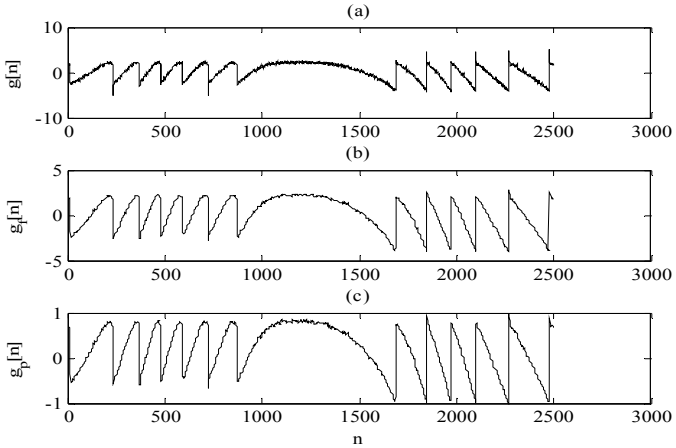

Figure 7. Filtering result for an experimental SMI signal: (a) an original experimental SMI signal; (b) the filtered SMI signal; (c) the normalized SMI signal

5. CONCLUSION

This paper presents a FPGA based pre-processing design for SMI signals. Based on the features of SMI signals, this FPGA based pre-processing includes two parts, a de-noising part and a normalization part. In the de-noising part, a wavelet filter and a median filter are employed. The de-noising part reduces the high-frequency and sparkle-like noise and the normalization part makes SMI signals into the range of [-1, 1]. By implementing this method on a Xilinx Spartan 3E board, hardware co-simulation is carried out to verify the performance of this FPGA based pre-processing method.

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