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Controllable DC-link fault current limiter augmentation with DC chopper to improve fault ride-through of DFIG

Amin Jalilian
University of Tabriz, Jaliliyan-amin90@ms.tabrizu.ac.ir

Seyed Behzad Naderi
University of Tasmania (UTAS)

Michael Negnevitsky
University of Tasmania (UTAS), michael.negnevitsky@utas.edu.au

Mehrdad Tarafdar Hagh
University of Tabriz, mehrdadh@uow.edu.au

Kashem M. Muttaqi
University of Wollongong, kashem@uow.edu.au

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Controllable DC-Link Fault Current Limiter Augmentation with DC Chopper to Improve Fault Ride-Through of DFIG

1*Amin Jalilian, 2Seyed Behzad Naderi, 2Michael Negnevitsky, 1Mehrdad Tarafdar Hagh and 3Kashem M. Muttaqi

1Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666-15813, Iran
2School of Engineering and ICT, University of Tasmania, Hobart, TAS, 7000, Australia
3School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, NSW 2522, Australia
E-mails addresses: Jaliliyan-amin90@ms.tabrizu.ac.ir, Seyedbehzad.Naderi@utas.edu.au, Michael.Negnevitsky@utas.edu.au, Tarafdar@tabrizu.ac.ir, Kashem@uow.edu.au

Abstract—Doubly fed induction generator (DFIG) based wind turbines are sensitive to grid faults due to utilising small-scale rotor side converter (RSC). The application of crowbar protection to improve the fault ride-through (FRT) capability of the DFIG converts it to a squirrel cage induction generator, which makes it difficult to comply with grid codes. This paper proposes an innovative DC-link controllable fault current limiter (C-FCL) based FRT scheme for the RSC to improve the FRT capability of the DFIG. The proposed scheme replaces the AC crowbar protection and eliminates its disadvantages. The C-FCL does not affect the normal operation of the DFIG. By means of the proposed scheme, rotor over-currents are successfully limited during balanced and unbalanced grid faults, even at zero grid voltage. Also, the C-FCL prevents rotor acceleration and high torque oscillations. In this paper, an analysis of the proposed approach is presented in detail. The performance of the proposed scheme is compared with the conventional crowbar protection scheme through simulation studies carried out in power system computer-aided design/electromagnetic transients, including dc software (PSCAD/EMTDC). Moreover, the main concept of the proposed approach is validated with an experimental setup and test results are presented.

Keywords—Doubly fed induction generator, fault ride-through, DC-link, fault current limiter.

*Corresponding Author. Tel.: +98 918 930 1405.
I. INTRODUCTION

By increasing the penetration level of wind power in the grid in recent years, grid operators are experiencing new challenges ensuring secure and reliable operation of the utility. One of these challenges is that wind turbines, similar to conventional power plants, must be able to stay connected to the grid during fault. This operational behaviour is known as fault ride-through (FRT) capability [1].

Nowadays, doubly-fed induction generator (DFIG) based wind turbines are widely used because of many salient features, mainly for applications more than 1 MW [1, 2]. The stator of the DFIG is directly connected to the utility and the rotor circuit via partial scale back-to-back voltage source converters (VSCs) connected to the network. In the case of grid faults, transient over-currents flow from the rotor circuit towards the rotor side converter (RSC). These over-currents can either trip out the DFIG or damage its power electronic components [3, 4]. Therefore, keeping the DFIG based wind turbine connected with the utility and preventing the equipment from damage are great challenges during the fault conditions. Of all the different grid codes, which are regulated by the various operators, the “E.ON” grid code has the most severe FRT requirements [1, 5]. With regard to “E.ON”, when the point of the common coupling (PCC) voltage drops to zero for 0.15 seconds after the fault occurrence, the wind turbine must not be disconnected from the grid.

Several approaches have been introduced in the literature to improve the FRT capability of the DFIG [6]. These methods can be basically categorised as crowbar protection [7-9], DC choppers [10, 11], new configurations for the DFIG [12-15] and the application of advanced control strategies [16-21].

The most common method to improve the FRT capability of the DFIG is to employ crowbar protection and protect the back-to-back converters during the fault [7, 8]. This method changes the DFIG to a squirrel cage induction generator. In this situation, due to absorption of the reactive power from the grid, the DFIG does not comply with the grid requirements [5, 9].

To eliminate crowbar protection problems in the DFIG based wind turbine, a DC chopper has been proposed in [10, 11] as an efficient device to enhance the FRT capability of the DFIG. However, in the proposed approach in [10], to prevent damages in the semi-conductor switches of the RSC, the PWM
switching signals of the RSC are blocked during the grid fault and the rotor over-currents pass through anti-parallel diodes of the RSC. In this situation, the high rated anti-parallel diodes of the RSC must be able to withstand the rotor fault current to 5 \( (p.u.) \) [10].

Recent works, [12-15], present the FRT schemes by using the new configurations for the DFIG. In [12] and [13], nine switch grid side converter has been proposed to overcome the fault situation in the power system. Meanwhile, in [14] and [15], a series grid side converter connected to a star point terminal of the stator, including parallel grid side rectifier and three winding transformer has been utilised to make an adequate power processing capability to ride though the low voltage. These approaches make fundamental changes in the conventional DFIG configuration. Therefore, it may not be straightforward for industry to implement their control strategies, without special engineering measures. Consequently, provision of a practical economic justification may be impossible.

Several studies [16-21] have discussed the advanced control strategies as FRT solutions for the DFIG. Nevertheless, in practice, DFIG manufacturing companies find it difficult to apply most of these approaches due to their complexity [18]. Moreover, the DFIG cannot solely ride through the network faults with control of the converters, during deep voltage sags [7].

Most of the proposed FRT approaches in the literature, [3], [19] and [21], only deal with the FRT performance of the DFIG during balanced faults, whereas unbalanced faults are the majority of the faults in the power system. The DFIG is very vulnerable to unbalanced fault conditions [4, 16, 22].

Well-known in the power systems [23-25], the application of a fault current limiter (FCL), to reduce the fault current level, could be a good solution for the FRT improvement of the DFIG-based wind turbines [26-30]. A three phase FCL, including an isolation transformer and a large DC inductance with a bypass resistance located in the stator side of the DFIG, is used to restrict the fault current level [26, 27]. A single phase bridge type FCL is utilised in the terminal of the DFIG to improve the LVRT capability of the DFIG during all grid faults [28, 29]. Super-conducting FCL is also effective in limiting the fault current in the DFIG [30]. All the above-mentioned configurations are either three phase FCLs or three sets of the single
phase FCL in the grid side. A large number of components with a high voltage rating and a high cost of the superconductor are disadvantages of the previous FCLs in the FRT improvement of the DFIG based wind turbines.

This paper proposes an innovative FRT scheme with minimum additional components to improve the FRT capability of the DFIG during balanced and unbalanced grid faults. An alternative solution is proposed, replacing the conventional crowbar protection method to limit the rotor transient over-currents during various faults in the grid with a DC-link controllable-FCL (C-FCL). In this way, continuous operation of the DFIG can be ensured even at zero grid voltage. Also, the C-FCL is simple in configuration and less expensive due to the use of non-super-conducting inductance in its structure.

II. PROPOSED FRT SCHEME

Fig. 1(a) shows a schematic diagram of the proposed FRT configuration to provide continuous operation of the DFIG during the faults in the power system. The instantaneous value of DC-link current \(i_{dc}\) depends on the switching states of the RSC during normal operation. To improve the FRT capability of the DFIG during the various faults, application of the C-FCL is proposed. In the proposed approach, the C-FCL is placed in series with the RSC (between the RSC and DC-link capacitor), as shown in Fig. 1(a). It should be noted that, in Fig. 1(a), it is necessary to use a diode bridge in the DC-link; otherwise, the ripples of \(i_{dc}\) could generate a voltage drop, which can affect the performance of the DFIG in normal operation. The C-FCL is composed of four main parts:

1) a diode rectifier bridge, including diodes of \(D_1\) to \(D_4\);
2) a coil (copper coil) that is modelled by a resistor \(r_{ld}\) and an inductance \(L_{ld}\);
3) a parallel connection of a fully controllable semi-conductor switch \(S_{C-FCL}\) such as IGBT, IGCT with a discharging resistor \(r_{p}\), which are connected in series with the DC inductance, and
4) a DC voltage source \(V_c\) that is connected in series with the DC inductance for compensation of voltage drops caused by \(r_{ld}\) and semiconductor devices.

Because of employing the C-FCL, the rotor transient over-currents are effectively limited at the fault
incident and its clearing time. Meanwhile, $L_d$ can effectively suppress high $di/dt$ in the first moments of the fault occurrence and also successfully limit the rotor over-current during the fault. In this way, continuous operation of the DFIG can be achieved even at zero grid voltage. Furthermore, an over-voltage appears across the FCLs due to $Ldi/dt$, which especially happens at the beginning of the fault [31]. In order to suppress the over-shoots and avoid any component damage, a zinc oxide (ZnO) surge arrester device is usually employed in the FCLs [26]. So, to protect the semiconductors against over-voltage, it is necessary to include a ZnO device in parallel with the proposed C-FCL.

More details about modelling the DFIG can be found in [32, 33]. Both converters of the DFIG, the RSC and the grid side converter (GSC) operate by direct torque control (DTC) strategy [32]. The DFIG system could have a DC-chopper installed at the DC-link [34]. During the fault, the DC chopper protects the DC-link from over-voltage by consuming the excess energy of the DC-link capacitor with its braking resistance ($R_{brake}$). Furthermore, during normal operation, the DC chopper enhances overall system performance, especially, when there is an imbalance of power between the RSC and the GSC [32, 34]. With the proposed C-FCL, the restricted rotor fault current reduces the charging current to the DC-link capacitor [35].

### A. Operation of the C-FCL in normal conditions

In the normal operation of the power system, the $S_{C-FCL}$ is ON and bypasses $r_p$. Utilising $V_c$ compensates for the voltage drops on the diodes, the $S_{C-FCL}$, and the inherent resistance of the DC inductance. Considering Fig. 1(a), the value of $V_c$ should be selected in a way that the DC inductance current ($i_d$) is adjusted to higher than the maximum possible peak of $i_{dc}$ during normal operation. Consequently, the diode rectifier bridge remains fully conducting and $i_d$ freewheels through the diodes of $D_1$ to $D_4$ and $D_2$ and $D_3$. In this situation, the DC inductance does not have any impact on the normal operation of the DFIG.

As is mentioned, by utilising $V_c$, the C-FCL is bypassed during normal operation and all diodes of the bridge rectifier are ON. Considering kirchhoff’s voltage law (KVL) in the bridge rectifier of the C-FCL, as shown in Fig. 1(a), we have:

$$L_d \frac{di_d}{dt} + i_d (2r_{on} + r_a) = V_c - 2V_{df} - V_{sf}$$

(1)
whereby the C-FCL’s diodes are modelled by a series connection of their voltage drop ($V_{df}$) and resistance ($r_{on}$) during the ON state. Meanwhile, the $S_{C-FCL}$ is represented by its resistance ($r_{on}$) and voltage drop ($V_{sf}$) in the ON state. When the DC inductance current is biased, the minimum value for the $V_c$ can be achieved, considering (1) as follows:

$$V_c \geq 2V_{df} + V_{sf} + i_d(2r_{on} + r_d)$$

The resistance value of the diodes and $S_{C-FCL}$, $r_{on}$ is very low. Therefore, the voltage drop caused by $r_{on}$ can be ignored. Consequently, the following expression can be concluded:

$$V_c \geq 2V_{df} + V_{sf} + i_d r_d$$

As is clear, by changing the power system parameters, the third part of (3) ($r_d i_d$) will be changed. To be sure that the $V_c$ will bypass the C-FCL during normal operation for all load variations, the maximum load current should be considered to compute $V_c$. In the paper, to provide $V_c$, an external DC source is utilised. However, the external DC source to obtain $V_c$ can be provided from the power lines, using an isolation transformer and three phase diode bridge rectifier [25]. Alternatively, a DC-DC converter can be employed to control the output dc voltage level during all load conditions [36, 37].

**B. Operation of the C-FCL in the fault condition**

During the fault condition, the fault current tends to increase intensively. At the first moment of the fault, the high $di/dt$ is limited by $L_d$. However, for lengthy periods of the fault, $L_d$ will be charged and will not solely be able to restrict the fault current level. In this situation, whenever the fault current reaches a pre-defined current value ($I_c$ as a maximum permissible fault current level), the control system turns off the $S_{C-FCL}$, which inserts $r_p$ into the fault current path and discharges $L_d$. Therefore, $i_d$ decreases. After that, the control system turns on the $S_{C-FCL}$ and $r_p$ retreats from the fault path. Obviously, by turning on the $S_{C-FCL}$, $i_d$ will start to increase. Turning on and off of the $S_{C-FCL}$ continues until the removal of the fault.

By selecting an appropriate value for $r_p$, it is possible to maintain $i_d$ below $I_c$. It should be mentioned that $r_p$ provides a route to evacuate excess energy due to the imbalance between mechanical and electrical powers during the fault. In this way, the C-FCL prevents the DFIG’s rotor acceleration. Moreover, $r_p$ significantly
mitigates severe electrical torque oscillations by consuming active power in a controlled manner. In this way, the C-FCL increases the lifetime of both the turbine shaft and the gear box.

Considering the switching states of the RSC, two operation modes are discussed for the C-FCL during the fault, as follows:

**Mode I) when \( i_d \) is higher than \( i_{dc} \) and the \( S_{C-FCL} \) is ON (Fig. 1(b)):** In this situation, \( i_{dc} \) is lower than \( i_d \) of the C-FCL. This situation is the discharging mode during the fault. Considering Fig. 1(b), all diodes of the diode rectifier bridge are ON. As a result, \( L_d \) will be discharged by \( r_d \) and the voltage drops on the diodes of the bridge rectifier and the \( S_{C-FCL} \). Therefore, \( i_d \) decreases until it reaches \( i_{dc} \).

**Mode II) when \( i_d \) is equal to \( i_{dc} \):** In this state, only diodes of \( D_2 \) and \( D_4 \) are ON in the bridge rectifier. Charging and discharging conditions of \( L_d \) depend on the switching state of the \( S_{C-FCL} \), which are described as follows:

**Mode II-A) In this situation, the \( S_{C-FCL} \) is ON.** So considering Fig. 1(c), \( i_{dc} \) charges \( L_d \).

**Mode II-B) Whenever \( i_d \) reaches \( I_c \), the control system operates and turns off the \( S_{C-FCL} \).** So, \( r_p \) enters in series with \( L_d \) (Fig. 1(d)). Consequently, \( L_d \) will be discharged and \( i_{dc} \) is limited during the fault. This condition continues until the \( S_{C-FCL} \) is switched to the ON state.

### III. CONTROL SYSTEM OF THE C-FCL

Fig. 2(a) shows the control system of the C-FCL. To turn on and turn off the \( S_{C-FCL} \), \( i_d \) is utilised as a control signal. In this way, by turning on and turning off of the \( S_{C-FCL} \), it is possible to maintain \( i_d \) below \( I_c \), in which the current of the semi-conductor devices of the RSC (shown in Fig. 2(b)) is restrained to its maximum permissible current.

When \( i_d \) reaches the pre-defined current level, \( I_c \), the control system senses the fault situation and turns off the \( S_{C-FCL} \). As a result, the special value of \( r_p \) enters in series with \( L_d \) and discharges its absorbed energy. Therefore, \( i_d \) decreases. The control system realises that the fault current level is lower than \( I_c \), so it turns on the \( S_{C-FCL} \). The turning on and off of the \( S_{C-FCL} \) by the control circuit continues up to the end of the fault. The flowchart for the operation of the proposed FRT scheme is presented in Fig. 3.
The value of $r_p$ should be selected in a way that the fault current is limited to $I_c$ during the fault condition. The calculation procedure of $r_p$ with regard to $I_c$ is obtained in section V-C.

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**Fig. 1.** (a) The proposed FRT configuration of the DFIG-based wind turbine. The C-FCL’s equivalent circuits during the fault condition. (b): Mode I (discharging state), (c): Mode II-A (charging state), (d): Mode II-B (discharging state).
Fig. 2. (a): The control system of the C-FCL. (b): Schematic diagram of the DFIG with regard to the analysis.

Fig. 3. The flowchart for the operation of the proposed FRT scheme. (a): the proposed C-FCL. (b): the DC link chopper.
IV. ANALYSIS OF THE PROPOSED FRT SCHEME

A. System Description

In the fault condition, the high rotor over-currents flow toward the RSC. In this condition, the switching pulses of the RSC are continuously applied to the semi-conductor devices. Therefore, these over-currents pass through the semi-conductor devices of the RSC, as well as through the DC-link. In the proposed approach, the C-FCL is connected to the RSC and the DC-link capacitor, so that the rotor over-currents have to pass through it. In this way, the C-FCL limits the rotor over-currents to the maximum permissible currents of the semi-conductor devices.

During the fault, the additional energy, which cannot be transferred to the grid by the GSC, flows into the DC-link capacitor and rapidly charges it. Therefore, the DC-chopper is triggered to restrain the DC-link voltage \( V_{DC} \) to an acceptable range. In this situation, the system response is highly non-linear due to the operation of the DC-chopper and time varying behaviour of the induced rotor voltages. However, the \( V_{DC} \) is almost fixed during the fault by the DC-chopper operation. So, in the analysis performed in this study, similar to the research conducted in [38], the DC-chopper and the DC-link capacitor are considered as a constant DC voltage source.

Considering the Park model of the DFIG, the rotor and stator voltages, \( \vec{v}_r, \vec{v}_s \), and fluxes, \( \vec{\psi}_r, \vec{\psi}_s \), are expressed as follows (in a static stator-oriented reference frame) [3]:

\[
\vec{v}_s = R_s \vec{i}_s + \frac{d\vec{\psi}_s}{dt} \tag{4}
\]

\[
\vec{v}_r = R_r \vec{i}_r + \frac{d\vec{\psi}_r}{dt} - j\omega_r \vec{\psi}_r \tag{5}
\]

\[
\vec{\psi}_s = L_s \vec{i}_s + L_m \vec{i}_r \tag{6}
\]

\[
\vec{\psi}_r = L_m \vec{i}_s + L_r \vec{i}_r \tag{7}
\]

whereby \( R, L, \vec{i} \) and \( \omega \) denote resistance, inductance, current and angular frequency, respectively. Also, subscripts of \( m, s, \) and \( r \) represent mutual, stator and rotor parameters, respectively. To calculate \( \vec{\psi}_r \) in terms of \( \vec{i}_r \) and \( \vec{\psi}_s \), (6) and (7) are used. As a result, we have:
\[ \bar{\psi}_r = \frac{L_m}{L_s} \bar{\psi}_s + \sigma L_r \tilde{i}_r \]  

(8)

whereby \( \sigma \) is the leakage coefficient, which is equal to \( 1 - L_m^2 / L_s L_r \). Considering (5) and (8), it is concluded that:

\[ \tilde{v}_r = \frac{L_m}{L_s} \left( \frac{d}{dt} - j \omega_r \right) \bar{\psi}_s + \left( R_r + \sigma L_r \frac{d}{dt} - j \omega_r \right) \tilde{i}_r \]  

(9)

whereby \( \tilde{v}_{ro} \) is the rotor voltage during an open circuit condition in which the rotor current, \( \tilde{i}_r \), is zero. In a rotor reference frame, (9) can be expressed as follows:

\[ \tilde{v}^r_r = \tilde{v}^r_{ro} + \left( R_r + \sigma L_r \frac{d}{dt} \right) \tilde{i}^r_r \]  

(10)

whereby \( \tilde{v}^r_r \), \( \tilde{v}^r_{ro} \) and \( \tilde{i}^r_r \) are the rotor voltage, the open circuit rotor voltage and the rotor current all in the rotor reference frame. Considering (10), the rotor circuit during the grid fault is represented by the three-phase AC voltage source of \( \tilde{v}^r_{ro} \) (\( V_{ro,a} \), \( V_{ro,b} \) and \( V_{ro,c} \) in time domain), the transient inductance (\( \sigma L_r \)) and the rotor resistance (\( R_r \)), as shown in Fig. 2(b). According to the fault type, the depth of the voltage sag and the fault inception instant, the maximum rotor over-current will change [3, 4]. In this paper, the analysis regarding the three phase fault is discussed. In the three phase fault, \( \tilde{v}^r_{ro} \) is composed of two parts, as mentioned below [4]:

\[ \tilde{v}^r_{ro} = (1 - p)V_s \frac{L_m}{L_s} s e^{j s \omega_s t} - \frac{L_m}{L_s} \left( \frac{1}{\tau_s} + j \omega_r \right) \frac{p V_s}{j \omega_s} e^{-j \omega_r t} e^{-t/\tau_s} \]  

(11)

whereby \( p \), \( V_s \), and \( s \) are the depth of voltage sag during the three phase fault, the stator or terminal constant voltage of the DIFG before the fault and the slip, respectively. Meanwhile, the first part frequency and second part frequency are \( s \omega_s \) and \( \omega_r \), respectively, with a decaying time constant of \( \tau_s=L_s/R_s \).

The DC link current can be expressed in the basis of AC side currents and switching states as follows [39]:

\[ i_{dc}(t) = S_{ra} i_{r,a}(t) + S_{rb} i_{r,b}(t) + S_{rc} i_{r,c}(t) \]  

(12)

whereby \( S_{ra} \), \( S_{rb} \), and \( S_{rc} \) are switching states of the RSC in phases \( a \), \( b \), and \( c \), respectively. Also, the three phase rotor currents, in phases \( a \), \( b \), and \( c \), are denoted by \( i_{r,a}(t) \), \( i_{r,b}(t) \) and \( i_{r,c}(t) \), respectively. In carrier
based sinusoidal pulse width modulation (SPWM) converters, carrier frequency is very high compared with output frequency. So, in this section, the performance of the proposed scheme is explained during one carrier period. The analysis of the DFIG system is performed as follows:

**B. Analytical Approach for the DFIG System including the C-FCL**

In this section, for a better understanding of the performance of the proposed FRT scheme, the charging and discharging operating conditions of $i_d$ are analysed. In this analysis, each semi-conductor device of the RSC and the diodes of the C-FCL are modelled by a series connection of their voltage drop ($V_{df}$) and resistance ($r_{on}$) in the ON state. Meanwhile, the $S_{C-FCL}$ is represented by its voltage drop ($V_{sf}$) and resistance ($r_{on}$). Fig. 4(a) shows $i_{dc}$, $i_d$ and switching sequences of the RSC during normal and fault conditions in one switching period ($T_s$), after the three phase fault occurrence at $t=t_0$. The analytical procedures are carried out based on section II.

**B.1. Operation of the DFIG system including the C-FCL in normal condition**

During normal operation, as mentioned in section II, $i_d$ is charged to higher than the peak of $i_{dc}$ due to $V_c$, and all diodes of the bridge rectifier and the $S_{C-FCL}$ in the C-FCL are in the ON state. Therefore, before the fault occurrence at $t=t_0$, $L_d$ is in discharging mode and $i_d$ freewheels through $D_1-D_3$ and $D_2-D_4$. The differential equation of $i_d$ can be expressed as follows:

$$L_{e1} \frac{di_d}{dt} + R_{e1} i_a = V_{e1}$$  \hspace{1cm} (13)

whereby $r_{e1}=r_d+2r_{on}$, $L_{e1}=L_d$, $V_{e1}=V_c-V_{sf}-2V_{df}$. Solving (13) leads to (14).

$$i_d(t) = e^{-(t-t_0)/\tau_1} \left[ i_1 - \frac{V_{e1}}{r_{e1}} \right] + \frac{V_{e1}}{r_{e1}}$$  \hspace{1cm} (14)

whereby $i_1=i_d(t_0)$ and $\tau_1=L_{e1}/r_{e1}$.

**B.2. Operation of the DFIG system including the C-FCL in the fault condition**

At $t=t_0$, the three-phase fault occurs in the terminal of the DFIG. As discussed in section II, there are two modes of operation during the fault, as follows:

**Mode-I) when $i_d$ is higher than $i_{dc}$ and the $S_{C-FCL}$ is ON:**
Considering Fig. 4(a), from \( t_0 \) to \( t_1 \), the switching state is 000. In this condition, \( L_d \) is in the discharging state. Therefore, \( i_d \) expression is as (14). At \( t = t_1 \), the switching state changes to 100. As is clear from Fig. 4(a), \( i_{dc} \) increases until it reaches \( i_d \) at \( t = t_2 \). So, from \( t_1 \) to \( t_2 \), because \( i_d \) is higher than \( i_{dc} \), \( i_d \) expression is similar to (14). At \( t = t_2 \), \( i_{dc} \) reaches \( i_d \) and the next mode of operation starts.

**Mode II-A): when \( i_d \) is equal to \( i_{dc} \) and the Sc-FCL is ON**

At \( t = t_2 \), the charging state of \( L_d \) begins. Fig. 4(b) shows the equivalent circuit in this condition. As the equivalent circuit reveals, \( i_d \) is equal to \( i_{dc} \) and only diodes of \( D_2 \) and \( D_4 \) are ON. The differential equation of \( i_d \) can be expressed as (15).

\[
L_{e2} \frac{di_d}{dt} + R_{e2} i_d = V_{e2} + V_{e,AC}
\]

whereby \( L_{e2} = \frac{3}{2} \sigma L_r + L_d, \quad R_{e2} = \frac{3}{2} R_r + r_d + \frac{9}{2} r_{on}, \quad V_{e2} = V_{DC} + V_c - V_{sf} - 4V_{df}, \) and \( V_{e,AC} = -\frac{3}{2} \text{Re}\{\bar{v}_{r,o,a}\} \).

With regard to (11), \( \text{Re}\{\bar{v}_{r,o,a}\} \) can be written as (16) [35].

\[
\text{Re}\{\bar{v}_{r,o,a}\} = (1 - p)V_s \frac{L_m}{L_s} s [\cos s \omega_s t] - p \frac{L_m}{L_s} V_s (1 - s) [\cos \omega_r t] e^{-t/\tau_s}
\]

Equation (17) is derived by using (15), that is the expression of \( i_d \) in the charging mode:

\[
i_d(t) = -\frac{3}{2} (1 - p)V_s \frac{L_m}{L_s} s \frac{1}{\sqrt{R_{e2}^2 + L_{e2}^2 s^2 \omega_r^2}} \cos(s \omega_s (t - t_2) + \theta_{s \omega_s}) + \\
\frac{3}{2} p V_s \frac{L_m}{L_s} (1 - s) \frac{1}{\sqrt{R_{e2}^2 + L_{e2}^2 \omega_r^2}} \cos(\omega_r (t - t_2) + \theta_{\omega_r}) e^{-\frac{1}{\tau_s}(t-t_2)} + \\
\frac{V_{e2}}{R_{e2}} + \\
\left[ I_0 - \frac{V_{e2}}{R_{e2}} + \frac{3}{2} (1 - p)V_s \frac{L_m}{L_s} s \frac{1}{\sqrt{R_{e2}^2 + L_{e2}^2 s^2 \omega_r^2}} \cos(\theta_{s \omega_s}) - \frac{3}{2} p V_s \frac{L_m}{L_s} (1 - s) \frac{1}{\sqrt{R_{e2}^2 + L_{e2}^2 \omega_r^2}} \cos(\theta_{\omega_r}) \right] e^{-\frac{R_{e2}}{L_{e2}}(t-t_2)}
\]

whereby \( I_0 = i_d(t_2), \ \theta_{s \omega_s} = \text{Arctan}(L_{e2} s \omega_s / R_{e2}), \) and \( \theta_{\omega_r} = \text{Arctan}(L_{e2} \omega_r / R_{e2}) \). At \( t = t_3 \), \( i_d \) reaches \( I_c \). So, the next mode of operation commences during the fault.
Mode II-B: when $i_d$ is equal to $i_{dc}$ and the SC-FCL is OFF: Considering Fig. 4(a), at $t=t_3$, $i_{dc}$ reaches $I_c$. Therefore, the control system turns off the SC-FCL. $r_p$ enters in series with the DC-link and discharges $L_d$, which decreases its current (time interval of $t_3$ till $t_4$). Fig. 4(c) shows the equivalent circuit after SC-FCL operation. The differential expression of $i_d$ is as follows:

$$L_{e3} \frac{di_d}{dt} + R_{e3}i_d = V_{e3} + V_{e,AC}$$  \hspace{1cm} (18)

whereby $L_{e3} = L_{e2}$, $R_{e3} = \frac{3}{2}R_r + r_d + r_p + \frac{7}{2}r_{on}$, and $V_{e3} = V_{DC} + V_c - 4V_{df}$. In the time interval of $t_3$ till $t_4$, $i_d$ expression is the same as (17). However, instead of $R_{e2}$, $V_{e2}$, and $I_0$, their new values, $R_{e3}$, $V_{e3}$, and $i_d(t_3)$, should be substituted during $t_3$ till $t_4$, respectively. Mode II-B continues up until the control system turns on the SC-FCL at $t=t_4$. Therefore, regarding Fig. 4(a), another charging mode, the same as Mode II-A, will commence. To ensure a clear explanation, Table I is presented, showing the different modes of operation of the C-FCL with regard to Fig. 4(a).

<table>
<thead>
<tr>
<th>Time frame (according to Fig. 4(a))</th>
<th>Switching state in the RSC</th>
<th>Operation states of the C-FCL</th>
<th>State of the SC-FCL</th>
<th>The diodes in the C-FCL, which are ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_0$ till $t_1$</td>
<td>000</td>
<td>Mode I</td>
<td>ON</td>
<td>All diodes</td>
</tr>
<tr>
<td>$t_1$ till $t_2$</td>
<td>100</td>
<td>Mode I</td>
<td>ON</td>
<td>All diodes</td>
</tr>
<tr>
<td>$t_2$ till $t_3$</td>
<td>100</td>
<td>Mode II-A</td>
<td>ON</td>
<td>$D_2$ and $D_4$</td>
</tr>
<tr>
<td>$t_3$ till $t_4$</td>
<td>100</td>
<td>Mode II-B</td>
<td>OFF</td>
<td>$D_2$ and $D_4$</td>
</tr>
<tr>
<td>$t_4$ till $t_5$</td>
<td>100</td>
<td>Mode II-A</td>
<td>ON</td>
<td>$D_2$ and $D_4$</td>
</tr>
<tr>
<td>$t_5$ till $t_6$</td>
<td>100</td>
<td>Mode II-B</td>
<td>OFF</td>
<td>$D_2$ and $D_4$</td>
</tr>
<tr>
<td>$t_6$ till $t_7$</td>
<td>100</td>
<td>Mode II-A</td>
<td>ON</td>
<td>$D_2$ and $D_4$</td>
</tr>
<tr>
<td>$t_7$ till $t_8$</td>
<td>101</td>
<td>Mode I</td>
<td>ON</td>
<td>All diodes</td>
</tr>
<tr>
<td>$t_8$ till $t_9$</td>
<td>101</td>
<td>Mode II-A</td>
<td>ON</td>
<td>$D_2$ and $D_4$</td>
</tr>
</tbody>
</table>
V. DESIGN CONSIDERATIONS

A. Power loss calculation of the C-FCL

During normal operation, as discussed in section II, $V_c$ is utilised to compensate for the voltage drop on the diodes, the $S_{C-FCL}$ and $r_d$ in the C-FCL. Due to employing $V_c$, $L_d$ is in discharging mode. So, the total
power losses of the C-FCL ($P_{\text{Total-loss}}$) include the power losses on all diodes of the single rectifier bridge ($P_{\text{Bridge}}$), $L_d$ ($P_{Ld}$), and the $S_C$-FCL ($P_s$). The $P_{\text{Total-loss}}$ can be calculated as follows:

$$
\begin{align*}
P_{Ld} &= r_d i_d^2 \\
P_{\text{Bridge}} &= V_{df} i_{D1} + V_{df} i_{D2} + V_{df} i_{D3} + V_{df} i_{D4} = 2V_{df} i_{D1} + 2V_{df} i_{D2} = 2V_{df} i_d \\
P_s &= V_{sf} i_d \\
P_{\text{Total-loss}} &= P_{Ld} + P_{\text{Bridge}} + P_{Ld} = \left[r_d i_d + (2V_{df} + V_{sf})\right]i_d = V_c i_d
\end{align*}
$$

whereby average currents of $D_1$ ($\bar{i}_{D1} = \bar{i}_{D3}$) and $D_2$ ($\bar{i}_{D2} = \bar{i}_{D4}$), are equal to $(i_d + \bar{i}_{dc})/2$ and $(i_d - \bar{i}_{dc})/2$, respectively ($\bar{i}_{dc}$ is average of $i_{dc}$).

For the DFIG, which is simulated in the paper with the total rated capacity of 2 MW ($P_{\text{DFIG}}$), $i_d$=1016 A, $r_d$=0.01 Ω, and $V_s$=$V_{df}$=3 V, the $P_{\text{Total-loss}}$ is 19450 W. The ratio of $P_{\text{Total-loss}}$ to $P_{\text{DFIG}}$ is defined by $K$ and can be derived as follows:

$$
K = \frac{P_{\text{Total-loss}}}{P_{\text{DFIG}}} = \frac{19450 \text{ W}}{2 \text{ MW}} = 0.009
$$

Equation (20) shows that, in the presence of the C-FCL, the total power dissipation is a small percentage of the overall rated power of the DFIG, and it can be ignored for most of the practical applications in order to provide a reliable protection system.

**B. Calculation of the DC inductance ($L_d$)**

$L_d$ is employed to restrict the high $di/dt$ in the first moments of the fault. This characteristic guarantees a safe area of operation for the semi-conductor devices in the C-FCL and the RSC. The value of $L_d$ should be calculated regarding the maximum rate of current change in the semi-conductor devices ($di_{\text{max}}/dt$). The charging state of $L_d$ in the first moments of the fault is expressed in (15) for a three phase fault. In the worst condition ($p=1$ and $s=-0.2$) [26], the differential expression of $i_d$ is as follows:

$$
L_e \frac{di_d}{dt} + R_e i_d = V_{e2} + 1.8 \frac{L_m}{L_s} V_s [\cos \omega_r t] e^{-t/\tau_s}
$$

As a result, the minimum value of $L_d$ can be written as (22).

$$
L_d > \frac{V_{e2} + 1.8 \frac{L_m}{L_s} V_s - R_e i_0}{di_{\text{max}}/dt} = \frac{3}{2} \sigma L_r
$$
C. Calculation of the Discharging resistor of the C-FCL ($r_p$)

As discussed, after the control system operation, the $S_{C-FCL}$ goes to the OFF state. Consequently, the C-FCL inserts $r_p$ to the fault current pass. The value of $r_p$ should be selected considering the value of $I_c$. In fact, $r_p$ should be able to evacuate $L_{d1}$ as much as possible to keep the fault current around $I_c$. To compute $r_p$, (18) is used. In the worst condition ($p=1$ and $s=-0.2$) [26], the rate of the current change is equal to (23).

$$\frac{di_d}{dt} = \frac{V_{e3} + 1.8 \frac{L_m}{L_s} V_s \cos \omega r t e^{-t/r_s} - R e3 i_d}{L_e3}$$

(23)

Considering Fig. 4(a), by inserting $r_p$, the change rate of $i_d$ is negative, which means that $r_p$ is able to discharge $L_{d1}$ when its current is $I_c$. So, by using (23), the value of $r_p$ can be achieved as (24).

$$r_p = \frac{V_{e3} + 1.8 \frac{L_m}{L_s} V_s}{I_c} - \frac{3}{2} R_r - r_d - \frac{7}{2} r_m$$

(24)

D. Comparison of the proposed C-FCL with other corresponding schemes

In this section, the proposed C-FCL is compared with other corresponding FCLs, crowbar protection and the DC chopper. All methods are effective in controlling the DC link voltage. As is clear from Table II, the C-FCL has a lower number of components than the previously employed FCLs in the FRT capability improvement of the DFIG based wind turbines. Due to the benefits of the low number of components, using non-superconductor and simple control circuit, the configuration of the C-FCL can be easily implemented by the industry.

<table>
<thead>
<tr>
<th>The FRT strategy</th>
<th>The rotor current</th>
<th>The RSC status</th>
<th>Effective for fault type</th>
<th>Semiconductor devices and passive elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>The C-FCL</td>
<td>Limited to &lt;2</td>
<td>Operation</td>
<td>Effective</td>
<td>Balanced Unbalanced No. of semiconductor switches No. of diodes No. of inductance No. of resistance No. of transformer No. of capacitor</td>
</tr>
<tr>
<td>Crowbar [7-9]</td>
<td>Limited to &lt;2</td>
<td>Blocked</td>
<td>Effective</td>
<td>1 4 1 1 _ _ _</td>
</tr>
<tr>
<td>The DC Chopper [10, 11]</td>
<td>No change</td>
<td>Blocked with over-rated anti-parallel diodes of RSC</td>
<td>Effective</td>
<td>1 1 _ 1 _ _ _</td>
</tr>
<tr>
<td>The BTPFL [26, 27]</td>
<td>Limited to &lt;2</td>
<td>Operation</td>
<td>Effective</td>
<td>1 7 3 used at the stator side of the machine _ 3 2 with large capacity to absorb the excessive energy of the stator</td>
</tr>
<tr>
<td>Three phase FCL [28]</td>
<td>Limited to &lt;2</td>
<td>Operation</td>
<td>Effective</td>
<td>3 12 6 6 _ _ _</td>
</tr>
<tr>
<td>The DC Resistive fault current limiter [29]</td>
<td>Limited to &lt;2</td>
<td>Operation</td>
<td>Effective</td>
<td>_ 12 3-Superconductor _ _ _</td>
</tr>
</tbody>
</table>
VI. SIMULATION RESULTS

A single line diagram of the test system is shown in Fig. 5(a). The DFIG system is connected to the grid via parallel transmission lines, which are equipped with circuit breakers (CBs), as shown in Fig. 5(a). Each line has two circuit breakers with both slow and fast operation times and a dead time of 0.5 seconds. The simulation has been undertaken based on “E.ON” grid code. Therefore, for the fault duration of 0.15 seconds, the wind turbine should stay connected to the power system. The faults are applied on line 1, close to CB1. After first operation of the circuit breakers (CB1 and CB2 simultaneously open), line 1 is disconnected at 4.15 s. Since all types of the fault are considered the transient ones, therefore, before first reclosing time of CB1 and CB2 at 4.65 s, the faults are removed from line 1. So, the DFIG is subjected to the grid disturbances for only 0.15 seconds based on “E.ON” grid code. The grid is represented by a three phase AC voltage source with an equivalent impedance of $Z_g$. The complete model of the DFIG, including mechanical and electrical parts, has been simulated in PSCAD/EMTDC software. The DFIG system specifications and C-FCL parameters can be found in Table III. Also, the grid data are given in Fig. 5(a). To demonstrate the effectiveness of the proposed FRT scheme, its performance is compared with conventional crowbar protection. The threshold for activation of crowbar protection and the DC chopper is set to 1.1 p.u. With crowbar protection, whenever the DC-link voltage exceeds the threshold voltage value, the switching pulses of the RSC are blocked. The different fault scenarios, including a balanced three phase to ground fault (LLLG), unbalanced two phase to ground fault (LLG) and unbalanced single phase to ground fault (LG), are simulated for the different wind speeds and various fault inception instants. Fig. 5(b) and 5(c) show the terminal voltage of the DFIG during the LLLG and the LLG faults, respectively. As is clear, based on “E.ON” grid code, the PCC voltage drops to zero for 0.15 seconds. The next sections present the corresponding results and key variables of the DFIG response during the LLLG, the LLG and the LG faults.
Fig. 5. (a) Single line diagram of the test system used for simulation, terminal voltage of the DFIG based wind turbine during (b) the LLLG fault, (c) and the LLG fault.

Table III: Simulated DFIG System Specifications

<table>
<thead>
<tr>
<th>The DFIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power</td>
</tr>
<tr>
<td>Rated Stator Voltage</td>
</tr>
<tr>
<td>Rated Frequency</td>
</tr>
<tr>
<td>Stator leakage inductance</td>
</tr>
<tr>
<td>Rotor leakage inductance</td>
</tr>
<tr>
<td>Magnetising Inductance</td>
</tr>
<tr>
<td>Stator to Rotor turns ratio</td>
</tr>
<tr>
<td>Stator resistance</td>
</tr>
<tr>
<td>Stator inductance</td>
</tr>
<tr>
<td>Generator inertia constant</td>
</tr>
<tr>
<td>Nominal wind speed</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>The DC Chopper</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated DC-link voltage</td>
</tr>
<tr>
<td>DC bus capacitor</td>
</tr>
<tr>
<td>DC link activation threshold voltage</td>
</tr>
<tr>
<td>Nominal wind speed</td>
</tr>
<tr>
<td>DC-chopper resistor</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>The C-FCL</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC inductance ($L_d$)</td>
</tr>
<tr>
<td>Inherent resistance of the DC inductance ($r_d$)</td>
</tr>
<tr>
<td>Voltage drop across the diode bridge and the $S_{C\cdot FCL}$ of the C-FCL ($V_{sf}$ and $V_{df}$)</td>
</tr>
<tr>
<td>Discharging resistor ($r_p$)</td>
</tr>
<tr>
<td>DC Voltage source ($V_c$)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>The crowbar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crowbar resistance</td>
</tr>
</tbody>
</table>
A. Balanced LLLG Fault

With a temporary LLLG fault (usually considered as a worst fault scenario), a voltage dip of 100% at the stator terminal, Fig. 5(b), is applied at point F, close to CB1, as shown in Fig. 5(a), at \( t=4 \) s. Fig. 6(a) and 6(c) show the transient response of the stator currents and the rotor currents of the DFIG with crowbar protection, respectively. It is clear that the current level increases more than 4 p.u. By using the proposed approach, considering Fig. 6(b) and 6(d), not only the stator currents and the rotor currents of the DFIG are restricted to 2 p.u., respectively, but also their transient response is improved during and after the fault. Consequently, a safe area of operation is guaranteed for the semi-conductor devices of the RSC.

With a severe voltage dip at the PCC, the active power cannot transfer to the grid. So, \( V_{DC} \), as well as the rotor speed, increase until the fault is cleared. In this situation, to decrease the \( V_{DC} \), the DC-chopper triggers and regulates \( V_{DC} \) around the nominal value. In Fig. 6(e), the \( V_{DC} \) is shown as both with and without the C-FCL. Furthermore, as is clear in Fig. 6(f), \( i_d \) is adjusted to \( I_r \) during the LLLG fault. After fault removal, \( i_d \) is discharged to the pre-fault current value by \( r_d \) and the voltage drops on the semi-conductor devices.

When crowbar protection is triggering in the modern DFIG-based wind turbines, it causes high stress on the mechanical parts of the system, including the shaft and gear box as shown in Fig. 6(g). However, with the implementation of the proposed approach, not only the first peak point of the electrical torque in the initial moments of the fault has been limited successfully, but also the large electrical oscillations have been reduced.

Fig. 6(h) presents the generator rotor speed. As can be concluded, the proposed scheme can effectively decrease the rotor speed oscillations during the fault, in comparison with crowbar protection. In general, with the present scheme, the DFIG can stay connected to the grid during the LLLG fault at the PCC.

B. Unbalanced LLG Fault

In this section, the performance of the proposed approach is evaluated during the LLG fault (B and C phases to G, Fig. 5(c)) in point F at \( t=4 \) s. The transient response of the key variables of the DFIG, when the proposed FRT scheme is employed, is shown in Fig. 7. As is clear, during the fault, both the rotor currents
and the stator currents are limited to the maximum permissible current (2 p.u.). But crowbar protection just restricts the stator and rotor currents to about 4 p.u. In addition, considering the electrical torque oscillations (Fig. 7(g)) and the rotor speed (Fig. 7(h)), the C-FCL has better performance compared with crowbar protection. In fact, the transient response of the DFIG is improved during the LLG fault, when the proposed approach is utilised for the FRT of the DFIG. Also, the transient response of other variables is kept under control during a voltage dip.

Fig. 6. Simulation results for the LLLG fault at the PCC. The stator current: (a) with crowbar protection, (b) with the proposed FRT scheme. The rotor current: (c) with crowbar protection, (d) with the proposed FRT scheme. (e) The $V_{dc}$. (f) $i_d$. (g) The electrical torque. (h) The rotor speed.
The rotor may experience more severe induced voltages when the fault occurs at particular instants. This section is devoted to an evaluation of the performance of the proposed scheme for three different fault inception instants on the power system frequency cycle \(f_s\), i.e., \(t=0\), \(t=T/4\) and \(t=T/2\) where \(T = 1/f_s\). The corresponding results for the rotor currents are shown in Fig. 8 during the LG fault at the PCC. As Fig. 8 reveals, the efficiency of the proposed scheme is not affected by changing the fault inception instant.

### C. Effect of Fault Inception Instant

The rotor may experience more severe induced voltages when the fault occurs at particular instants. This section is devoted to an evaluation of the performance of the proposed scheme for three different fault inception instants on the power system frequency cycle \(f_s\), i.e., \(t=0\), \(t=T/4\) and \(t=T/2\) where \(T = 1/f_s\). The corresponding results for the rotor currents are shown in Fig. 8 during the LG fault at the PCC. As Fig. 8 reveals, the efficiency of the proposed scheme is not affected by changing the fault inception instant.

### D. Performance of the Proposed FRT Scheme at Super-Synchronous and Sub-Synchronous Speeds

The output active power of the DFIG is a function of the wind speed. Any change in the wind speed can cause the DFIG to change its operating mode from a super-synchronous speed to a sub-synchronous speed, and vice versa. In this section, the performance of the proposed FRT scheme is evaluated during the LLLG
fault at point F for two typical wind speeds, including 15 m/s, super-synchronous speed, and 8 m/s, sub-synchronous speed. The FRT behaviour of the DFIG’s rotor currents is shown in Fig. 9 during the LLLG fault for both modes of operation. With regard to Fig. 9(a) and (b), the C-FCL based FRT scheme operates effectively in comparison with crowbar protection during the super-synchronous speed, limiting the rotor over-currents to less than 2 p.u. The same situation occurs during sub-synchronous speed in Fig. 9(c) and Fig. 9(d), and the proposed scheme effectively restricts the transient rotor over-currents.

Fig. 8. Transient response of the rotor current during the LG fault at the PCC, for the different fault inception instants.

Fig. 9. Transient performance of the rotor currents in two modes of operation of the DFIG during the LLLG fault at the PCC. (a) and (c) crowbar protection. (b) and (d) the proposed FRT scheme.
VII. EXPERIMENTAL RESULTS

To prove the effectiveness of the proposed approach from a practical point of view, some simplifications are considered in the experimental section. Due to operation of the DC chopper in the fault, the DC-link voltage is fixed. Therefore, the DC-link capacitor and the DC-chopper, as shown in Fig. 2(b), are represented by a fixed DC source, \( V_{DC} \). As a result, only the RSC operation is taken into account. Furthermore, in the DFIG setup, due to the fault in the terminal, high voltage induced in the rotor causes high currents in the RSC. To simulate these high currents in the RSC in the experiment, the fault occurs in the AC side terminal of the RSC, a similar situation to the DFIG setup, which is faced with the fault in the terminal. The layout of the experimental setup is shown in Fig. 10.

The experimental parameters are presented in Table IV. Experiments are carried out for two cases:

**Case 1:** without the proposed C-FCL.

**Case 2:** with the proposed C-FCL in the DC-link.

After the LLLG fault, in case 1, the current level in the AC side of the RSC increases more than 3 A, as shown in Fig. 11(a). The same situation occurs during the LLG fault considering Fig. 11(b) for case 1. However, in case 2, considering Fig. 11(c) and 11(d), the C-FCL ensures that the fault current level of the RSC in the DC and the AC sides is restricted to less than 0.75 A during the LLLG and LLG faults, respectively.

<table>
<thead>
<tr>
<th>DC source parameters</th>
<th>( V_{DC} ) (two series DC power supplies, GPC-3030)= 80 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>The C-FCL parameters</td>
<td>( V_c=3.5 \text{ V} ), Single phase diode bridge rectifier BR354: 400 V 35 A</td>
</tr>
<tr>
<td></td>
<td>IGBT switch IKW75N60T: 75 A 600 V. ( L_d=50 \text{ mH} ), ( r_d=0.3 \Omega ). ( r_p=15 \Omega ).</td>
</tr>
<tr>
<td>The RSC parameters</td>
<td>Superfast NPT-IGBT modules SKM50GB063D: 50 A 600 V. Output frequency=60 Hz. Carrier frequency= 1080 Hz</td>
</tr>
<tr>
<td></td>
<td>Control strategy: SPWM by MATLAB software linked to dSPACE CP1104 environment</td>
</tr>
<tr>
<td>Fault characteristics</td>
<td>Fault duration=150 ms. Fault switch: three phase TTL controlled switch, 415 V and 16 A</td>
</tr>
</tbody>
</table>
Fig. 10. Layout of experimental setup.

Fig. 11. Experimental results during the fault at the AC side of the RSC (current per division and time per division shown on the captured figures). The output AC currents of the RSC and $i_d$ for case 1 during: (a) the LLLG fault, (b) the LLG fault. The output AC currents of the RSC and $i_d$ for case 2 during: (c) the LLLG fault, (d) the LLG fault.
VIII. CONCLUSION

This paper presented the DC-link C-FCL based FRT scheme to improve the FRT capability of DFIG-based wind turbines. The proposed C-FCL scheme is an innovative concept of the application of FCLs in the field of FRT capability improvement of the DFIG. The C-FCL has a single phase setup (a simple power circuit topology) in the DC side of the RSC to limit the rotor high over-currents during the various grid faults, even at zero grid voltage. Furthermore, high $di/dt$, initiated at the first moment of the fault, is effectively suppressed. In the proposed approach, the RSC is controlled by a conventional control scheme (DTC) in normal conditions, as well as during the fault. From the extensive simulation studies carried out in the PSCAD/EMTDC software, it is revealed that the proposed FRT scheme can provide promising performance during balanced and unbalanced grid faults. Moreover, it is shown that changing the fault inception instant does not have any effect on the performance of the proposed FRT scheme. The main concept of the proposed approach has been validated by a three phase experimental setup. To sum up, the results obtained show that the proposed scheme enables the DFIG to remain connected with the utility grid during the faults in the power system, without blocking the switching pulses of the RSC. Therefore, it eliminates crowbar activation problems and subsequent complications in the DFIG-based wind turbines.

IX. REFERENCES


