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Thermionic cooling of optoelectronic and microelectronic devices

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Abstract - Solid-state thermionic cooling has gained attention recently because of its potential high cooling power. Thermionic devices based on semiconductor heterostructures utilize the band-edge offset at a heterojunction as the thermionic emission potential barrier and a thin layer to separate the cold and hot junction. In this paper, we present the behavior of thermionic coolers with periodic barriers using gallium arsenide/aluminium gallium arsenide ($GaAs/Al_xGa_{1-x}As$) semiconductor heterostructures. The exact numerical calculation to model the device performance has shown that the thermal efficiency in a multilayer structure is optimised when the effect of phonon scattering is introduced in the model. Besides, the thermal efficiency depends critically on applied bias.

A. Introduction

When a piece of metal (labeled as cathode) in contact with a heat source, it will emit electrons. This process is called thermionic emission. If the hot electrons are absorbed by a cooler anode, and they can flow back to the cathode through an external load, this will generate electricity. This is a thermionic generator. If this cycle inverted, a thermionic cooler is created. A simple thermionic cooler is shown in Figure 1.

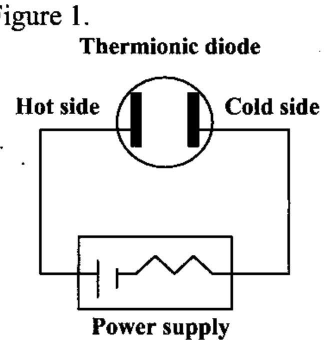

Figure 1: Schematic diagram of simple thermionic cooler.

Cooling using thermionic emission was proposed in 1994 by G.D.Mahan [1]. In his original paper, the cooler had two metal plates separated by a vacuum or air. However, this device is practical at room temperature only if the metal electrodes have a low work function of 0.3 eV or less. However, most materials having work functions less than 0.3 eV are unstable, therefore, the vacuum-based thermionic cooler is impractical. Later, Mahan suggested a new method of cooling by thermionic emission of electrons over periodic barriers in a multilayer

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geometry [2,3]. The multilayer systems such as semiconductor-semiconductor, and metal-semiconductor can easily produce a small work function, and this is determined by the band-edge discontinuity between heterolayers.

Experimentally, A. Shakouri and co-workers have constructed semiconductor multilayers for use as thermionic coolers [4-6]. In these systems, the band offsets between successive layers serve as the periodic barriers. The thermionic coolers of the Shakouri group in single barrier InP/InGaAsP heterostructures have given a cooling of 0.5° C at room temperature of 20° C. The group have recently reported 4° C of cooling in Si/SiGe superlattice barriers [7].

We are trying a different approach of having the multilayers of alternate layers of GaAs and AlGaAs. The material is a promising candidate for high-speed electronics and optoelectronic devices because the lattice parameter difference between GaAs and $Al_xGa_{1-x}As$ is very small, which allows the conduction band-edge to be easily tailored for specific application. In the following section, a design and numerical simulation results of a multilayer thermionic cooler based on this system will be presented.

B. Device design and simulation

The schematic of the device structures are depicted in Figures 2 and 3. The multilayer thermionic cooler structure used in this work is grown on n^+- GaAs substrate by metal organic chemical vapor deposition (MOCVD). The structure consists of ten periods of GaAs-$Al_{0.05}Ga_{0.95}As$ barrier layers surrounded by heavily doped n-GaAs cathode and anode layers with thickness of 100 nm respectively, and doped to 2 x 10^{18} cm^{-3}. The periodic barriers are undoped with thickness of 50 nm for each layer. AuGe is used for top contact metallization, and InGa eutectic is used for bottom substrate contact. Growth and device fabrication were performed at the Electronic Materials Engineering Laboratory, Australian National University, Canberra, Australia.

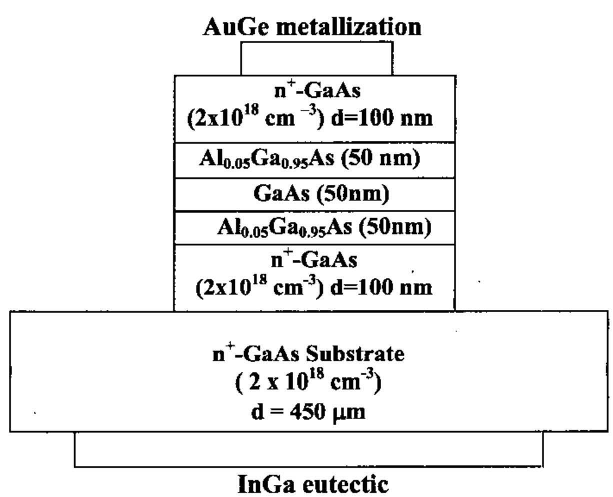

Figure 2: Schematic diagram of multilayer thermionic cooler based on GaAs/ $Al_{0.05}Ga_{0.95}As$ semiconductor heterostructures.

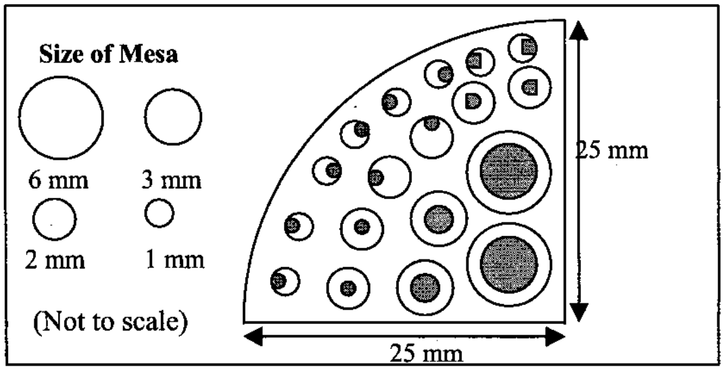

Figure 3: Mesa and metallization of device. The shaded areas showing the metallization.

In order to understand the thermionic emission cooling in heterostructures, an exact numerical calculation is used to simulate the performance of the device. Details of the calculations are lengthy, and are beyond the scope of the present paper. A longer manuscript has been prepared where the model is discussed in depth [8].

Figures 4 and 5 illustrate the thermal efficiency of multilayer coolers as a function of applied bias. In our examples here, we used ten-barrier structures, and fixed temperature difference and work function to 0.02 K and 0.07 eV respectively. For comparison, an InP-based system is illustrated in both plots. Figure 4 shows the thermal efficiency as a function of applied bias when the effect of interface phonon scattering is ignored in the model. Figure 5 reveals that when the effect of interface phonon scattering is considered in the model, the thermal efficiency for a multilayer structure is improved. The efficiency changes significantly with applied bias. The negative efficiencies shown on both figures are corresponded to a net heat flow into, rather than away from the cold electrode. Under the conditions investigated theoretically here the AlGaAs-based cooler has better efficiency than the InP-based system.

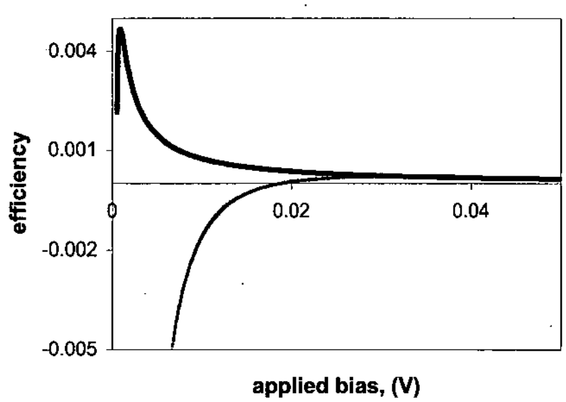

Fig. 4: Thermal efficiency as a function of applied bias for 10-barrier structure neglecting phonon scattering. The upper thick line is a GaAs-based, and lower thin line is an InP based sample.

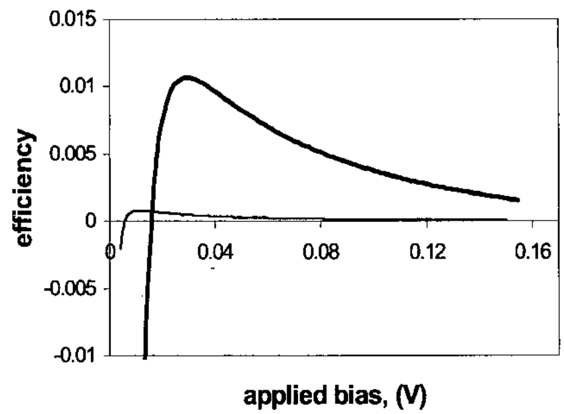

Figure 5: Thermal efficiency as a function of applied bias for 10-barrier structure including phonon scattering. The upper thick line is a GaAs-based, and the lower thin line is an InP-based sample.

Conclusion

In conclusion, we have designed and modelled a GaAs-based multilayer thermionic cooler. Our exact numerical calculation has shown that the thermal efficiency is improved when the effect of phonon scattering is considered in the model. The thermal efficiency depends critically on applied bias. The experimental analysis and methods for further improving the device performance are now under development.

Acknowledgements

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