1980

Apple I/O card documentation

P.J. McKerrow

University of Wollongong, phillip@uow.edu.au

Recommended Citation


http://ro.uow.edu.au/compsciwp/19
APPLE I/O CARD DOCUMENTATION

1. Specifications of Card

8 digital outputs, TTL level, sink 40mA, source 10mA
8 digital inputs, TTL level, maximum 20μA
1 Analog output 0-10V, 5mA maximum output current
1 Analog input 0-10V, 3KΩ minimum input impedance

Variations

1. digital outputs can be used as digital inputs
2. Analog output variable between ±10V by changing reference voltage and reference resistor.
3. Analog input can be changed to -5, -0, +5V by removing link Z.

2. Bibliography

1. Terrapin Turtle Instruction and Assembly Manual.

3. Installation

The card can be inserted into any of the I/O slots on the Apple mother board. The attached programs are written for slot 2. The components go toward the right side and I/O connectors toward the front. Plug I/O cable into card before installing into the Apple.

N.B. Power should be off when card is inserted or removed.
4. Addressing

a. Base Address (A)

<table>
<thead>
<tr>
<th>Slot No.</th>
<th>Hex Address</th>
<th>Decimal Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>C080</td>
<td>-16256</td>
</tr>
<tr>
<td>1</td>
<td>C090</td>
<td>-16240</td>
</tr>
<tr>
<td>2</td>
<td>C0A0</td>
<td>-16224</td>
</tr>
<tr>
<td>3</td>
<td>C0B0</td>
<td>-16208</td>
</tr>
<tr>
<td>4</td>
<td>C0C0</td>
<td>-16192</td>
</tr>
<tr>
<td>5</td>
<td>C0D0</td>
<td>-16176</td>
</tr>
<tr>
<td>6</td>
<td>C0E0</td>
<td>-16160</td>
</tr>
<tr>
<td>7</td>
<td>C0F0</td>
<td>-16144</td>
</tr>
</tbody>
</table>

b. Input/Output Address

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A + 0</td>
<td>Data Register A</td>
</tr>
<tr>
<td>A + 1</td>
<td>Control Register A</td>
</tr>
<tr>
<td>A + 2</td>
<td>Data Register B</td>
</tr>
<tr>
<td>A + 3</td>
<td>Control Register B</td>
</tr>
<tr>
<td>A + 8</td>
<td>Analog Input</td>
</tr>
</tbody>
</table>

5. PIA Initialization and Digital I/O

a. A side Digital Out

10    Poke A + 1, 0    Select Data Direction Register
20    Poke A, 225      Select lines as outputs
30    Poke A+1, 52     Select Data Reg and Enable Buffer
40    Poke A, Data     Output Data
b. A side Digital In

10 Poke A + 1, \( \emptyset \) \hspace{1cm} \text{Select Data Direction Register}
20 Poke A, \( \emptyset \) \hspace{1cm} \text{Select lines as Inputs}
30 Poke A + 1, 6\( \emptyset \) \hspace{1cm} \text{Select Data Reg and Disable Buffer}
40 DATA = PEEK(A) \hspace{1cm} \text{Read Data}

c. B side Digital In

10 Poke A + 3, \( \emptyset \) \hspace{1cm} \text{Select Data Direction Register}
20 Poke A + 2, \( \emptyset \) \hspace{1cm} \text{Select lines as inputs}
30 Poke A + 3, 6\( \emptyset \) \hspace{1cm} \text{Select Data Reg \& Enable Buffer}
40 DATA = PEEK(A + 2) \hspace{1cm} \text{Read Data}

6. Analog I/O

a. Initialize PIA, A side as required for Digital Signals, B side as Digital in.

b. Analog in

10 Poke A + 3, 52 \hspace{1cm} \text{Start conversion}
20 X := PEEK(A + 3) \hspace{1cm} \text{Read status}
30 IF X < 128 then 20 \hspace{1cm} \text{Is conversion complete}
40 Input = PEEK(A + 2) \hspace{1cm} \text{Read Data}
50 Poke A + 3, 6\( \emptyset \) \hspace{1cm} \text{Finish conversion}

N.B. 1. Between the start and finish of conversion (CB2 Low) the Analog Input has control of the B Side Data Lines and the B Side Digital Input Buffer is disabled.

2. CB2 going low starts the conversion. CB2 high tristates the ADC outputs

3. CB1 going low indicate conversion complete.

4. CB2 is controlled by Control Register B bits 5, 4, 3
   \( 11\emptyset = \text{low} \hspace{1cm} 111 = \text{high} \)

5. The status of CB1 can be read from Control Register B bit 7. It will be set (high) when CB1 input signal goes low if Control Register B bits 1 and \( \emptyset \) are set to zero. It can also be set to interrupt the processor when the conversion is complete.
b. Analog Out

10  Poke A + 8, Data  Write data to address

7. Turtle Cable - from I/O Card to Molex Connector

<table>
<thead>
<tr>
<th>Connector A (f)</th>
<th>Molex Plug</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
<td>Data</td>
</tr>
<tr>
<td>1</td>
<td>RMF</td>
</tr>
<tr>
<td>2</td>
<td>RMB</td>
</tr>
<tr>
<td>3</td>
<td>LMF</td>
</tr>
<tr>
<td>4</td>
<td>LMB</td>
</tr>
<tr>
<td>5</td>
<td>Light</td>
</tr>
<tr>
<td>6</td>
<td>Pen</td>
</tr>
<tr>
<td>7</td>
<td>Horn</td>
</tr>
<tr>
<td>7</td>
<td>Tone</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Connector B (n)</th>
<th>Molex Plug</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
<td>Data</td>
</tr>
<tr>
<td>1</td>
<td>LT</td>
</tr>
<tr>
<td>2</td>
<td>RT</td>
</tr>
<tr>
<td>3</td>
<td>FT</td>
</tr>
<tr>
<td>4</td>
<td>BT</td>
</tr>
<tr>
<td>5</td>
<td>+12V (from 12V supply</td>
</tr>
<tr>
<td>9</td>
<td>0V (from 12V supply &amp; I/O card)</td>
</tr>
</tbody>
</table>

grey wire from I/O card not connected
LIST
10 PRINT "APPLE I/O TEST"
20 PRINT "P.J.MCKERROW.......5.3.80"
40 C=0
50 W=-16224
60 R=-16222
70 REM C=ERROR COUNT, I=TEST COUNT
80 REM W=WRITE ADDRESS, R=READ ADDRESS
90 REM X=DATA OUT, Y=DATA IN, T=TEMP
91 PRINT
92 PRINT "TEST ERROR DATA"
96 PRINT "OUT IN"
100 FOR I=1 TO 100
105 GOSUB 300
110 FOR X=1 TO 255
120 POKE W,X
130 Y=PEEK (R)
140 IF Y=X THEN 150
142 C=C+1
144 PRINT I,C,X,Y
150 NEXT X
160 PRINT I,C
170 NEXT I
180 GOTO 400
300 REM INITIALISE PIA
310 POKE W+1,0
320 POKE W,255
330 POKE W+1,52
340 POKE R+1,0
350 POKE R,0
360 POKE R+1,60
370 RETURN
400 END
LIST
10 PRINT "APPLE ANALOG I/O TEST"
20 PRINT " P.J.MCKERROW....7.3.80"
80 REM INITIALISE PIA
90 PRINT "FOR 10 SLOT 2"
91 REM A=ADDRESS,V=MAX VOLTS OUT
92 V=10
95 A=-16224
100 POKE A+1,0
110 POKE A+2,255
120 POKE A+1,52
130 POKE A+3,0
140 POKE A+2,0
150 POKE A+3,60
160 PRINT " ANALOG DATA"
170 PRINT "OUT IN VOLTS OUT *10"
180 O=1
240 GOSUB 2000
250 GOSUB 1000
260 O=2*O
270 IF O=256 THEN O=255
280 IF O<256 THEN 240
300 O1=1
310 O=255-O1
320 GOSUB 2000
330 GOSUB 1000
340 O1=2*O1
350 IF O1<255 THEN 310
400 END
1000 REM WAIT LOOP
1010 T=0
1020 T=T+1
1030 IF T<500 THEN 1020
1040 RETURN
2000 REM I/O ROUTINE
2010 POKE A+8,0
2020 POKE A+3,52
2030 X= PEEK (A+3)
2040 IF X<128 THEN 2030
2050 I= PEEK (A+2)
2060 POKE A+3,60
2070 VO=10*O*V/255
2080 PRINT O,I,VO
2090 RETURN
LIST

10 PRINT "TURTLE TEST"
20 PRINT
30 PRINT "SUPPORT THE TURTLE SO THAT THE WHEELS ARE FREE TO TURN"
90 GOSUB 1000
100 W=-16224
110 R=-16222
190 REM INITIALISE PIA
200 POKE W+1,0
210 POKE W,255
220 POKE W+1,52
230 POKE R+1,0
240 POKE R,0
250 POKE R+1,60
290 PRINT
300 PRINT "OUTPUT TEST"
310 PRINT
320 PRINT "TEST ORDER"
330 PRINT "RIGHT MOTOR FORWARD"
340 PRINT "RIGHT MOTOR REVERSE"
350 PRINT "LEFT MOTOR FORWARD"
360 PRINT "LEFT MOTOR REVERSE"
365 PRINT "LIGHTS"
370 PRINT "PEN DOWN"
380 PRINT "LOW TONE"
390 PRINT "HIGH TONE"
392 GOSUB 1000
395 A=1
400 POKE W,A
410 GOSUB 1000
420 A=2*A
430 IF A=128 THEN A=192
440 IF A(255 THEN 400
450 POKE W,0
500 PRINT
510 PRINT "INPUT TEST"
520 PRINT "OPERATE MICRO SWITCHES BY TOUCHING THE DOME"
525 FOR I=1 TO 8
530 A= PEEK (R)
540 IF A=247 THEN PRINT "BACK TOUCH"
550 IF A=251 THEN PRINT "FRONT TOUCH"
560 IF A=253 THEN PRINT "RIGHT TOUCH"
570 IF A=254 THEN PRINT "LEFT TOUCH"
580 IF A=255 THEN PRINT "NO TOUCH"
585 PRINT "DATA IS ",A
590 GOSUB 1000
600 NEXT I
610 END
1000 REM WAIT LOOP
1010 C=0
1020 C=C+1
1030 IF C(300 THEN 1020
1040 RETURN
PROGRAM EXAM;
(*USED TO LOOK AT AND MODIFY MEMORY LOCATIONS*)
(* PHILLIP MCKERROW 11.7.80 *)
VAR TERM, DATA, DAT1, ADDR: INTEGER;
    REQUEST1, REQUEST2, RUBISH: CHAR;
PROCEDURE POKE (DATA, ADDR: INTEGER);
EXTERNAL;
FUNCTION PEEK (ADDR: INTEGER): INTEGER;
EXTERNAL;
BEGIN
    TERM:=0;
    WHILE TERM=0 DO
        BEGIN
            WRITELN (OUTPUT, 'ENTER REQUEST PEEK, POKE, QUIT');
            READ (INPUT, REQUEST1, REQUEST2);
            WHILE NOT EOLN (INPUT) DO READ (INPUT, RUBISH);
            READLN;
            IF REQUEST1='P' THEN
                BEGIN
                    IF REQUEST2 = 'E' THEN
                        BEGIN
                            WRITELN (OUTPUT, 'ENTER ADDRESS - DECIMAL');
                            READLN (INPUT, ADDR);
                            DATA := PEEK(ADDR);
                            WRITELN (OUTPUT, 'CONTENTS IS ', DATA);
                        END
                    ELSE IF REQUEST2 = '0' THEN
                        BEGIN
                            WRITELN (OUTPUT, 'ENTER DATA 0-255, ADDRESS - DECIMAL');
                            READLN (INPUT, ADDR);
                            DATA := PEEK(ADDR);
                            WRITELN (OUTPUT, 'CONTENTS IS ', DATA);
                        END
                END
            END
READLN (INPUT, DATA, ADDR);
POKE (DATA, ADDR);
DAT1:=PEEK(ADDR);

IF DAT1>DATA THEN WRITELN(‘ERROR ’, DATA, ’ ’, DAT1);
END;
END
ELSE IF REQUEST1 =’Q’ THEN TERM := 1;
END;

WRITELN (OUTPUT, ’BYE BYE’);
END.

; ASSEMBLER ROUTINES TO CONTROL TURTLE
; THE UNIVERSITY OF WOLLONGONG
; PHILLIP MCKERROW 4.6.80
; PEEK AND POKE
;
; MACRO DEFINITIONS
;
; MACRO POP ADDRESS
; POPS 16 BIT ARG FROM STACK TO ADDRESS
;
.

.MACRO POP
PLA ; PULL LS BYTE
STA %1
PLA ; PULL MS BYTE
STA %1+1
.ENDM
; MACRO PUSH ADDRESS
; PUSHES 16 BIT ARG TO STACK
;
; MACRO PUSH
LDA %1+1
PHA ; PUT MS BYTE
LDA %1
PHA ; PUT LS BYTE
. ENDM

; FUNCTIONS
;
; FUNCTION PEEK(ADDRESS: INTEGER): INTEGER;
; RETURNS CONTENTS OF SPECIFIED ADDRESS
; 8 BITS OF DATA RETURNED IN LS BYTE
; MS BYTE SET TO ZERO
;
; FUNC PEEK, 1
ADDR . EQU 0  ; ADDRESS OF DATA
POP RETURN ; GET RETURN ADDRESS
PLA ; STACK BIAS
PLA
PLA
PLA
POP ADDR ; GET ADDRESS
LDA $0
PHA ; SET MS BYTE TO 0
LDY $0
LDA @ADDR,Y ;GET DATA
PHA ;RETURN DATA
PUSH RETURN
RTS ;GO BACK

RETURN .WORD 0,0

; ;

; PROCEDURE DEFINITIONS
;

; PROCEDURE POKE(DATA, ADDR: INTEGER)
;PROCEDURE TO WRITE TO ADDRESS
;

.PROC POKE,2
ADDR .EQU 0
POP RETURN ;SAVE RETURN ADDRESS
POP ADDR ;MEMORY LOCATION
LDX $0
PLA ;GET OUTPUT
STA @ADDR,X ;POKE
PLA ;CLEAN UP STACK
PUSH RETURN
RTS ;GO BACK
RETURN .WORD 0,0

.END
INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

<table>
<thead>
<tr>
<th>RS1</th>
<th>RS0</th>
<th>CRA 2</th>
<th>CRB-2</th>
<th>Location Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>Peripheral Register A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>Data Direction Register A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Control Register A</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>Peripheral Register B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>Data Direction Register B</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Control Register B</td>
</tr>
</tbody>
</table>

X = Don't Care

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset. Details of possible configurations of the Data Direction and Control Register are as follows.

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

<table>
<thead>
<tr>
<th>CRA-1 (CRB-1)</th>
<th>CRA-0 (CRB-0)</th>
<th>Interrupt Input CA1 (CB1)</th>
<th>Interrupt Flag CRA-7 (CRB-7)</th>
<th>MPU Interrupt Request IRQA (IRQB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>✷ Active</td>
<td>Set high on ✷ of CA1 (CB1)</td>
<td>Disabled — IRQ remains high</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>✷ Active</td>
<td>Set high on ✷ of CA1 (CB1)</td>
<td>Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>✷ Active</td>
<td>Set high on ✷ of CA1 (CB1)</td>
<td>Disabled — IRQ remains high</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>✷ Active</td>
<td>Set high on ✷ of CA1 (CB1)</td>
<td>Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high</td>
</tr>
</tbody>
</table>

Notes:
1. ✷ indicates positive transition (low to high)
2. ✷ indicates negative transition (high to low)
3. The interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs after CRA-0 (CRB-0) is written to a "one".
Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) - The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals IRQA and IRQB, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

<table>
<thead>
<tr>
<th>CRA-5 (CRB-5)</th>
<th>CRA-4 (CRB-4)</th>
<th>CRA-3 (CRB-3)</th>
<th>Interrupt Input CA2 (CB2)</th>
<th>Interrupt Flag CRA-6 (CRB-6)</th>
<th>MPU Interrupt Request IRQA (IRQB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>↑ Active</td>
<td>Set high on ↑ of CA2 (CB2)</td>
<td>Disabled — IRQ remains high</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>↑ Active</td>
<td>Set high on ↑ of CA2 (CB2)</td>
<td>Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>↑ Active</td>
<td>Set high on ↑ of CA2 (CB2)</td>
<td>Disabled — IRQ remains high</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>↑ Active</td>
<td>Set high on ↑ of CA2 (CB2)</td>
<td>Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high</td>
</tr>
</tbody>
</table>

Notes:
1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs after CRA-3 (CRB-3) is written to a "one".

<table>
<thead>
<tr>
<th>CRB-5</th>
<th>CRB-4</th>
<th>CRB-3</th>
<th>Cleared</th>
<th>CB2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Low on the positive transition of the first &quot;E&quot; pulse following an MPU Write &quot;B&quot; Data Register operation.</td>
<td>High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Low on the positive transition of the first &quot;E&quot; pulse after an MPU Write &quot;B&quot; Data Register operation.</td>
<td>High on the positive edge of the first &quot;E&quot; pulse which occurred while the part was deselected.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Low when CRB-3 goes low as a result of an MPU Write in Control Register &quot;B&quot;.</td>
<td>Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register &quot;B&quot; that changes CRB-3 to &quot;one&quot;.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register &quot;B&quot; results in clearing CRB-3 to zero.</td>
<td>High when CRB-3 goes high as a result of an MPU Write into Control Register &quot;B&quot;.</td>
</tr>
</tbody>
</table>
Control of CA2 and CB2 Peripheral Control Lines
(CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

### TABLE 6 – CONTROL OF CA-2 AS AN OUTPUT

<table>
<thead>
<tr>
<th>CRA-5</th>
<th>CRA-4</th>
<th>CRA-3</th>
<th>Cleared</th>
<th>CA2</th>
<th>Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Low on a negative transition of E after an MPU Read ”A” Data operation.</td>
<td>High when the interrupt flag bit CRA-7 is set by an active transition of the CA1 signal.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Low on negative transition of E after an MPU Read ”A” Data operation.</td>
<td>High on the negative edge of the first “E” pulse which occurs during a deselect.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Low when CRA-3 goes high as a result of an MPU Write to Control Register “A”.</td>
<td>Always low as long as CRA-3 is low. Will go high on an MPU Write to Control Register “A” that changes CRA-3 to “one”.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Always high as long as CRA-3 is high. Will be cleared on an MPU Write to Control Register “A” that clears CRA-3 to a “zero”.</td>
<td>High when CRA-3 goes high as a result of an MPU Write to Control Register “A”.</td>
<td></td>
</tr>
</tbody>
</table>

### PIN ASSIGNMENT

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VSS</td>
</tr>
<tr>
<td>2</td>
<td>PA0</td>
</tr>
<tr>
<td>3</td>
<td>PA1</td>
</tr>
<tr>
<td>4</td>
<td>PA2</td>
</tr>
<tr>
<td>5</td>
<td>PA3</td>
</tr>
<tr>
<td>6</td>
<td>PA4</td>
</tr>
<tr>
<td>7</td>
<td>PA5</td>
</tr>
<tr>
<td>8</td>
<td>PA6</td>
</tr>
<tr>
<td>9</td>
<td>PA7</td>
</tr>
<tr>
<td>10</td>
<td>PB0</td>
</tr>
<tr>
<td>11</td>
<td>PB1</td>
</tr>
<tr>
<td>12</td>
<td>PB2</td>
</tr>
<tr>
<td>13</td>
<td>PB3</td>
</tr>
<tr>
<td>14</td>
<td>PB4</td>
</tr>
<tr>
<td>15</td>
<td>PB5</td>
</tr>
<tr>
<td>16</td>
<td>PB6</td>
</tr>
<tr>
<td>17</td>
<td>PB7</td>
</tr>
<tr>
<td>18</td>
<td>CB1</td>
</tr>
<tr>
<td>19</td>
<td>CB2</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
</tr>
</tbody>
</table>

### PACKAGE DIMENSIONS

**CASE 715-02 (CERAMIC)**

**SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS.**

**DIMENSIONS (MILLIMETERS)**

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.960</td>
<td>2.020</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>0.565</td>
<td>0.615</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>0.254</td>
<td>0.256</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>0.065</td>
<td>0.067</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>0.008</td>
<td>0.013</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>1.400</td>
<td>1.400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>0.100</td>
<td>BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>1.780</td>
<td>1.780</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>0.007</td>
<td>0.010</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>0.100</td>
<td>0.100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.050</td>
<td>0.050</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>1.060</td>
<td>1.060</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>0.080</td>
<td>0.080</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**

1. Leads, true positioned within 0.25 mm (0.010) dia (at seating plane), at max. mat’l condition.
Component Overlay

Test Cable

APPLE I/O-Overlay
The University 18/4 Bl
of Wollongong