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Harmonic control techniques for inverters and adaptive active power filters

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Harmonic Control Techniques for Inverters and Adaptive Active Power Filters

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In the name of God, the merciful and compassionate

Dedicated to my wife

who was beside me during these hard years

and my mother

who first encouraged me to undertake postgraduate studies

DECLARATION

This is to certify that the work presented in this thesis was performed by me, unless specified otherwise, and no part of it has been submitted previously for any other degree to any other university or similar institution.

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Ali Yazdian Varjani

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ABSTRACT

This thesis is concerned with the general issue of power quality. The specific areas of interest include harmonic distortion and its minimisation. In particular the thesis considers a PWM switching strategy which yields near optimal performance in terms of harmonic distortion as well as on-line harmonic detection mechanisms and adaptive active power filtering solutions.

For the purpose of load side harmonic reduction, a novel equal area based PWM (EAPWM) switching strategy is developed which is suitable for voltage source full bridge inverter applications. The objective of this strategy is to minimise both the harmonic distortion and the switching losses in the inverter. Switching losses in the inverter are minimised by developing a hybrid switching sequence. The harmonic distortion is minimised by adopting a technique which ensures that the PWM pulses are placed at appropriate positions of choice based on an equal area criterion so that their areas are better matched with the areas under the reference waveform.

The EAPWM technique is evaluated and its performance is compared with existing PWM techniques including natural and regular PWM switching strategies. The performance evaluation and comparison is based on the total harmonic distortion and maximum inverter fundamental output voltage. For a case where the ideal output waveform is sinusoidal it is shown through simulation that the proposed technique provides a PWM output with minimum harmonic distortion and maximum fundamental voltage.

The second issue addressed by the thesis is adaptive active power filtering. The objective is to develop an economical solution where a partial and flexible harmonic reduction technique is provided such that the established harmonic standards are satisfied. Partial and selective compensation of those individual harmonics which exceed the

recommended levels as set by regulatory bodies reduces the rating of active power filters thus leading to cost savings. This approach contrasts with existing techniques where the objective is to reduce all possible harmonic components to zero.

A new control strategy for active power filters that combines adaptive online harmonic estimation with partial and selective harmonic compensation schemes has been implemented within an integrated controller. To have an accurate online estimation of harmonic components, a new adaptive structure based on a combination of resonator filter bank and frequency demodulation frequency tracking is proposed.

Performance evaluation of the proposed technique for harmonic estimation for time-varying nonlinear load is carried out where the simulation results show that the proposed filter bank structure provides better performance when compared to widely used conventional technique such as short term Fourier transform. The proposed control strategy has been implemented using a digital signal processor. Experimental results from a laboratory prototype are presented showing steady state and transient performance. It is shown that the proposed harmonic estimation together with the flexible harmonic compensation scheme provides an efficient solution in reducing the power rating of the active power filter while limiting specific harmonics to desired levels of compensation.

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∇_a	Partial derivative of the mean squared error
γ	Forgetting factor
Γ	Smoothed estimate of the power of the ∇_a
ω	Angular phase
Φ	Phase angle
ε	Small positive real number
μ	Step size
ξ	Variance of the error signal
$\varepsilon(n)$	White noise
Δf	Fundamental frequency deviation
ΔI_{high}	Upper boundary of the hysteresis band
ΔI_{low}	Lower boundary of the hysteresis band
τ_k	k^{th} pulsewidth
ϕ_h	Magnitude of the h^{th} input signal
a	Bandpass filter parameter
A_h	Magnitude of the h^{th} input signal
C_{dc}	DC link capacitor
C_k	Fourier coefficients of the output signal
D_k	Fourier coefficients of the output signal
$E(e^2)$	Expected error
$e(n)$	Error signal
f_o	Reference waveform frequency
f_p	Centre frequency
f_s	Sampling frequency
f_{sw}	Switching frequency
g	Filter bank feedback gain
h	Harmonic order

$H_{BP}(z)$	Bandpass transfer function
$H_r(z)$	Resonator transfer function
i_{apf}	Active filter current
i_{comp}	Inverter compensation current
i_{load}	Load current
i_{losses}	Compensating switching losses current
I_h	Harmonic amplitude vector
I_h^{ref}	Reference load current weighting
$i_{reactive}$	Reactive current of the load
i_{ref}	Active power filter reference current
i_s	Source current
$K_{reactive}$	Constant which controls the level of fundamental reactive power
L_{apf}	Active power filter Inductance
M	Modulation Index
N	Number of filter in filter bank
p	Frequency ratio
$\bar{p}$	Average power
$\tilde{p}$	Oscillatory power .
$p(t)$	Instantaneous power
r	Bandpass IIR filter bandwidth parameter
SW	Switching command
T_{tri}	Triangular waveform period
V_{dc}	DC voltage
V_m	Peak magnitude of reference waveform
v_{ref}	Reference waveform
v_s	Source voltage
V_{tri}	Triangular voltage waveform
$W(n)$	Window function
$x(t)$	Input signal
$X_{centroid}$	Centroid, pulse position
X_{COI}	Centre of integration
$y^f(n)$	Estimate for $\frac{\partial y(n)}{\partial a}$

CHAPTER 1.

PRELIMINARY

1.1 INTRODUCTION

The widespread use of power electronics-based loads to improve energy efficiency and flexibility has increased the harmonic distortion levels in end use facilities and on the overall power system. The need for reducing distortion in power systems has led to a great deal of research attention in the area of power quality [1].

Regulatory organisations have increased their efforts towards establishing standards which limit the harmonic pollution in power systems [2-5]. Harmonic standards recommend limits on harmonic distortion in two ways. First, limits are placed on the amount of the harmonic current that consumers can inject into a utility network as a preventative action and secondly limits are imposed on the levels of harmonic voltages that utilities can supply to consumers.

1.2 POWER SYSTEM HARMONICS

As stated above, the proliferation of semiconductor devices used in many electronic systems that are essentially exhibiting nonlinear voltage-current characteristics lead to excessive power system voltage and current distortions. The distorted supply voltage can cause further harmonic current distortions in other linear loads [6, 7]. Most distorted current waveforms contain harmonic components which are primarily integer multiples of

the fundamental frequency. However, it is also possible to have non-integer multiples for certain types of loads.

1.2.1 Harmonic Sources

There are many types of nonlinear loads that cause current harmonics. The largest types of nonlinear loads are power electronic converters. These include high voltage DC (HVDC) stations, AC and DC variable speed drives and diode rectifiers systems that are found in many electrical appliances such as televisions and computers. Other nonlinear sources of harmonics include arc furnaces, transformer magnetising impedances, switched mode power supplies and fluorescent lights.

1.2.2 Effects of Harmonic

The harmonic currents that are injected into a power system by harmonic sources can affect the power system voltage and subsequently customer equipment. On the power system side, harmonic currents are one of the main sources of disturbances, causing equipment overheating and deterioration of the performance of electronic equipment. The impact is worse when network resonances amplify harmonic currents. Harmonics may also interfere with relaying and metering to some degree [8]. They can cause interferences with power system control including ripple control, remote load control, protection systems and power plant excitation systems [9]. Harmonics can also cause thyristor firing errors in converter and static var compensator (SVC) installations, metering inaccuracies and false tripping of protective devices.

On the consumer side, the performance of equipment such as motor drives and computer power supplies can be adversely affected by harmonics. The higher order harmonics cause interferences on communication lines or electronically controlled equipment while lower order harmonics increase the heat losses in equipment. Some of these heating problems are proportional to frequency and some are proportional to the square of the frequency which can ultimately shorten the life-expectancy of equipment [8, 10-12].

1.2.3 Measurement of Harmonics

Accurate measurement of power system voltage and current harmonics is necessary to analyse and predict the harmonic behaviour of a power system. The harmonic quantities of interest include the magnitude, phase, and their variation with respect to time.

1.2.3.1 Measurement Techniques

Harmonic measurement techniques are classified into off-line and on-line techniques. Off-line techniques are usually used to identify the harmonics in a stationary signal whereas on-line techniques are used to track the dynamic variation of non-stationary harmonic signals. The non-stationary signals, such as power system voltage and current waveforms are characterised by the changing features in their frequency content and magnitude with respect to time. Therefore, on-line measurement of fundamental frequency and harmonics of such signals require sliding measurement techniques such as digital filtering and short-term Fourier transform. A detailed description of these methods will be presented in Chapter 3.

1.2.4 Standards on Harmonics

Harmonic standards provide guidelines, recommendations, and limits to help assure compatibility between end use equipment and the power system. They also give utilities and customers information about the environment in which equipment is expected to work.

The primary objective of a harmonic standards is to limit actual harmonic voltages on supply systems to acceptable levels (compatibility levels) that will not result in adverse effects on sensitive equipment. Since the harmonic voltages result from harmonic currents and power system impedances, harmonic standards provide guidance on the limitation of harmonic currents injected into power system [13]. Some of these standards also provide information that can be used for economic evaluation of harmonic reduction techniques [10, 14].

1.2.4.1 Australian Standards on Harmonics

The Australian Standard, AS2279.2-91 [4] recommends that the maximum level for total voltage harmonic distortion in industrial applications should be 5%. Further, the above standard applies limits of 2% and 4% for individual even and odd harmonics respectively. The limits may be increased at the discretion of the utilities, if substantiated by a thorough engineering assessment [4]. The utilities can further reduce these levels based on individual agreements [15].

1.3 COMPENSATION OF HARMONICS

When a harmonic source is identified and classified, it is then the responsibility of either the consumer or the utility or both parties to reduce the resulting harmonic distortion level on the power system. When harmonic levels exceed the compatibility limits of power system equipment, appropriate solutions should be employed for mitigation of harmonic effects on equipment. These solutions consist of a reduction of harmonic levels on power system voltage and current or an increase in the levels of compatibility of equipment against the harmonic distortion.

The harmonic compensation will be an extremely cost-sensitive issue when utilities start to enforce harmonic standards. Therefore, the task of choosing a reliable and economical methodology for harmonic reduction from both the industrial end user and utility perspective becomes very important [16]. In the next section a brief review of common harmonic reduction techniques is presented.

1.3.1 Harmonic Reduction Techniques

Harmonic reduction techniques can be classified into two categories including; wave-shaping and filtering techniques as shown in Figure 1.1 [16-18]. These techniques have been chosen by their ability to comply with the harmonic standards, particularly the IEEE-519 [3] requirement on total harmonic distortion (THD) level of connected loads. However, any comparison on the effectiveness of these techniques depends on the type and operating conditions of the load [17].

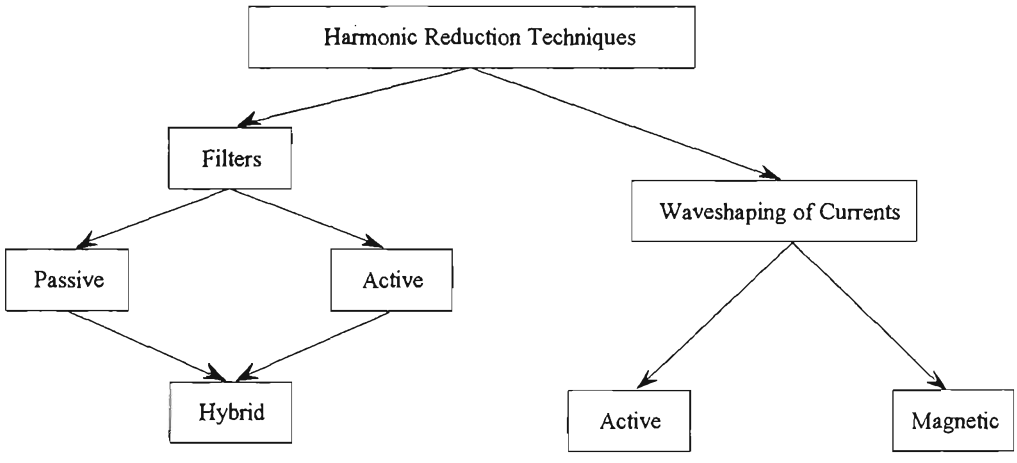


Figure 1.1: Harmonic reduction techniques [17].

In magnetic wave-shaping techniques, the line currents are shaped to have a sinusoidal waveform using magnetic devices such as differential delta transformers or a combination of semiconductor devices together with transformers [19]. Active wave-shaping techniques require controlling the semiconductor devices, such as power factor correction circuits or pulsewidth modulation (PWM) based rectifiers, to ensure that the line currents are sinusoidal [17].

External filters not only suppress harmonics but also provide reactive power compensation. They are often preferred when an improvement in power factor is also required. Active and passive power filters are the most common approaches used for harmonic cancellation and reactive power compensation.

1.3.2 Passive Power Filters

Passive power filters are single frequency filters which absorb individual harmonics. They have been employed to reduce a selected harmonic by tuning the band-pass characteristics of the filter. In time-varying environments an adaptive or automatic tuning feature should be added to these filters [20].

A passive filter as shown in Figure 1.2 consist of a series-resonant inductor-capacitor (LC) circuit tuned to a single frequency. The LC circuit provides a zero impedance path for a selected harmonic current to be filtered. If the line impedance, Z_u, is low the LC circuit should be used with a series impedance Z_s. The application of passive tuned filters may create new system resonances which are dependent on specific system conditions.

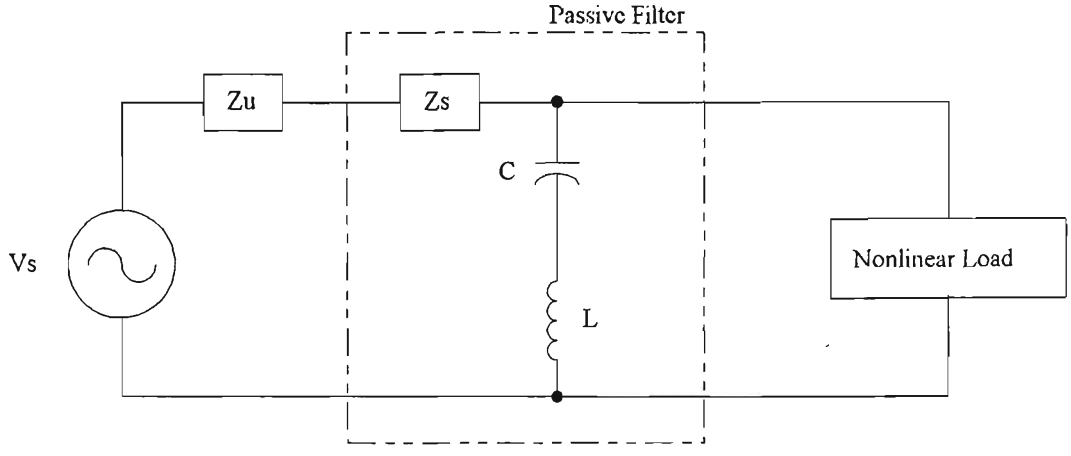


Figure 1.2: Passive power filter.

Passive filter ratings must be coordinated with reactive power requirements of the loads and it is often difficult to design the filters to avoid leading power factor operation for some load conditions. In other words, they often need to be significantly overrated to account for possible harmonic absorption from the neighbouring power system equipment or from other passive filters [20].

1.3.3 Active Power Filters (APF)

In the recent years there has been considerable interest in the use of active filters for reducing harmonic currents in power supply systems [21-24]. In this section, the general concept of active power filters and their applications will be discussed. A comparison of existing control strategies and hardware characteristics of active power filters is also presented [25].

One of the foremost literature reviews was undertaken by Grady *et al* [18] covering different APF circuits with emphasis on both time and frequency domain control strategies. Recent research has concentrated on the combination of series and shunt active power filters [26-29]. Power circuits of active power filters and the different series/parallel combinations are investigated in [29].

1.3.3.1 Principle of Active Power Filter

To cancel harmonic currents, active power filters inject equal-but-opposite current thereby cancelling the original distortion. Active filters have the advantage of being able to compensate for harmonics without fundamental frequency reactive power concerns. This means that the rating of an active filter can be less than that of a passive filter for the

same nonlinear load. Also an active filter will not introduce system resonances that can move a harmonic problem from one frequency to another.

Classification and comparison of the active power filters can be made from different points of view. Generally, comparison of characteristics of active power filters is summarised in terms of; power system connection, power circuit, and employed control strategy [18, 25].

1.3.4 Power System Connection

The power system connection which determines the type of APF configuration depends on the way in which APF's inverter is connected between source and load. An APF can be connected to the power system in shunt, series and hybrid configurations.

1.3.4.1 Shunt Configurations

A general block diagram of a conventional APF shunt topology is shown in Figure 1.3. In this configuration, the corrective current, i_c, is injected at the point of common coupling (PCC) to cancel the harmonics contained in the load current (i_l). The current, i_c, can also provide fundamental reactive power compensation for the load if necessary.

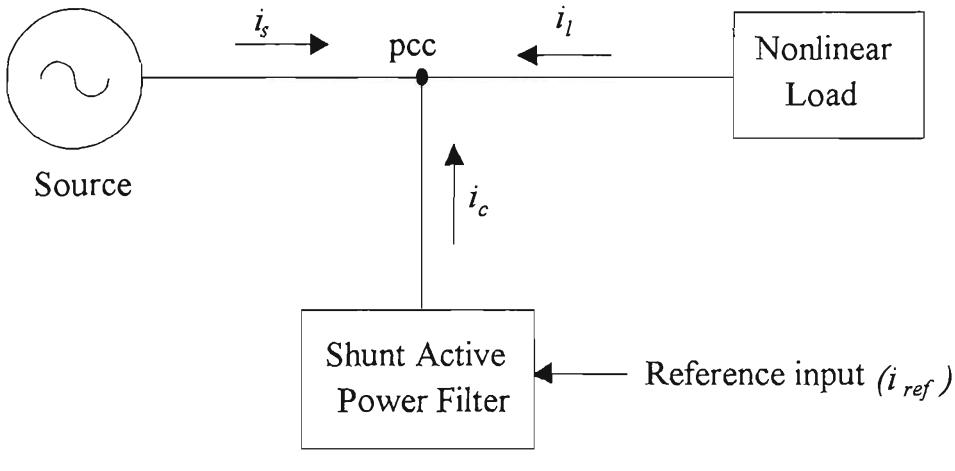


Figure 1.3: Basic principle of shunt active power filter.

The shunt APF is controlled in a closed loop to force the source current (i_s) into a sinusoidal waveform. Two of the main concerns in this configuration are the calculation of the reference input signal (i_{ref}) in steady state and/or transient conditions as well as the response of the system to APF operation. In shunt configurations it is assumed that the load introduces distortions in the form of harmonic currents [29-31].

1.3.4.2 Series Configurations

Figure 1.4 shows a series type of active power filter. In this configuration the active power filter acts as a voltage source in the power system line or as a series filter to prevent the flow of voltage harmonics from the load side to the source.

The voltage drop across the matching transformer of the series filter should be low compared to the nominal line voltage. Thus the power rating of the series active power filter is much smaller than the shunt active filter even though the source currents flow through the matching transformer of the series active power filter. Compared to shunt active power filters, series configurations have some protection difficulties [32].

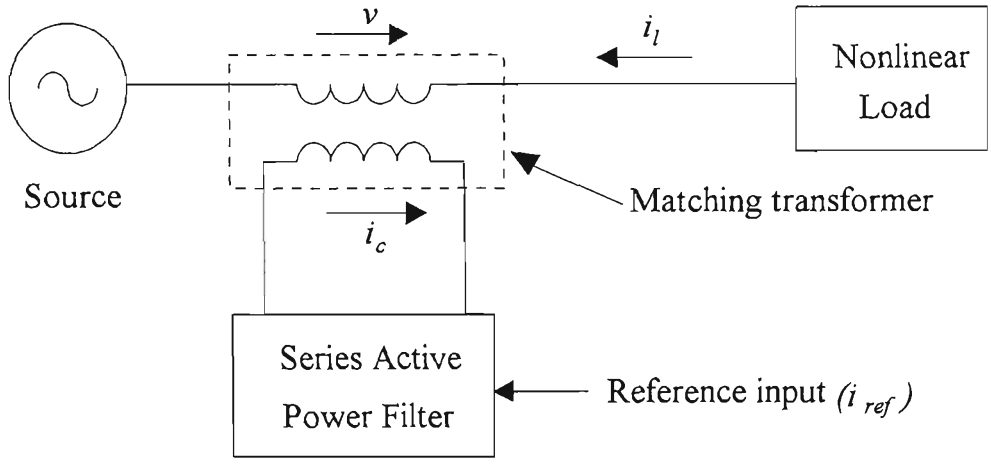


Figure 1.4: Basic principle of series active power filter.

1.3.4.3 Hybrid configurations

Advances in the area of harmonic reduction have reached the point of combining active and passive filters [29]. The aim is to improve the filter reliability by combining the active power filter performance with the passive filter robustness. Hybrid filters can further reduce the cost of the system compared to pure active power filter approach [25, 33, 34]. In hybrid filter configurations, by improving the compensation characteristics of the passive filter a reduction in the rating of active filter can be achieved [16].

There is a variety of possible active and passive filter combinations [35]. The following combinations can be used:

1. shunt passive and shunt active filters (parallel),

2. shunt passive and series active filter,
3. shunt passive and active filter in series,
4. series active filter with shunt active filter,
5. series active filter with shunt passive and active filter in series, and
6. shunt Passive filter and two series active filters.

Two configurations are possible for hybrid series active filter based on the position of the series filter. Series filter in the first configuration is placed on the ac side which is referred to as "unified power quality conditioner" [25]. In the second configuration, the series filter is placed on the load side which is referred to as "unified power flow controller" [36].

1.3.5 Control Strategies

The control of active power filters can be categorised into time and frequency domain methods [18, 19, 31]. These will be discussed in the following sections.

1.3.5.1 Time Domain Approaches

Time domain approaches are based on the principle of instantaneous compensation of voltage or current deviation from a sinewave [18, 37]. In this technique, the instantaneous error resulting from the deviation of voltage or current from its reference waveform is used to control the PWM voltage or current source inverters for injection of correcting component into the PCC. The active power filter reference waveform includes the harmonic components of current or voltage as well as the reactive component.

A phase locked loop (PLL) tracks the fundamental frequency component and provides a timing reference for the controls. The main advantage of time-domain techniques is the fast response to changes in the load harmonic current. The computational burden of time-domain approaches are minimal [18].

The instantaneous power transformation is a popular time-domain active power-filter control strategy [23, 38]. In this method a three-phase power system voltage, current and instantaneous power are transformed into well known α-β-0 components [39] and

the instantaneous active, reactive and harmonic powers are separated where the active power filter compensates for the instantaneous reactive power. The instantaneous reactive power is quite different in definition to conventional reactive power based on the average value concept [23].

In time domain approaches neither individual harmonics can be separately compensated nor any weighting could be applied for different harmonic components.

1.3.5.2 Predetermined Harmonic Cancellation

As in the case of tuned passive filters, predetermined harmonics can be chosen for compensation using active power filters [18, 22]. It is assumed that the load current harmonic components are stationary and known in advance. The compensating reference current waveform is synthesised from the predetermined harmonic components [40, 41]. It is possible to reduce the specific harmonic with a desired level of compensation leading to reduction in the power rating of the active power filter. The main disadvantage of this method is the high computational burden as the order of the highest harmonic to be compensated increases [41].

A PWM switching strategy for a full-bridge inverter has been proposed [42, 43] which can be used for predetermined harmonic compensation. This switching strategy can reduce the total harmonic distortion of the inverter current output while minimising the switching losses when hybrid switching sequences are employed. A detailed discussion on this PWM technique will be presented in Chapter 2.

1.3.5.3 Frequency Domain Approaches

In frequency domain approaches, the frequency components of the load current are identified using frequency analysis such as the Fourier or Wavelet transforms [44]. These frequency components are used to determine the harmonic compensation reference waveform.

The frequency domain analysis of voltage or current distortion gives the flexibility of using different configurations and circuits for each harmonic [35]. For instance, to compensate the current harmonics of an AC adjustable speed drive (ASD) passive filters

can be installed for the fifth harmonic which is the dominant harmonic component and a single active filter to compensate all the other harmonics and/or interharmonics.

The most commonly used tool for frequency domain analysis is the fast Fourier transform (FFT). The individual harmonic components in the load current are retrieved by performing a sliding FFT on the sampled load current waveform and then reproducing a compensating current waveform that has the exact harmonic components with the opposite phase angle. The main disadvantage of this technique is the high computational burden when compared to the time domain techniques.

1.4 THESIS OBJECTIVES AND OUTLINE

The objective of the work presented in this thesis is to develop control strategies that could be applied for harmonic reduction in the load and the power system. The work includes two different approaches for harmonic reduction, a new pulsewidth modulation technique and an adaptive control strategy for active power filtering. The proposed control strategy for active power filter employs adaptive online harmonic estimation together with a selective harmonic compensation scheme which is a compromise solution between fulfilling the requirements of a harmonic standard and the cost of equipment for power quality improvement.

1.4.1 Pulsewidth Modulation (PWM)

A novel PWM switching strategy using an equal area PWM (EAPWM) technique is developed which is suitable for full-bridge inverter applications. The objective of the new switching strategy is to minimise both the total harmonic distortion and low order harmonics in full-bridge inverter output. In addition, a hybrid switching sequence is developed for the proposed EAPWM technique such that further reduction in switching losses can be achieved.

1.4.2 Adaptive Active Power Filter (AAPF)

A novel control strategy suitable for a shunt active power filter is proposed. This control strategy includes on-line phase/frequency tracking, a filter bank based harmonic estimation and a selective harmonic compensation scheme. The motivation behind the

proposed control strategy is a reduction in active filter power rating while keeping the minimum requirements for harmonic reduction as specified by harmonic standards.

1.4.2.1 Harmonic Estimation

Selective harmonic cancellation requires an accurate on-line measurement of individual harmonics. This measurement should be fast and robust to transients, noise and time-varying phenomena such as variation in fundamental frequency and magnitude and the changes in the load current.

In order to retrieve individual harmonics on-line, a resonator based infinite impulse response (IIR) filter bank (FB) has been proposed. The parallel structure of this filter enables the desired harmonic order to be obtained while keeping the computational burden low. In this structure, each filter in the filter bank retrieves the specific harmonic.

To determine whether the requirements of a harmonic standard are fulfilled, the magnitude of each harmonic is compared against the recommended level. If the harmonic magnitude exceeds the recommended level or has been selected for full compensation, it will be considered in the harmonic reduction process.

1.4.2.2 Phase and Frequency Tracking

To adaptively change the parameters of the filter bank according to the time-varying parameters of the power system or compensation process, a frequency demodulation (FDM) technique for on-line tracking of the power system voltage phase and frequency has been employed. In this technique, any frequency deviation of the power system can be identified and applied for filter bank parameterisation.

The reactive power compensation for power factor correction has been incorporated into the harmonic compensation schemes. The power factor of the load is calculated using the estimated phase of the fundamental current with respect to the supply voltage phase.

1.4.2.3 Selective and Partial Harmonic Compensation Schemes

Different harmonic reduction schemes are proposed to generate the compensating reference current waveform for the active power filter. The different approaches are distinguished by how the reference current waveform is derived from the estimated

harmonic components and fundamental reactive power. The level of harmonic and reactive power compensation can be intelligently selected to meet the requirements set by harmonic standards.

A reduction in active filter power rating can be achieved by employing a selective harmonic compensation scheme. The way to use this concept is to provide only enough compensation power so that the supply harmonic current levels are within the recommended levels as set by the harmonic standards.

1.4.3 Contributions of the Thesis

A number of contributions have been made as a result of this work. A brief summary of each contribution is as follows:

1.4.3.1 New PWM Switching Strategy

A new PWM switching strategy for full-bridge inverters has been proposed which gives a lower harmonic distortion compared to conventional switching strategies [42, 43]. The performance of the proposed switching technique and three other conventional PWM switching techniques have been evaluated for synthesising sinusoidal waveforms. Application of the proposed PWM switching technique in active power filtering for predetermined harmonic cancellation has also been evaluated.

1.4.3.2 Harmonic Estimation

A resonator based IIR filter bank has been proposed for on-line power system harmonic estimation. The sliding technique for on-line measurement of the harmonic magnitude and phase is introduced for active power filter applications. Also a harmonic phase prediction technique is proposed to compensate for the phase error due to the delay in the data acquisition and processing.

Due to possible frequency variations in the power system an instantaneous phase and frequency tracking method is required. The tracking accuracy of two methods, FM demodulation and adaptive IIR filtering techniques were evaluated and subsequently the FM demodulation technique was chosen because of its preferred characteristics [45].

1.4.3.3 Adaptive Active Power Filter

A laboratory prototype of the active power filter circuit has been implemented. Software modules were developed for the proposed control strategy and were implemented on a digital signal processor (DSP).

By employing the proposed harmonic reduction schemes one is able to control the level of harmonic current compensation together with power factor correction. The proposed control strategy enables a reduction in the power rating of an active power filter by selecting specified harmonics for partial or full compensation.

1.4.4 Thesis Outline

Chapter 2 reviews the principles and software implementation of the proposed switching strategy for a full-bridge inverter along with a comparison of existing switching strategies including Natural, Uniform and Equal Sampling Techniques.

The concept of the filter bank based harmonic estimation is described in Chapter 3. An on-line frequency tracking methodology is proposed for the parameterisation of filter bank design. It includes power system voltage phase and frequency tracking. The simulation results for performance evaluation of the proposed frequency and harmonic estimation technique are presented. A comparison of the simulation results for the filter bank based harmonic estimation and the short term Fourier transforms (STFT) technique is presented.

Chapter 4 discusses issues regarding the hardware design of adaptive active power filter and software implementation of harmonic estimation and PWM techniques on the DSP board.

The experimental results of the entire system including the proposed PWM technique and its performance under different conditions are presented in Chapter 5. Experimental results for steady state and transient conditions are given to evaluate the performance of the proposed control strategy for active power filters. The results for different harmonic compensation schemes are also presented and discussed.

Chapter 6 concludes the thesis and outlines some recommendations for future research work.

CHAPTER 2.

EQUAL AREA BASED PWM TECHNIQUE

2.1 INTRODUCTION

This chapter is concerned with the development of a new pulse-width modulation (PWM) switching strategy for general inverter based applications. The proposed PWM switching strategy described herein is developed to give low harmonic voltage distortion without leading to significant switching losses.

In most pulsewidth modulation (PWM) switching environments, such as voltage source inverters (VSI), minimisation of unwanted harmonics implies a low harmonic distortion. Attempts to develop more sophisticated PWM switching strategies to obtain better (ie. minimal harmonic distortion) variable speed drive performance have recently been reported [46]. Existing PWM switching strategies have been designed to eliminate selected harmonics [47], minimise harmonic losses and reduce the harmonic distortion [48]. To generate such a PWM pattern, a set of complex equations associated with these PWM switching strategies require off-line solution [49]. On-line implementation of these switching strategies make extensive use of look-up tables (LUT) and significant off-line pre-calculation and computing resources [50].

The harmonic content of the inverter output waveform and switching losses are the principal concerns in most applications and thus the aim is to minimise the harmonic distortion and switching losses.

For medium and high power level inverters where the maximum switching frequency is restricted by switching losses, a PWM technique with a lower switching frequency is preferred. The idea is to optimise (ie minimise) both switching losses and total harmonic distortion. This Chapter is concerned with the development of a PWM switching strategy for full-bridge inverters with a low switching frequency which gives improved performance in comparison to existing switching strategies.

2.2 CONVENTIONAL PWM TECHNIQUES

2.2.1 Natural Sampling PWM Technique

The conventional PWM technique for generating the switching pattern for a full-bridge inverter is referred to as the natural sampling PWM technique [47, 51]. The PWM pattern for each leg of the inverter is determined by intersections between a triangular voltage waveform, V_{tri}, and a sinusoidal reference waveform $v_{ref}(t)$, as shown in Figure 2.1, as follows:

$$v_{ref}(t) = V_m \sin(\omega_0 t), \qquad \omega_0 = 2\pi f_0 \tag{2.1}$$

where V_m is the peak amplitude of desired output voltage $v_{ref}(t)$ and V_{tri} is the peak amplitude of the triangular waveform with a frequency of $f_{tri} = 1/T_{tri}$.

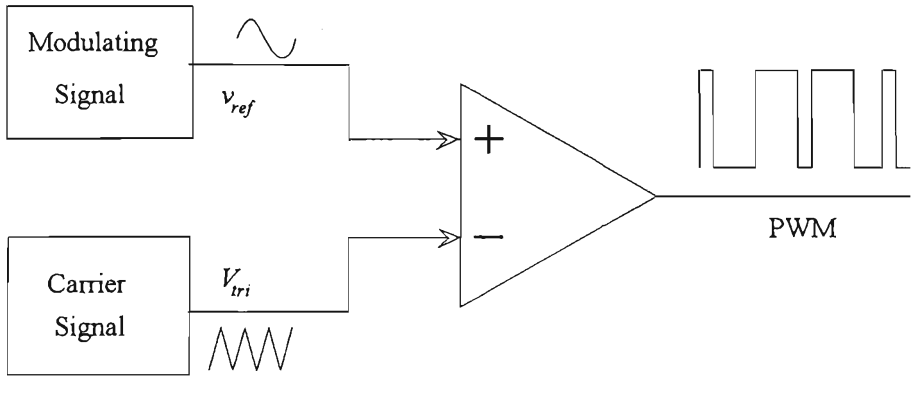


Figure 2.1: Natural PWM technique.

Figure 2.2 shows the PWM pattern for each leg of full-bridge inverter shown in Figure 2.3 for a frequency ratio p=10, and a modulation depth M = 0.8, where the frequency ratio p is defined as:

$$p = \frac{f_{tri}}{f_0} \tag{2.2}$$

where f_{tri} is the frequency of the triangular waveform and f_o is the reference waveform frequency. The modulation depth is defined as:

$$M = \frac{V_m}{V_{tri}} = modulation\ \ depth \tag{2.3}$$

The k^{th} pulsewidth (τ_{k+1}-τ_k) in the natural sampling technique is proportional to the amplitude of the modulated signal at the time of intersection which is defined by the transcendental equation [51]:

$$\tau_k = t_{k+1} - t_k = \frac{T_{tri}}{2}\left[1 + \frac{M}{2}(\sin\omega t_1 + \sin\omega t_2)\right] \tag{2.4}$$

Equation (2.4) can be solved only numerically [51]. The analog processes of natural sampling technique can be implemented on a digital platform. However it requires a large number of samples of the reference waveform and imposes extensive computational burden.

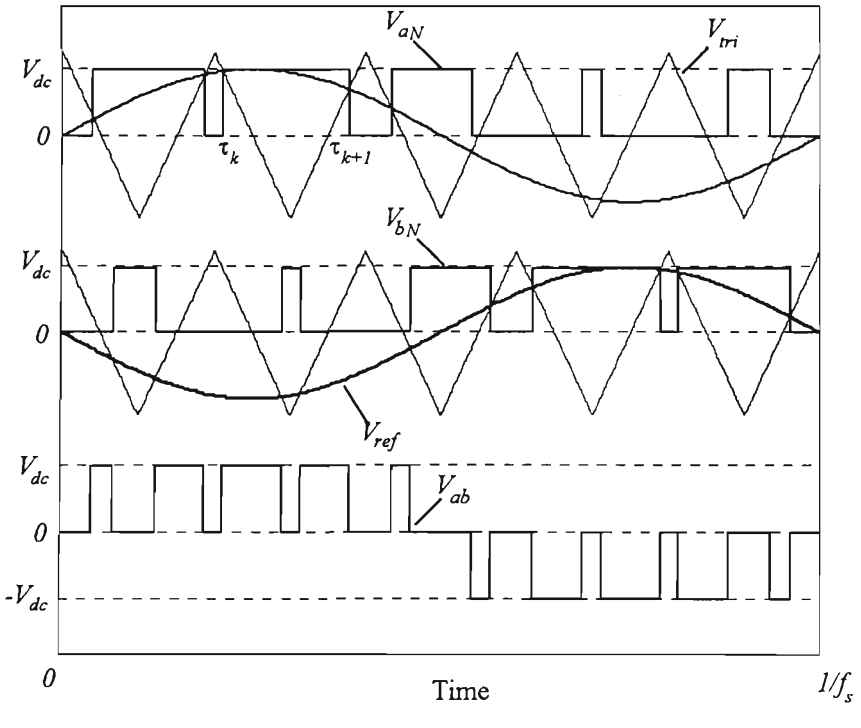


Figure 2.2: Unipolar natural sampling PWM patterns.

In the unipolar natural sampling (UPNS) PWM technique, each switching leg of the full-bridge inverter (Figure 2.3) is driven by its own PWM pattern [52]. As shown in

Figure 2.2, the reference waveform for switching of the second leg is 180° out-of-phase. Therefore, the output voltage changes between zero and $+V_{dc}$ or between zero and $-V_{dc}$ voltage levels where V_{dc} is the voltage of the DC link of the inverter.

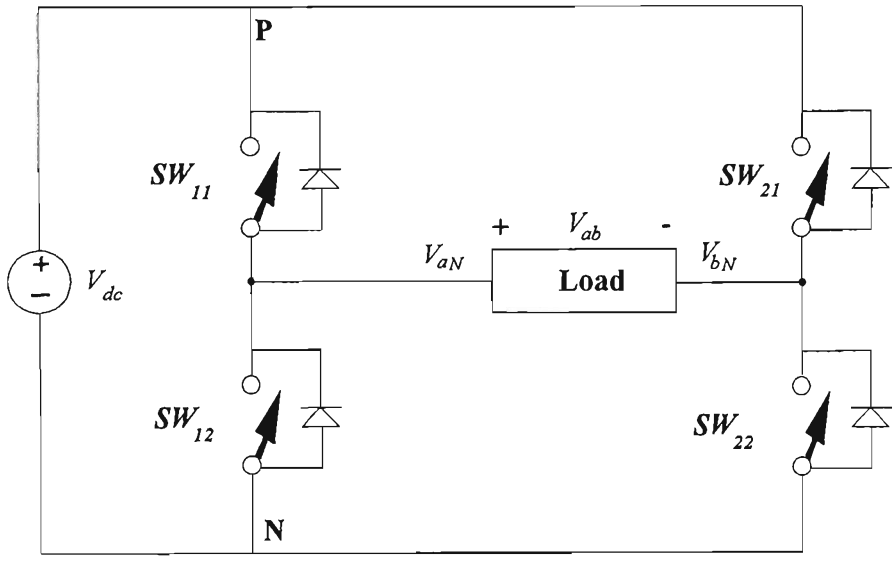


Figure 2.3: Full-bridge inverter.

2.2.2 Regular Sampling PWM Technique

Regular PWM sampling techniques, with and without third-harmonic distortion, has been adopted to reduce the harmonic distortion and facilitate implementation on a digital platform [51, 53]. Figure 2.4 shows the circuit block diagram for the regular sampling PWM technique. The reference waveform is sampled and then compared with the triangular carrier signal to generate the PWM switching pattern.

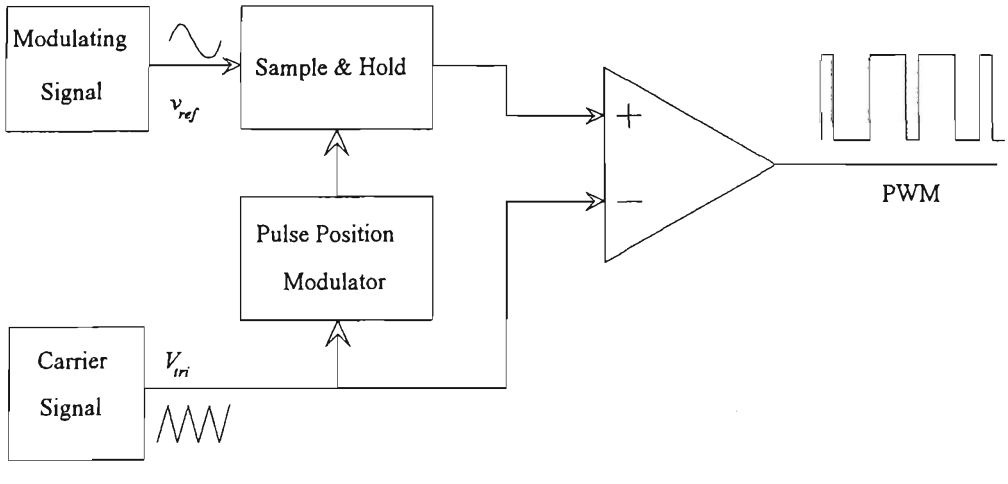


Figure 2.4: Regular sampling PWM technique.

Figure 2.5 shows the PWM pattern for unipolar regular asymmetric sampling (UPRAS) where the reference waveform is sampled at twice the carrier frequency. The k^{th} pulsewidth, τ_k, is given by:

$$\tau_k = \frac{T_{tri}}{2}\left[1 + \frac{M}{2}(\sin\omega t_k + \sin\omega t_{k+1})\right] \tag{2.5}$$

where

$$t_{k+1} = t_k + \frac{T_{tri}}{2} \tag{2.6}$$

The main advantage of this approach over the UPNS PWM technique is that the information required to be stored for on-line applications is reduced to the number of levels at the output of the sample and hold block of Figure 2.4, which is equal p [54].

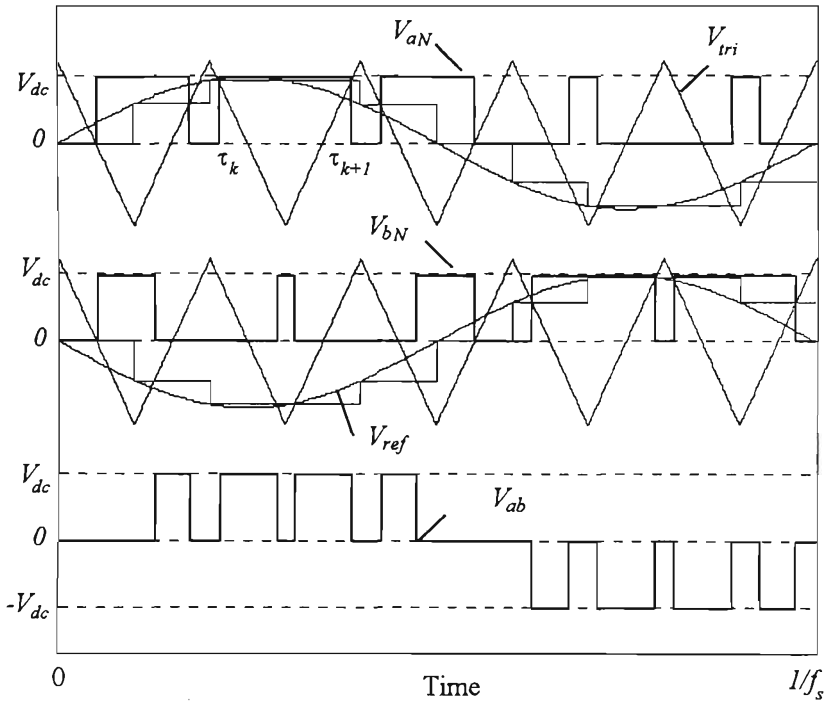


Figure 2.5: Unipolar regular asymmetric sampling PWM pattern.

2.2.3 Equal Sampling PWM Technique (EST)

The basic idea of the equal sampling technique is that the width of each PWM pulse is determined by making the area under the PWM signal equal to the area under the reference waveform [55]. As shown in Figure 2.6, the various pulse-widths of the output waveform are directly proportional to the corresponding magnitudes of the modulating waveform. The pulse-width, τ_k, for each sampling period, $T = T_{Tri}$, can be calculated as follows:

$$V_{dc} \times \tau_k = \int_{t_k}^{t_{k+1}} v_{ref}(t)dt \tag{2.7}$$

where V_{dc} is the DC link voltage. Making the area under the PWM signal equal to the area under the reference waveform using Equations (2.7), leads to the following:

$$\tau_k = \frac{V_m}{V_{dc}} \int_{t_k}^{t_{k+1}} \sin \omega t dt = \frac{M}{\omega}\left[\cos \omega t_k - \cos \omega t_{k+1}\right] \tag{2.8}$$

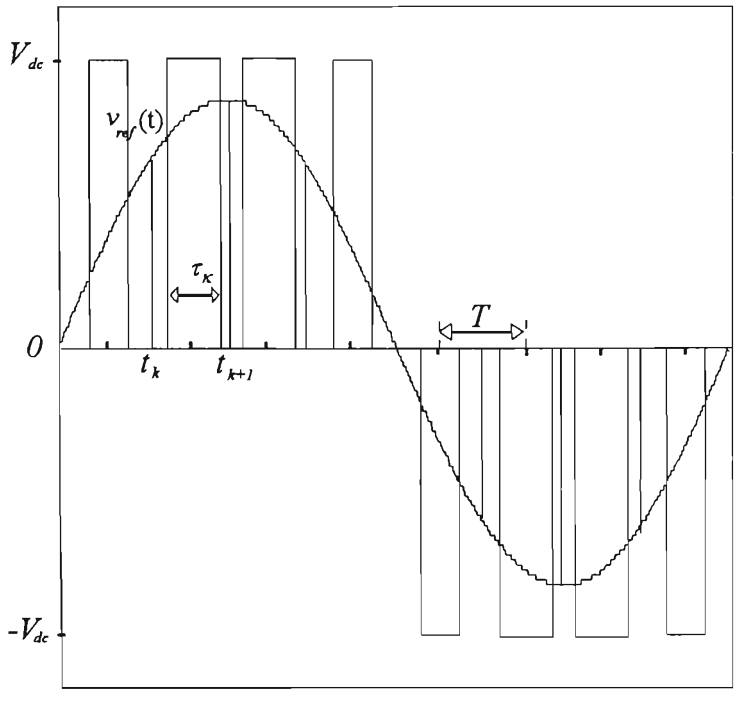


Figure 2.6: Equal sampling technique.

In this case, the pulsewidth is directly proportional to the modulation depth and the centre of each pulse is located at the centre of each sampling period. To determine the area under the reference waveform a numerical integration of the reference waveform for each sampling period is required. Furthermore, the pulse width given by Equation (2.8) can be pre-calculated off-line and stored as a look-up table for online operation.

2.2.4 Centroid Based PWM Technique (CBT)

Centroid based technique (CBT) is a new approach for the calculation of pulse position for each sampling period [40]. As shown in Figure 2.7, the width of a PWM pulse, τ_k, is determined by making the area under the PWM signal equal to the area under the reference waveform over the sampling period while the position of the PWM pulse is aligned with the centroid, $X_{centroid}$, of the sampled reference waveform over the sampling period [40].

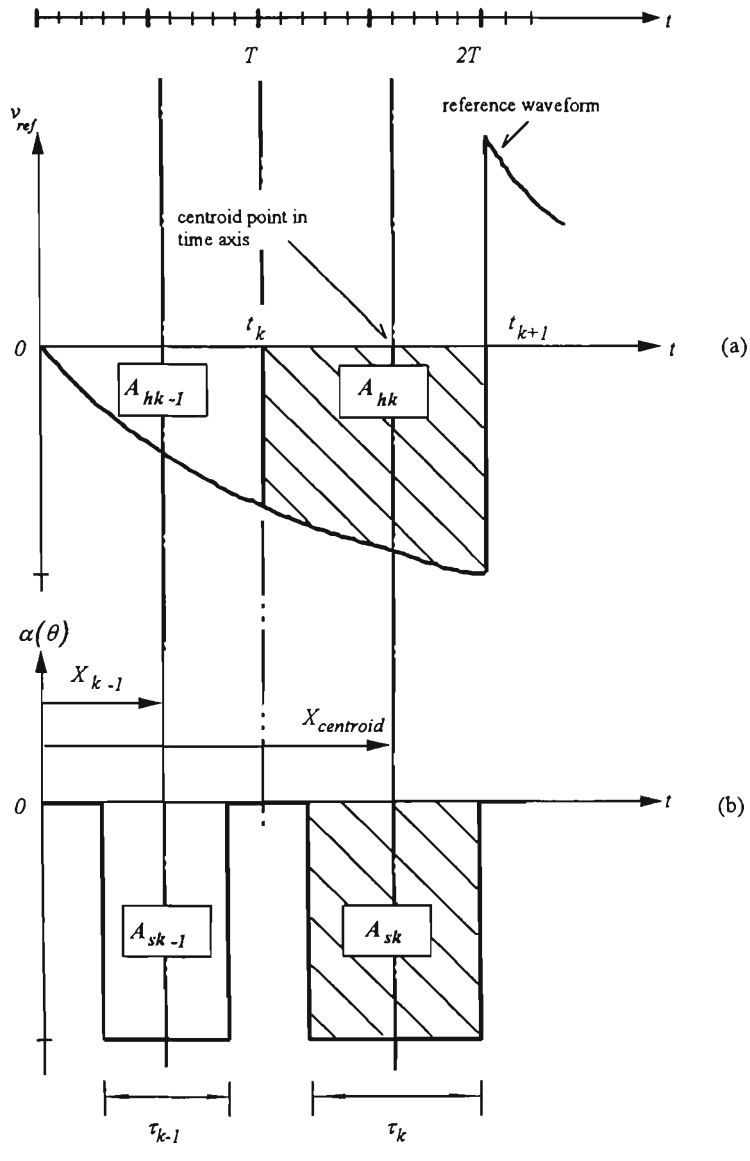


Figure 2.7: Centroid based PWM technique [40].

The pulsewidths of CBT PWM pattern is calculated using Equation (2.8). For a fixed switching frequency ratio, the pulsewidths can be stored in a LUT. The equation for calculating the time axis coordinate for the centroid of area A_{hk}, shown in Figure 2.8, is given by [56]:

$$\dot{X}_{centroid} = \frac{\int_{t_k}^{t_{k+1}} t \cdot |v_{ref}(t)| dt}{\int_{t_k}^{t_{k+1}} |v_{ref}(t)| dt} \tag{2.9}$$

Substituting Equation (2.7) in Equation (2.9) gives:

$$X_{centroid} = \frac{\int_{t_k}^{t_{k+1}} t \cdot |\sin(\omega t)| dt}{\int_{t_k}^{t_{k+1}} |\sin(\omega t)| dt} = \frac{\omega t \cos(\omega t) - \sin(\omega t)}{\omega \cos(\omega t)}\Bigg|_{t_k}^{t_{k+1}} \tag{2.10}$$

It is evident from Equation (2.10) that the pulse position $X_{centroid}$ is not a function of the magnitude of the reference waveform. For different modulation indices, only the pulsewidths should be updated whenever the modulation index changes.

2.3 Equal Area Based PWM Technique (EAPWM)

It is logical that a PWM switching strategy should produce PWM pulses which have voltage-time areas equivalent to those of the reference waveform being sampled. Further, the PWM pulses can be placed at appropriate positions of choice so that their areas are better matched with the areas under the reference waveform being sampled. On the basis of this intuitive notion, equal area PWM (EAPWM) technique has been proposed for a full-bridge inverter [42, 43]. The EAPWM is a new approach for calculating the position of each pulse at each sampling period. It aligns the time-axis centre of integration (COI) of both the PWM pulse and a corresponding area of the reference waveform to produce an optimal PWM pulse pattern.

As shown in Figure 2.8, the width of a PWM pulse is determined by making the area under the PWM signal equal to the area under the reference waveform while the position of the PWM pulse is aligned with the centre of integration, X_{COI}, of the sampled reference waveform which divides the total area under the sampled reference waveform (over a period T) into two equal areas.

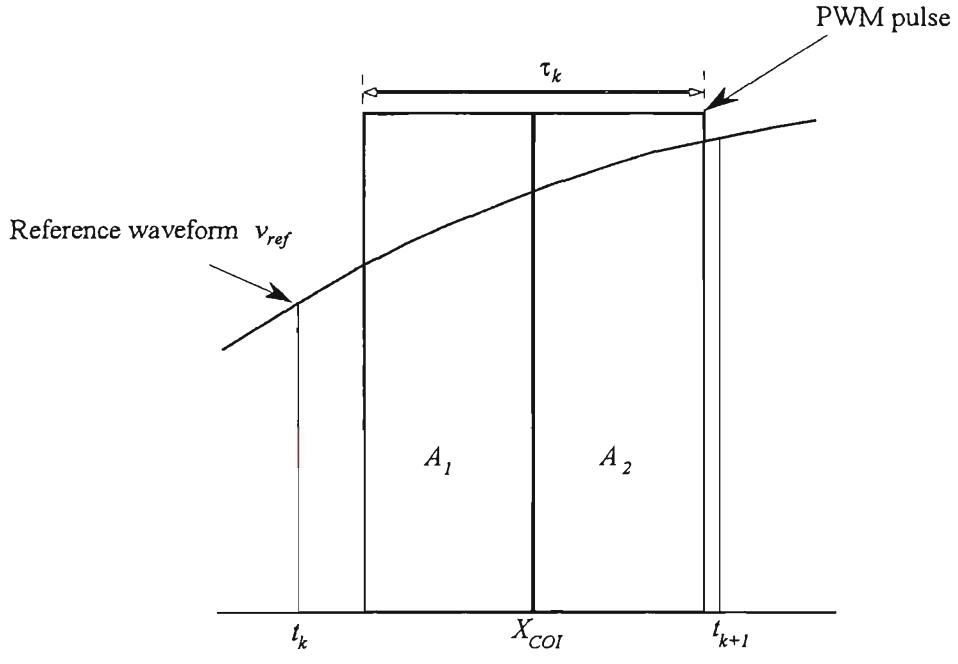


Figure 2.8: Equal area based PWM technique.

Referring to Figure 2.8, the total area under the reference waveform between t_k and t_{k+1} can be established using the integral of Equation (2.7) as follows:

$$A_\tau = \int_{t_k}^{t_{k+1}} v_{ref}(t)\,dt \tag{2.11}$$

The hatched area, $A_p = A_1 + A_2$, of the PWM pulse shown in Figure 2.8 has a width τ_k and an amplitude V_{dc}, given by:

$$A_p = V_{dc} \cdot \tau_k \tag{2.12}$$

Letting $A_p = A_\tau$ we can solve Equations (2.11) and (2.12) for τ_k:

$$\tau_k = \frac{V_m}{V_{dc}} \int_{t_k}^{t_{k+1}} \sin\omega t\,dt = \frac{M}{\omega}\left[\cos\omega t_k - \cos\omega t_{k+1}\right] \tag{2.13}$$

It is seen from Equation (2.13) that the pulse-width, τ_k, is directly proportional to the modulation depth (voltage ratio) and inversely proportional to the output frequency.

The areas under the reference waveform on both sides of the centre of integration, X_{COI}, can be considered as A_1 and A_2, as shown in Figure 2.8. Under these conditions the total area of the sinusoidal reference waveform can be calculated as:

$$\begin{aligned} A_p &= A_1 + A_2 = \frac{V_m}{\omega}[-\cos(\omega t)]_{t_k}^{t_{k+1}} \\ &= \frac{V_m}{\omega}\left(\cos(\omega t_k) - \cos(\omega t_{k+1})\right) \end{aligned} \tag{2.14}$$

where A_1 and A_2, are equal to:

$$\begin{aligned} A_1 = A_2 &= \frac{A_p}{2} \\ \frac{V_m}{\omega}[-\cos(\omega t)]_{X_{COI}}^{t_{k+1}} &= \frac{V_m}{\omega}[-\cos(\omega t)]_{t_k}^{X_{COI}} \end{aligned} \tag{2.15}$$

$$\cos(\omega X_{COI}) - \cos(\omega t_{k+1}) = \cos(\omega t_k) - \cos(\omega X_{COI}) \tag{2.16}$$

Hence, the position of the centre of the pulse can be given as:

$$X_{COI} = \frac{1}{\omega}\cos^{-1}\left(\frac{\cos(\omega t_k) + \cos(\omega t_{k+1})}{2}\right) \tag{2.17}$$

It should be noted that the position of the pulse is not a function of modulation depth. Therefore, the area and corresponding pulse position (X_{COI}) for each sampling period can be pre-calculated off-line and saved in a LUT. Since quarter-wave symmetry applies in this case we only need to store half of the pre-calculated pulsewidths and pulse positions.

2.3.1 CBT and EAPWM Comparison

In this section an example for comparison of the CBT and EAPWM techniques is presented. For a switching frequency ratio of $p=6$, the sample intervals are:

$$t_j = \left[0, \frac{\pi}{3}, \frac{2\pi}{3}, \pi, \frac{4\pi}{3}, \frac{5\pi}{3}, 2\pi\right] \quad j = 0,2,\cdots,6 \tag{2.18}$$

The pulse positions for CBT and EAPWM pulses are:

$$X_{centroid} = \left[\frac{\pi}{4.5872}, \frac{\pi}{2}, \frac{\pi}{1.2788}, 1.21180\pi, \frac{3\pi}{2}, 1.7820\pi\right] \tag{2.19}$$

$$X_{COI} = \left[\frac{\pi}{4.3468}, \frac{\pi}{2}, \frac{\pi}{1.2988}, 1.2301\pi, \frac{3\pi}{2}, 1.7699\pi\right] \tag{2.20}$$

The sampled intervals and the PWM pattern for CBT are shown in Figure 2.9.

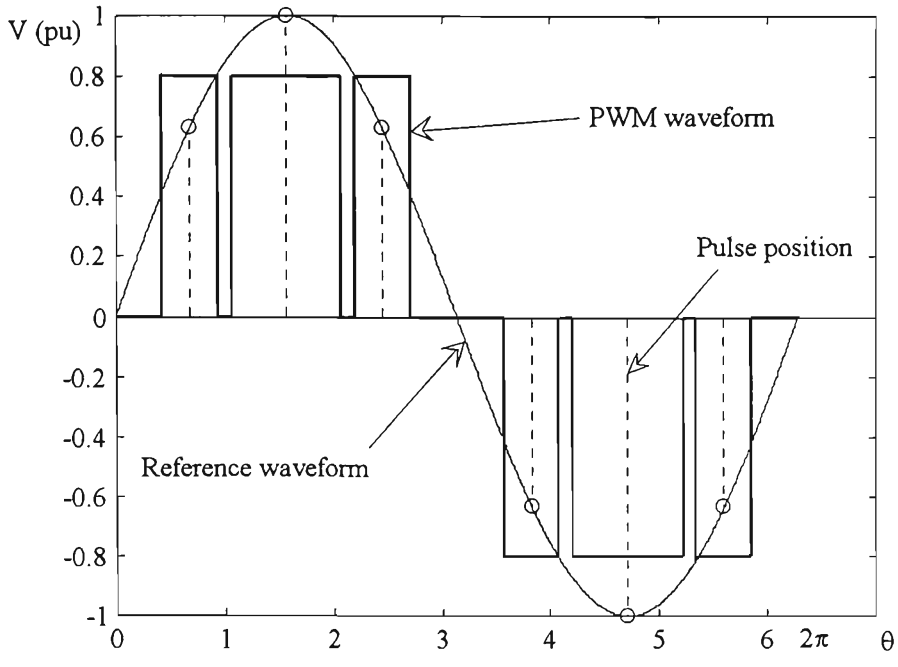


Figure 2.9: Pulse positions for CBT PWM patterns.

Figure 2.10 shows the comparison of the CBT and EAPWM patterns. From Equations (2.19) and (2.20) the difference ($e_{position}$) of the pulse position of these two methods can be defined as:

$$e_{position} = \frac{X_{centroid} - X_{COI}}{T} * 100 \qquad (2.21)$$

A maximum value of $e_{position}$ = 0.2% in this example shows that Equation (2.10) can be regarded as an approximation to Equation (2.17), especially when there is no large variation in the reference waveform during the sampling period. The performance evaluation of the proposed equal area based technique along with CBT and conventional PWM switching strategies is presented in Section 2.4.

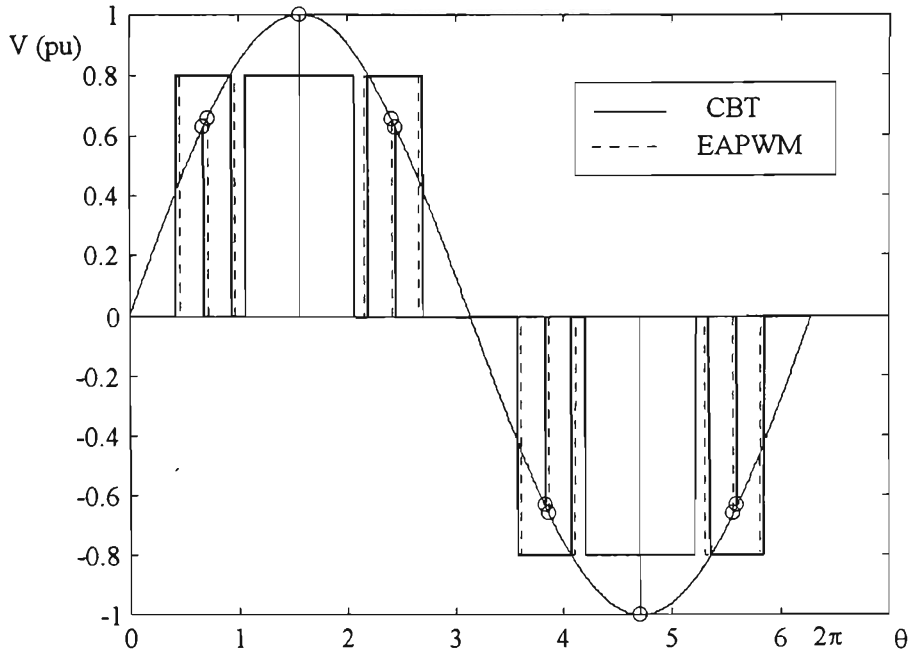


Figure 2.10: Comparison between the pulse positions of the CBT and EAPWM techniques.

2.4 SIMULATION AND PERFORMANCE ANALYSIS

2.4.1 Performance Evaluation

Usually, the performance of a PWM based inverter is evaluated on the basis of harmonic distortion and switching losses. A commonly used figure of merit to assess the performance of a voltage source inverter is the harmonic distortion factor (HDF) based on total harmonic distortion (THD) [48, 53]. The HDF for a voltage waveform is defined as:

$$HDF = \frac{\sqrt{\sum_{n=2}^{\infty}\left(V_n/n\right)^2}}{V_1} \tag{2.22}$$

where V_1 is the fundamental component and V_n represents the n^{th} harmonic component of the output waveform. The HDF, defined by Equation (2.22), is used here as a basis for the comparison of PWM switching strategies.

It should be noted that HDF is defined to reflect the actual level of harmonic distortion current in practical applications. With the assumption that the current ripple is largely determined by the inductance of the load (eg. AC motors), the harmonic distortion factor (HDF) can be used to quantify the harmonic content of the inverter output current

waveform [57]. For example, in most practical PWM inverter based applications [57] such as adjustable speed drives low pass filter characteristic of the load inductance will help attenuate the current harmonics in proportion to the inverse of the voltage harmonic order, n.

2.4.2 Simulation results

The results presented in this Section are specifically chosen to provide a comparative basis for assessing the performance of the new equal area based switching strategy. The comparison is made between natural and regular asymmetric sampling techniques, along with equal sampling and centroid based techniques. The simulation results were obtained using the MATLAB [58] software package. The same switching frequency ratio, $p=f_{tri}/f_o$ has been used for simulation of each of the switching strategies which corresponds to equal switching losses for the purpose of comparison.

Figures 2.11 and 2.12 show the harmonic distortion level for the CBT and EAPWM switching strategies for modulation depths ranging from 0.4 to 1.1 and frequency ratio ranging from 4 to 30. It is evident that the HDF reduces as the modulation frequency ratio and the modulation depth increases.

A close examination of the results depicted in Figures 2.11 and 2.12 indicates that for the low odd frequency ratios the HDF tends to be higher when compared to the adjacent even frequency ratios. The higher HDF of these frequency ratios are due to the symmetry changes of the PWM pattern form quarter-wave symmetry (for "even" frequency ratios) to half-wave symmetry (for "odd" frequency ratios).

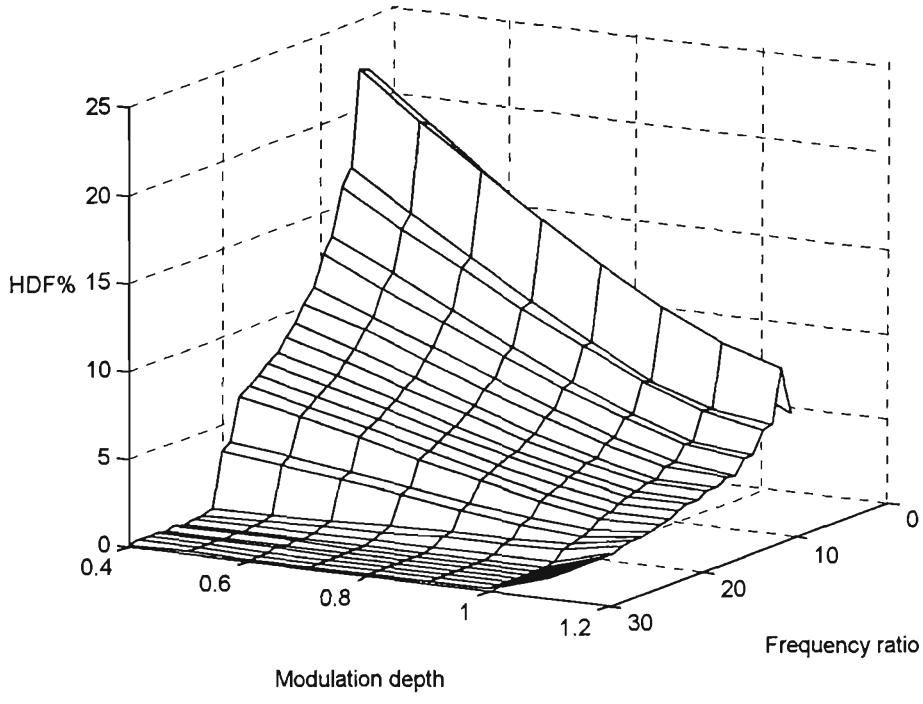


Figure 2.11: Harmonic distortion in CBT PWM technique.

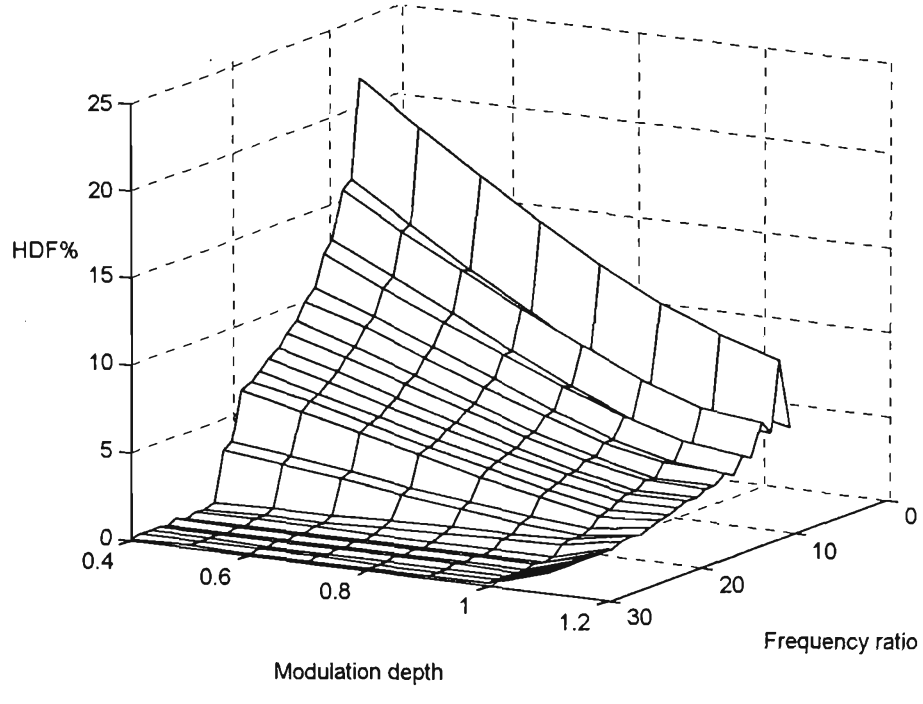


Figure 2.12: Harmonic distortion in EAPWM technique.

Figures 2.13, 2.14 and 2.15 show the variation of the harmonic distortion factor with the modulation depth and frequency ratio for the EST, unipolar natural and unipolar regular PWM switching strategies. The HDF reduces in all three cases as the frequency ratio and modulation depth increase.

The HDFs associated with the CBT and EAPWM techniques for low switching frequency ratios are similar (in magnitude of $\approx$ 25%). By comparison the EST and

unipolar natural techniques have a much higher HDF in the order of 40%. A more detailed comparison of these techniques based on HDF and fundamental voltage is presented in the next Section.

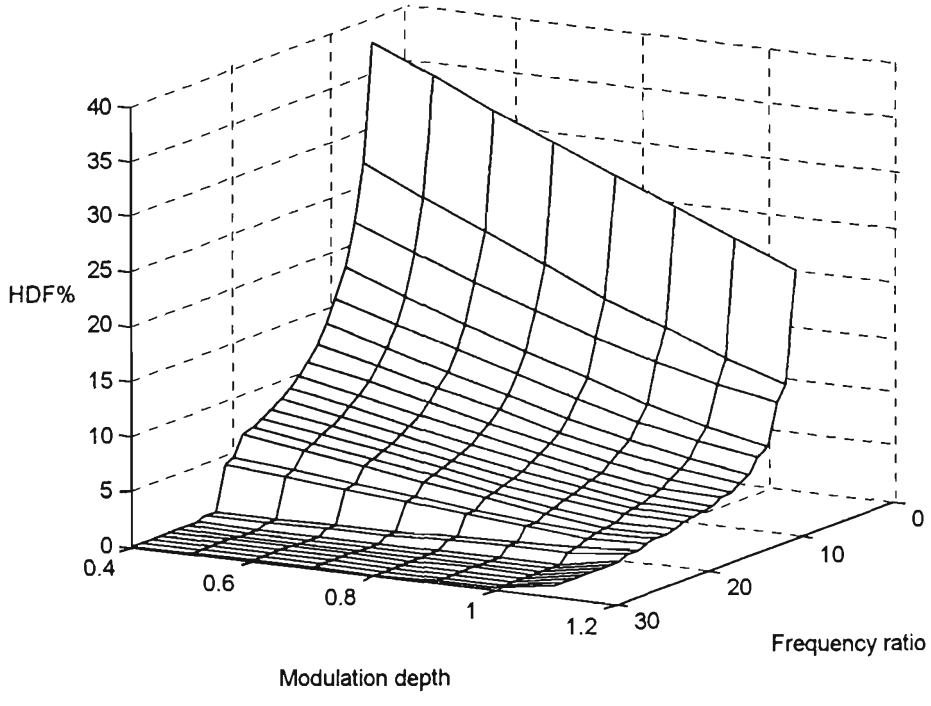


Figure 2.13: Harmonic distortion in EST PWM technique.

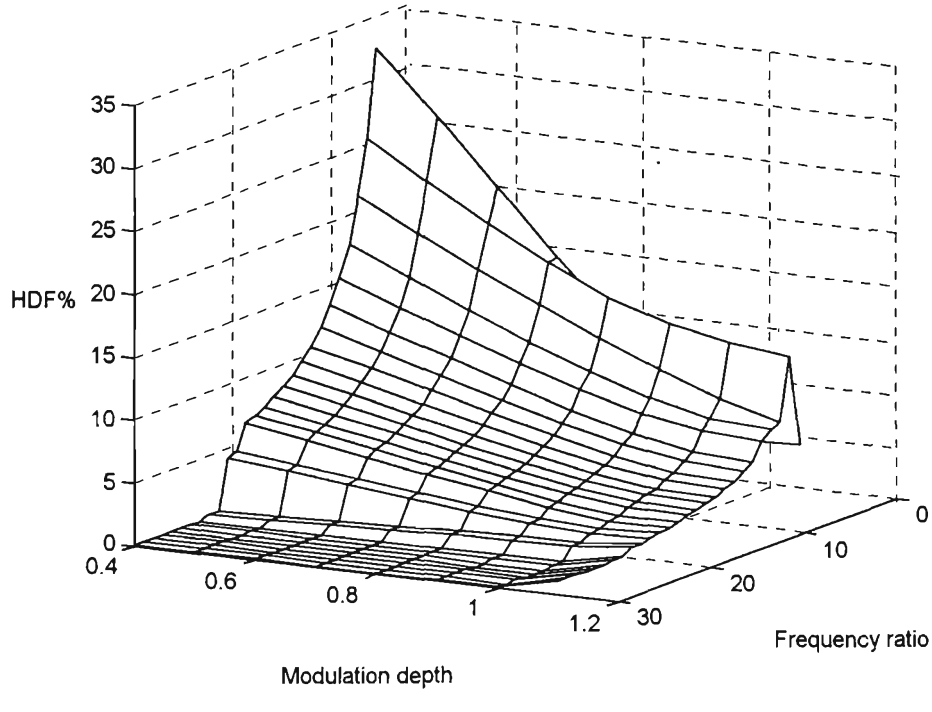


Figure 2.14: Harmonic distortion in UPNS PWM technique.

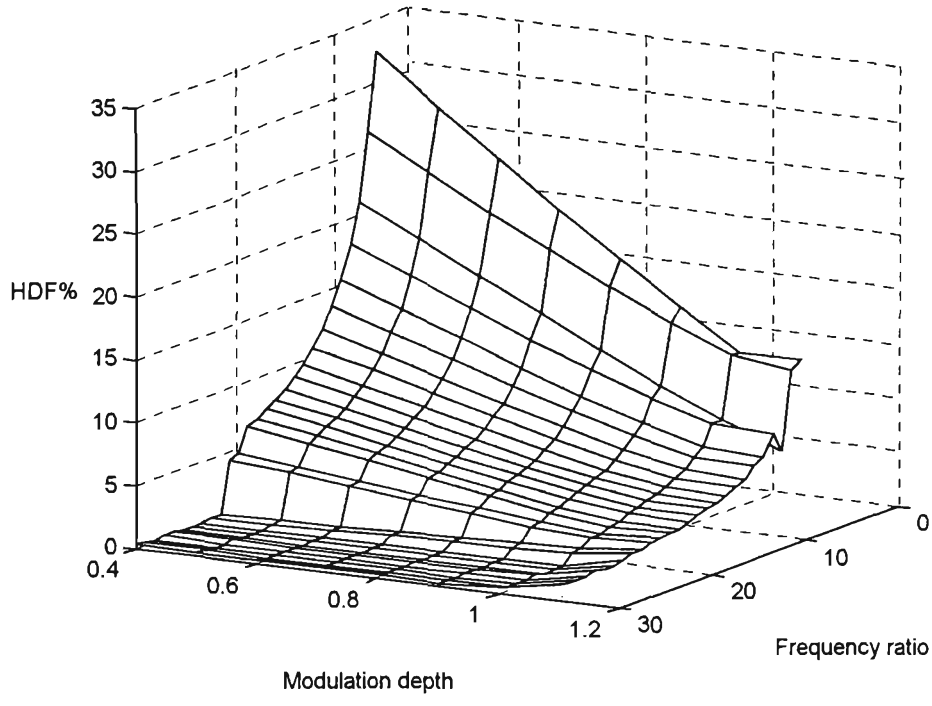
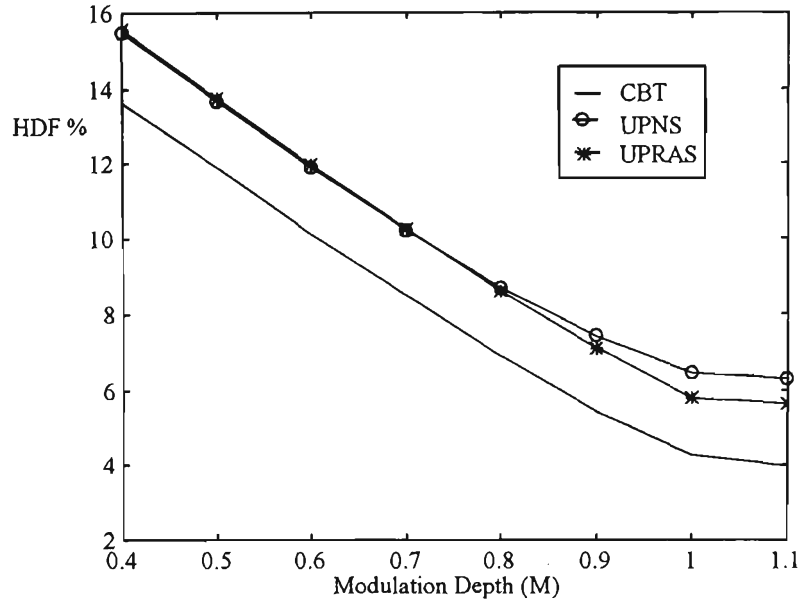


Figure 2.15: Harmonic distortion in UPRAS PWM technique.

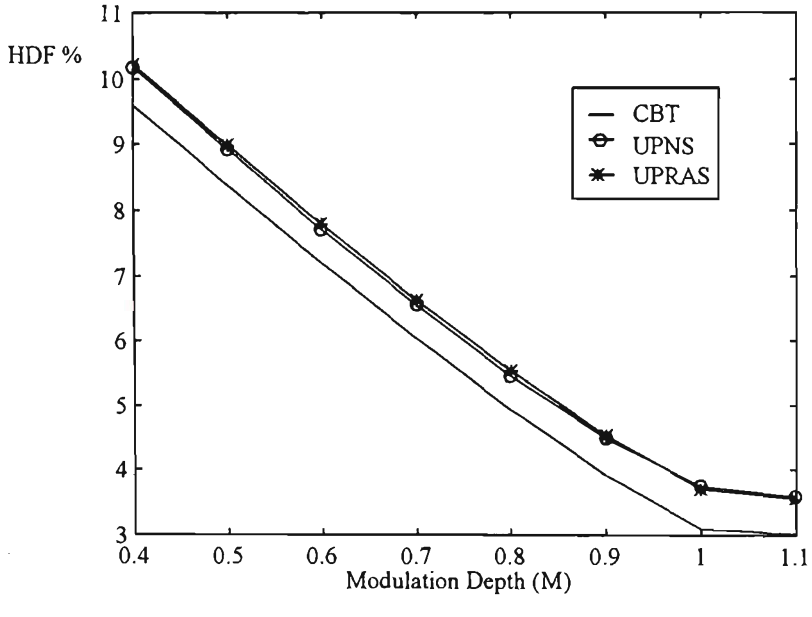
2.4.3 Comparison of CBT with Sinusoidal PWM Techniques

Figure 2.16 shows the performance comparison between the unipolar natural sampling (UPNS), unipolar regular asymmetric sampling (UPRAS) switching strategies and the centroid based (CBT) PWM techniques. As mentioned before in the case of odd frequency ratios there is half-wave symmetry for CBT and EAPWM techniques while there is quarter-wave symmetry for EST, UPNS and UPRAS techniques. Therefore, two "even" middle frequency ratios (8 and 12) from the entire range of frequency ratios (2 to 30) have been chosen for detailed comparison.

Figures 2.16 (a) and (b) show the variation of HDF as a function of modulation depth for given switching frequency ratios. It can be noted that HDF decreases as modulation depth increases. The CBT provides a significantly lower HDF over the whole range of modulation depths.



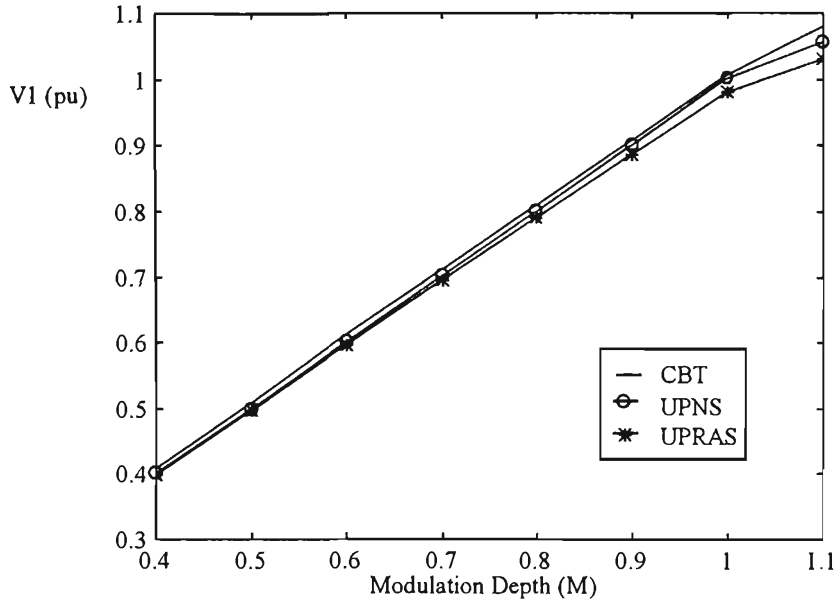
(a)



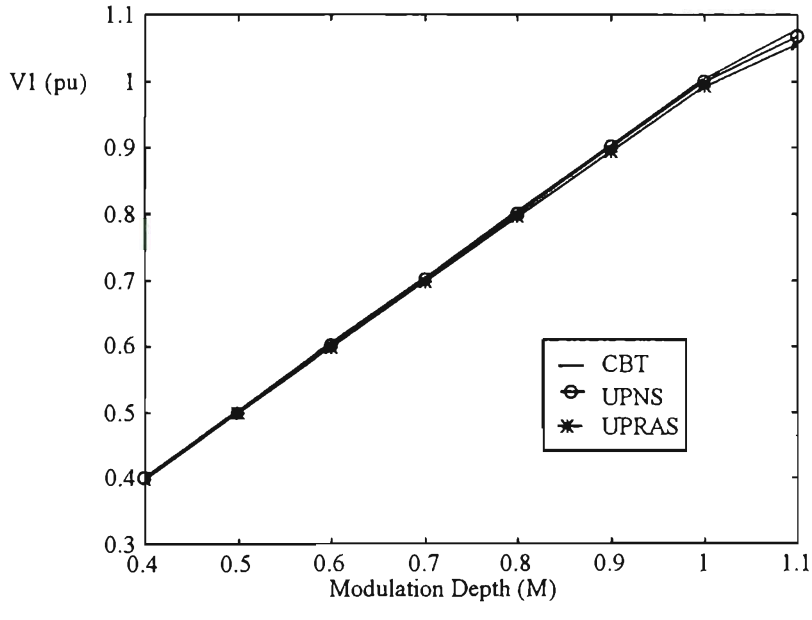
(b)

Figure 2.16: HDF vs. modulation depth for: (a) p=8, (b) p= 12.

The variation of fundamental voltage, V_1, as a function of modulation depth is shown in Figures 2.17 (a) and (b) for frequency ratios of 8 and 12 respectively. The fundamental voltage for CBT is slightly higher than for the two other methods over the entire range of modulation depths. In addition the linearity which exists between the fundamental voltage and modulation depth provides a simple means for controlling the output voltage.



(a)



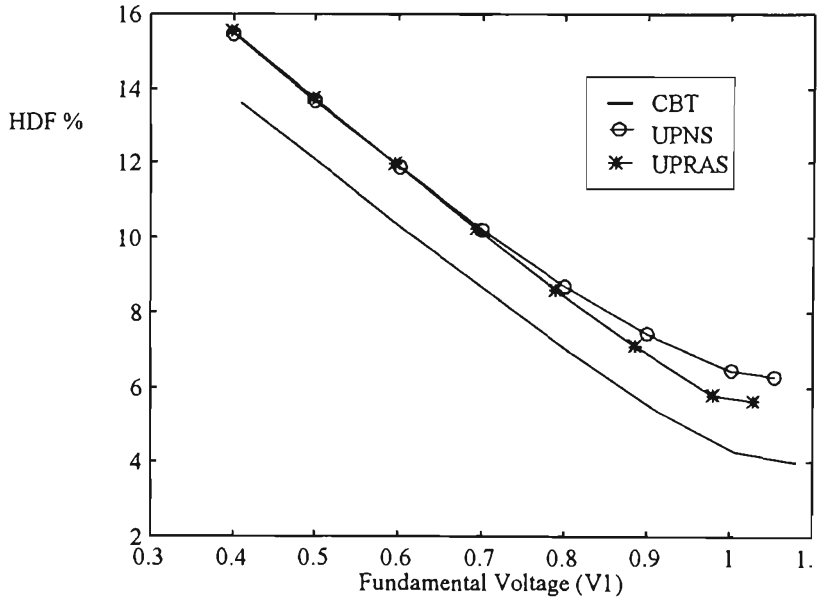
(b)

Figure 2.17: Fundamental voltage vs. modulation depth for: (a) p=8, (b) p= 12.

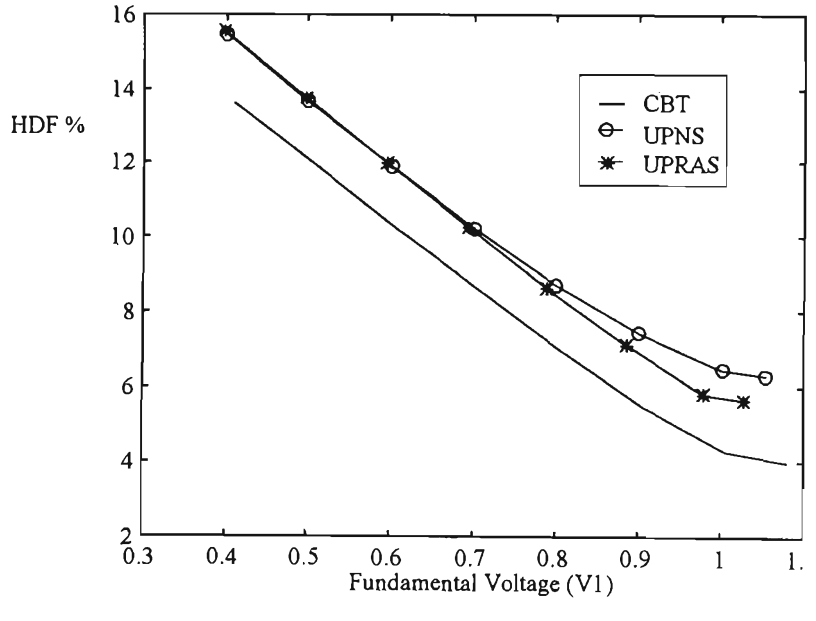
A comparison of HDF for the CBT, UPNS and UPRAS, as a function of fundamental voltage, is shown in Figure 2.18(a) and (b) for frequency ratios 8 and 12. From Figure 2.18 it is evident that the CBT produces a lower HDF over the entire range of fundamental voltage levels considered.

The ability to eliminate low order harmonics can be seen more clearly from Figure 2.19 which compares the harmonic content in the output voltage of the CBT with UPNS and UPRAS which are sinusoidal modulating techniques. Figures 2.19 (a-c) indicate that the low order harmonics up to the 9^{th} are negligible. Further, the 9^{th} harmonic of the CBT is 50% lower than that of the UPRAS. Indeed, as illustrated by these figures, the largest

voltage harmonic of the CBT is the 11^{th}, whereas, in the cases of UPNS and UPRAS the most significant lowest order harmonic is the 9^{th}, which reaches approximately 40% and 50% of the fundamental, respectively. Also the 7^{th} harmonic in the CBT is less than 3% while in the UPRAS and UPNS it is 12% and 20% of the fundamental, respectively. Clearly, at low switching frequencies, the CBT PWM technique provides better performance in harmonic elimination over the sinusoidally modulated PWM techniques.



(a)



(b)

Figure 2.18: HDF vs fundamental voltage for: (a) p=8, (b) p= 12.

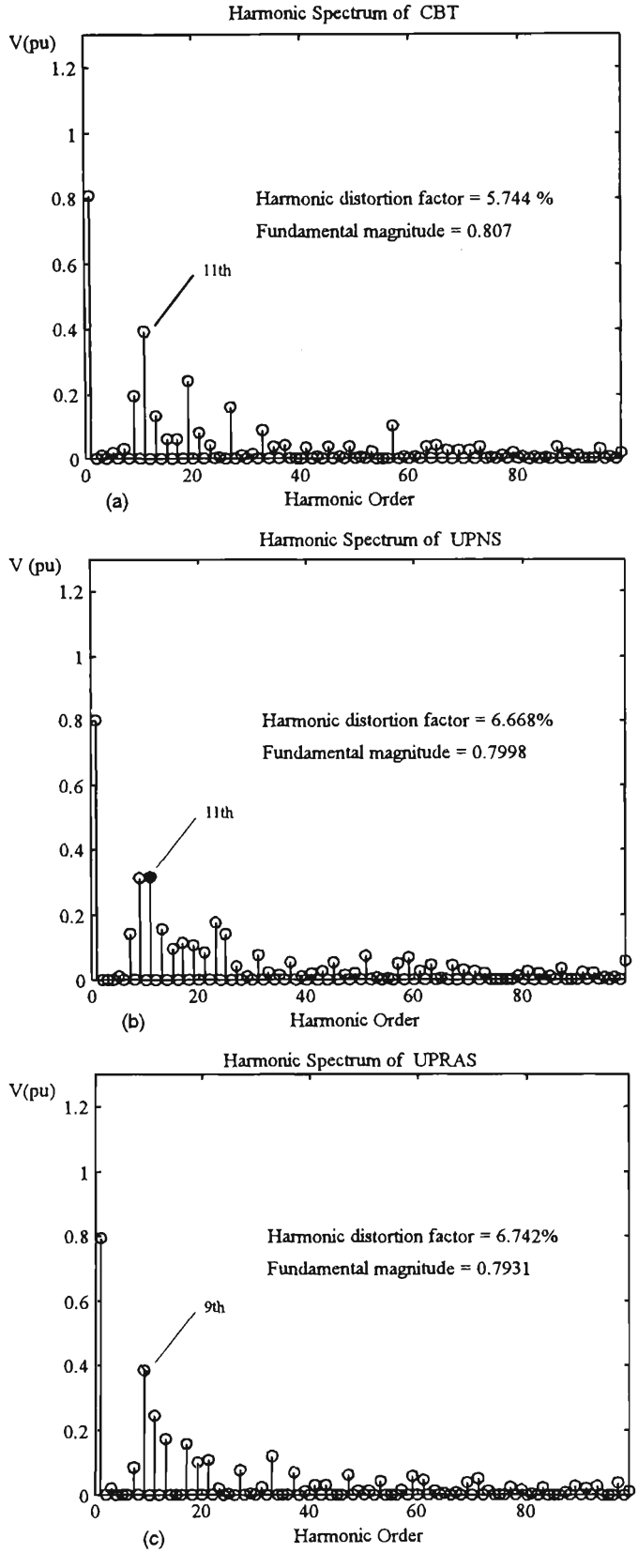


Figure 2.19: Harmonic spectrum: switching frequency ratio 10, modulation depth 0.8:

(a) Centroid based technique(CBT),

(b) Unipolar natural sampling technique (UPNS),

(c) Regular asymmetric sampling technique.(UPRAS).

2.4.4 Comparison of CBT and EAPWM

A comparison of the harmonic spectra for CBT, EAPWM and EST PWM techniques, for a frequency ratio of 10 and modulation depth of 0.8 is given in Figure 2.20. Low order harmonics below the 9^{th} are almost zero while the 9^{th} harmonic is the first harmonic of the centroid based switching strategy which is significantly smaller than in the EST technique. Figure 2.20 (a) indicates that the CBT and EAPWM are very effective in suppressing the low order harmonics.

From the frequency spectra, illustrated in Figures 2.20 (a-c), the magnitudes of the low order harmonics in EAPWM and CBT are significantly lower than for EST. This result is to be expected, since, in both the equal area based PWM technique (EAPWM) and the centroid based (CBT) switching strategies, the PWM pulses are placed at appropriate positions so that their areas are better matched with the areas under the reference waveform being sampled. However, the slight difference in pulse position calculation in CBT and EAPWM are reflected in the elimination of the low order harmonics and the HDF minimisation. The CBT and EAPWM are capable of eliminating the low order harmonics up to $n= p\pm 1$, while keeping the HDF at a lower value in comparison with other methods.

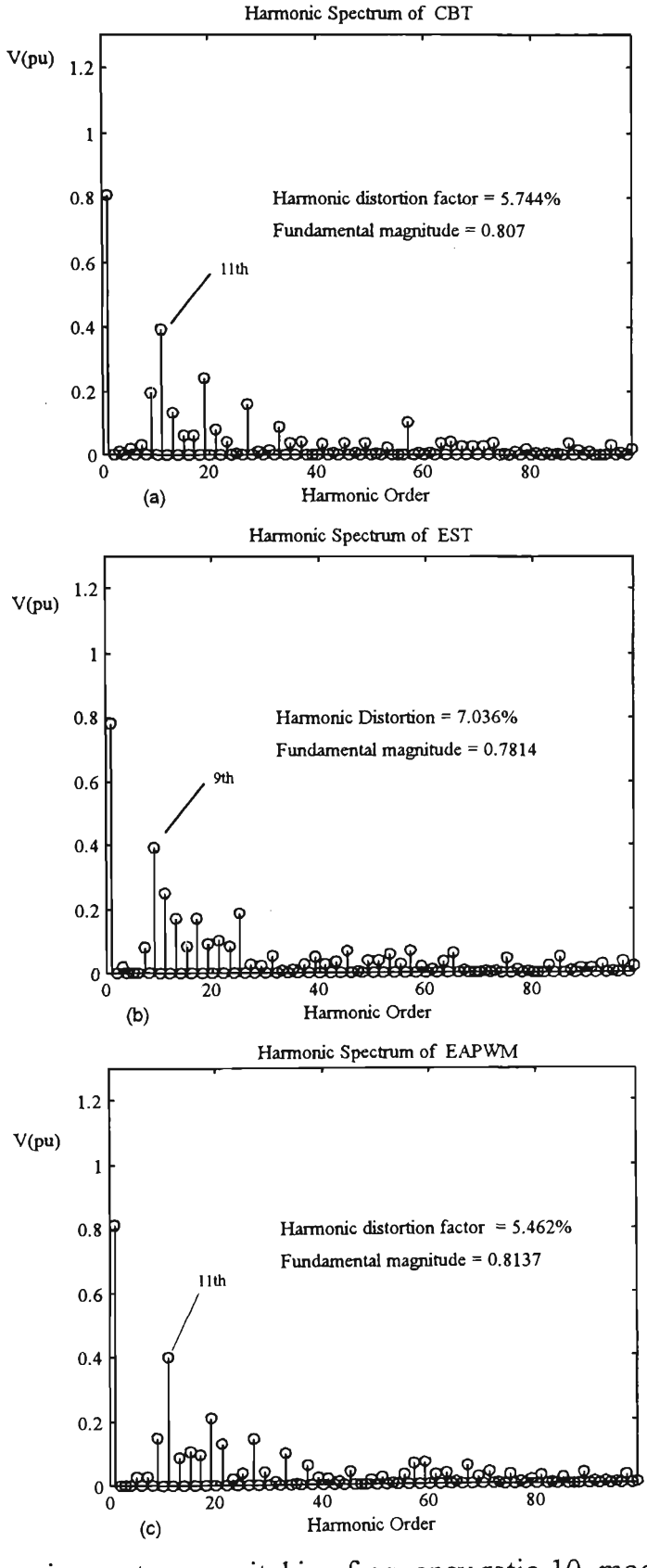


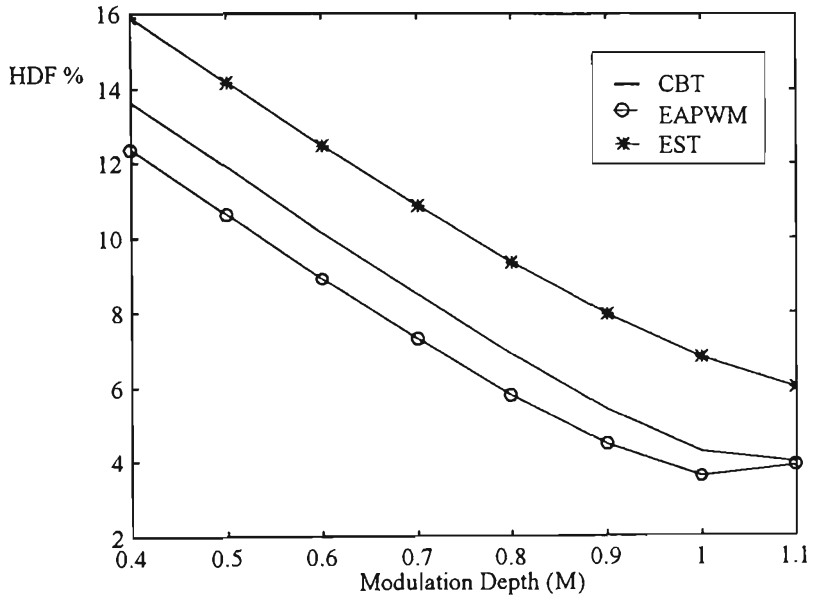
Figure 2.20: Harmonic spectrum: switching frequency ratio 10, modulation depth 0.8:

(a) Centroid based technique (CBT),

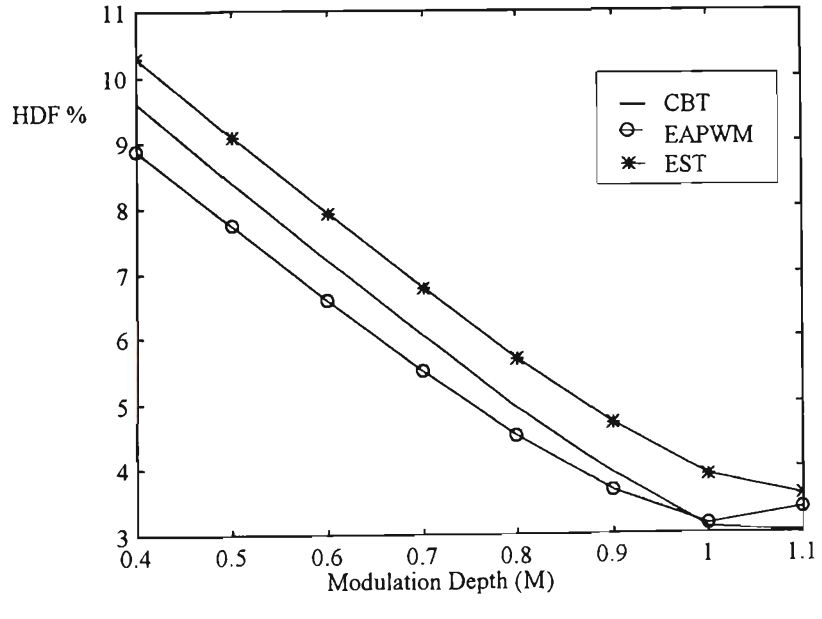
(b) Equal sampling technique (EST),

(c) Equal area based PWM technique (EAPWM).

Comparison of the harmonic distortion and fundamental voltage for the CBT, EST and EAPWM for various modulation depths are illustrated in Figures 2.21 and 2.22. As shown the HDF for CBT is smaller when compared to HDF of EST. However, the HDF for EAPWM over most of the modulation depths is lower when compared with the CBT and EST. Furthermore, the fundamental voltage is also higher over the entire range of modulation depths. As a consequence, the variation of HDF versus fundamental voltage, shown in Figure 2.23, is significantly lower for EAPWM when compared to CBT and EST.

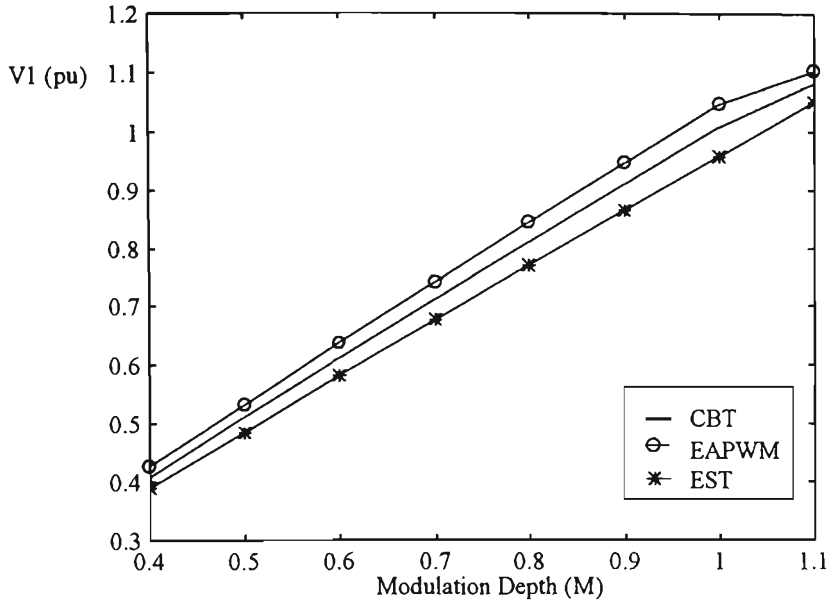


(a)

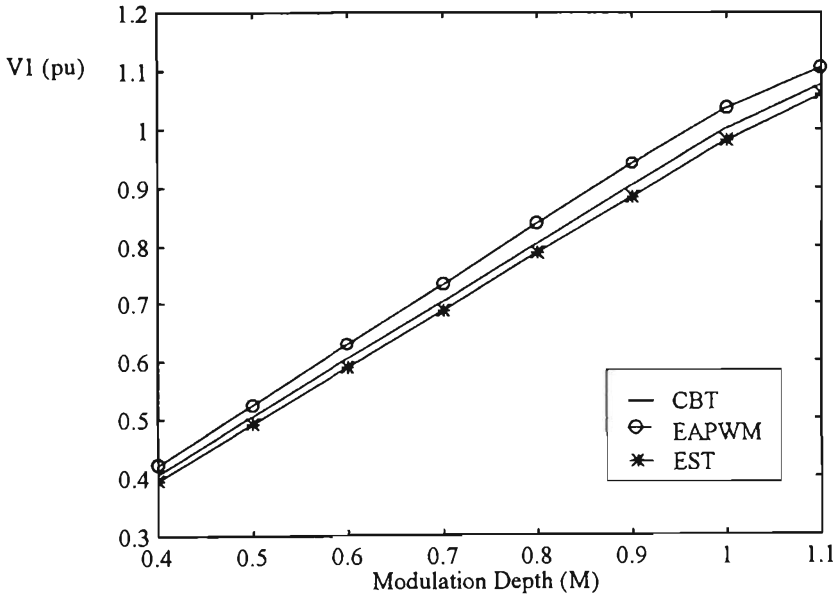


(b)

Figure 2.21: HDF vs. modulation depth for: (a) p= 8, (b) p = 12.

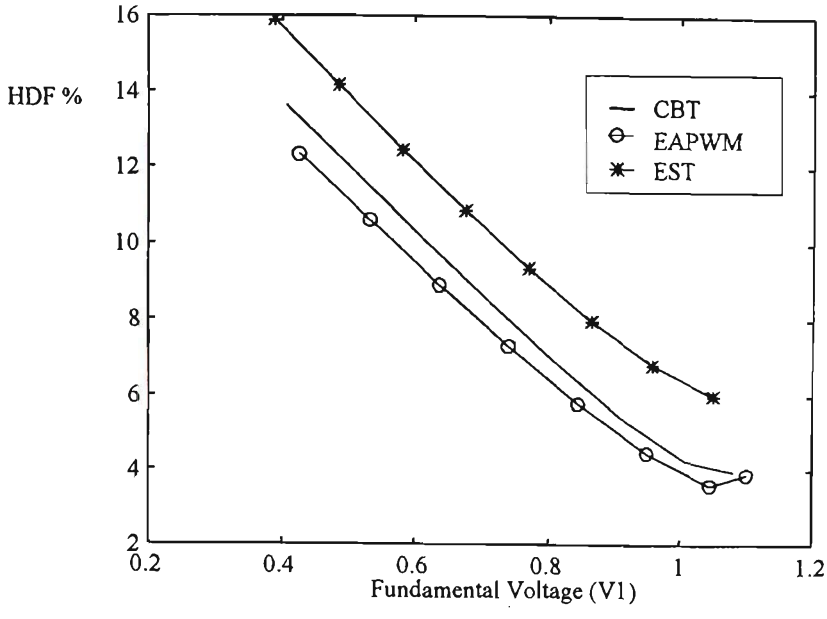


(a)

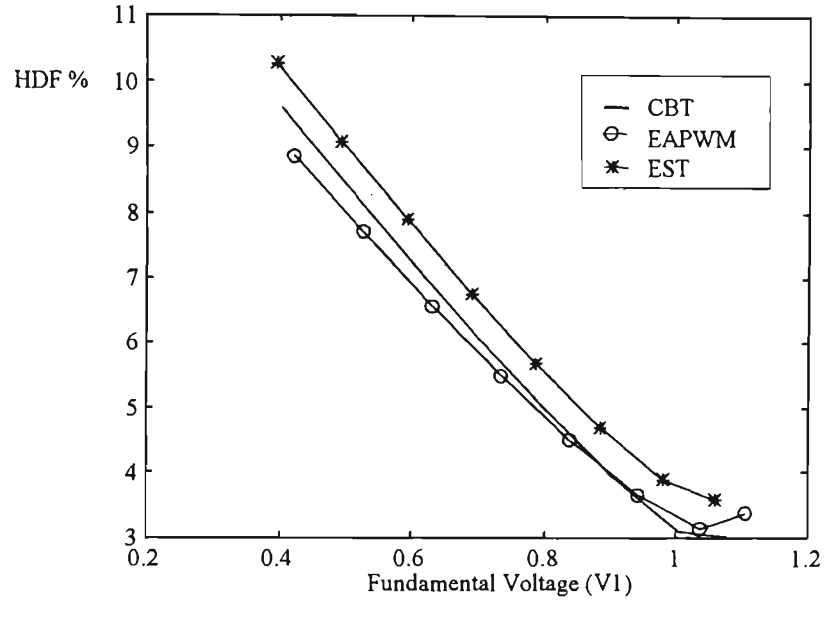


(b)

Figure 2.22: Fundamental voltage vs. modulation depth for: (a) p= 8, (b) p =12



(a)



(b)

Figure 2.23: HDF vs fundamental voltage for : (a) p= 8, (b) p = 12.

2.4.5 Predetermined Harmonic Cancellation

Application of the proposed equal area based PWM technique (EAPWM) for active power filters is presented in this Section [43]. In order to show the effectiveness of this PWM switching strategy for predetermined harmonic cancellation a quasi square load current waveform has been considered for the purpose of harmonic reduction. Figure 2.24 shows the actual load current, i_{load} , the desired supply current, i_s, and the reference current waveforms for an active power filter, i_{ref}.

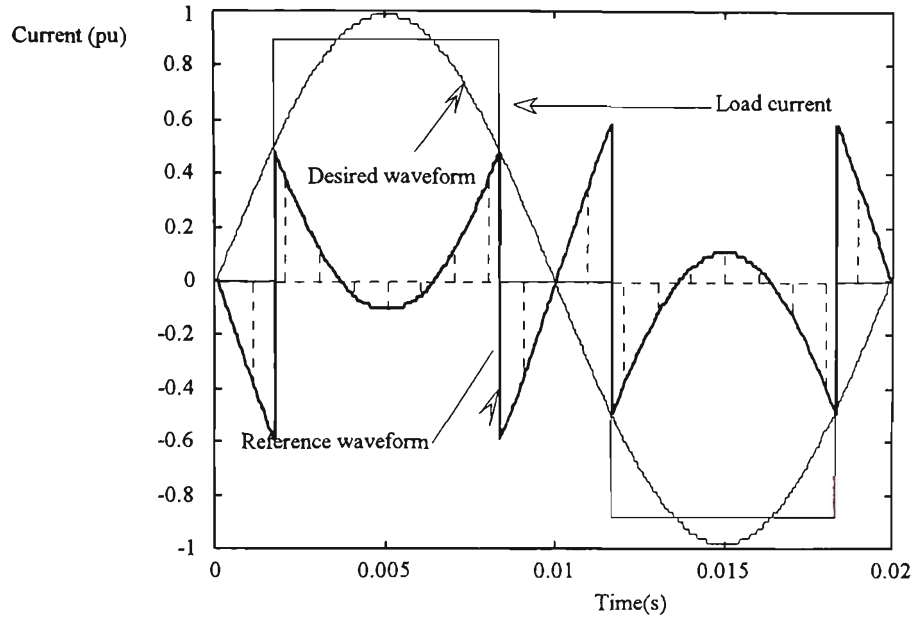


Figure 2.24: Current waveforms for predetermined harmonic cancellation.

Figure 2.25 shows the reference current waveform and PWM switching patterns generated for EAPWM, CBT and UPNS switching strategies.. The frequency spectrum of the active power filter reference current (i_{ref}) waveform is given in Figure 2.26 which shows the presence of low order odd harmonics in the load current. The level of cancellation and the parameters of active power filter determine the number of pulses per cycle in the PWM switching pattern. In this case the number of pulses per cycle of 50 Hz is chosen to be 20 which implies a switching frequency of 1000 Hz. The harmonic distortion factor for the load current calculated up to 24th harmonic is 4.63 %.

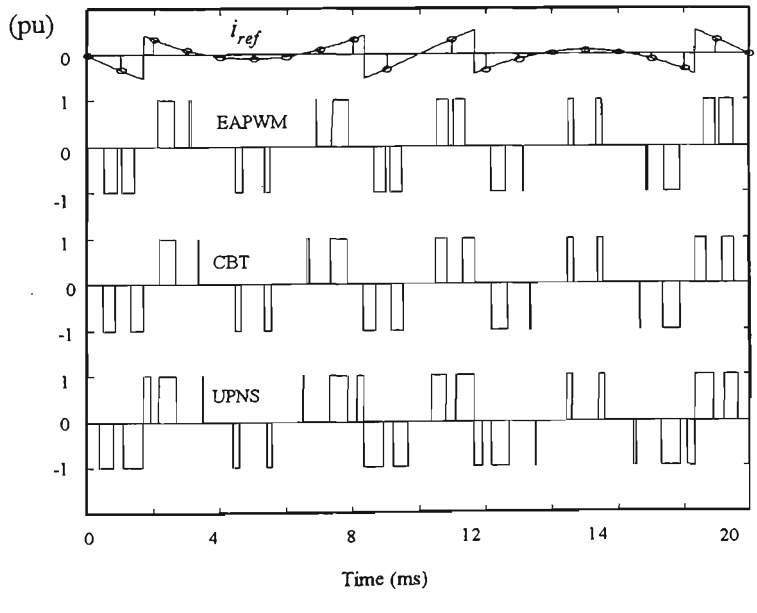


Figure 2.25: PWM pattern generated using: EAPWM , CBT and UPNS techniques.

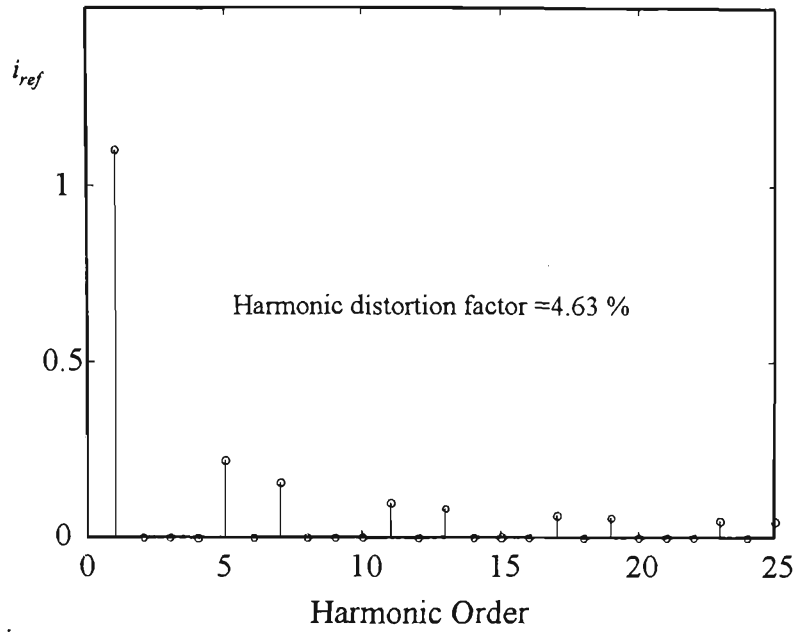
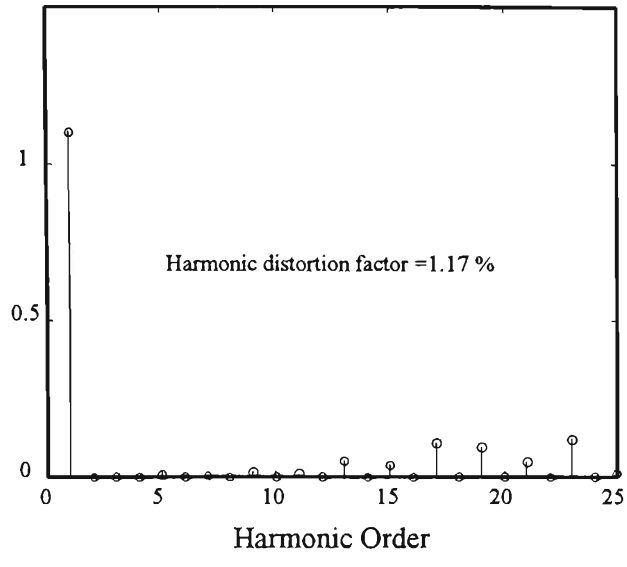


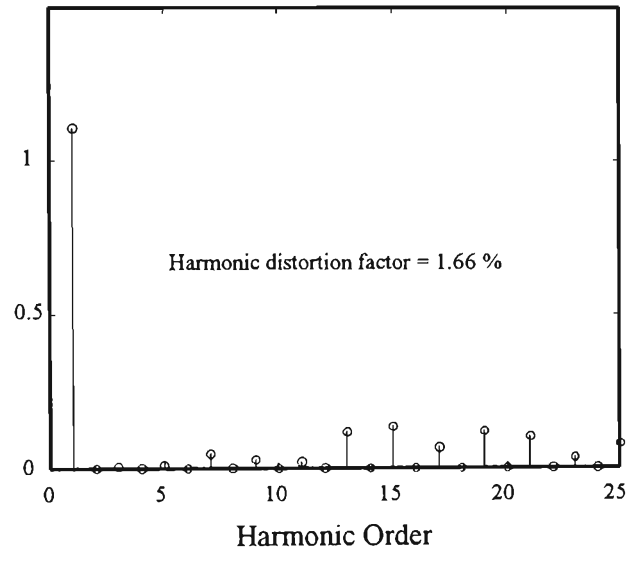
Figure 2.26: Harmonic spectrum of the load current waveform.

In order to compare the performance of the EAPWM technique for predetermined harmonic cancellation, the active power filter reference current waveform (i_{ref}) has been modulated using the unipolar natural (UPNS) and centroid based (CBT) PWM techniques. Figures 2.27 (a-c) show the harmonic spectra of the source current ($i_{ref} + i_{load}$) after compensation using EAPWM, CBT and UPNS techniques.

The HDF for EAPWM, CBT and UPNS calculated up to harmonic order of 24 are 1.17%, 1.66%, 1.22% respectively. This is clear that the EAPWM technique produces a lower HDF for low order harmonic when is compared to CBT and UPNS techniques.



(a)



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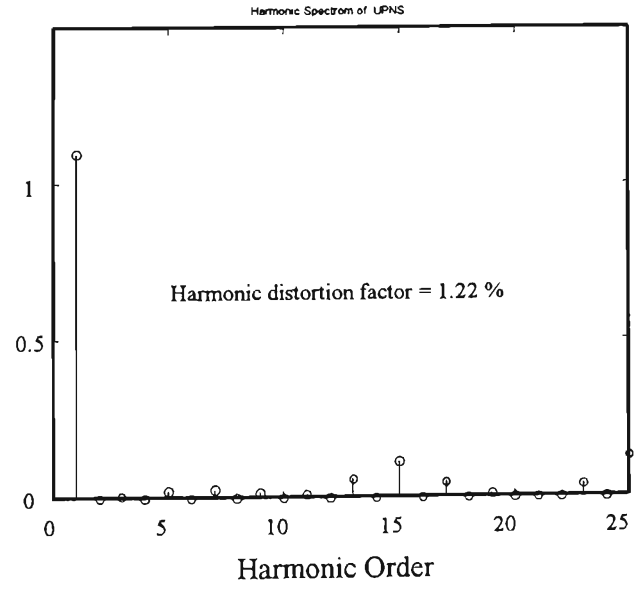


(c)

Figure 2.27: Frequency spectrum of the source current after compensation: (a) EAPWM, (b) CBT and (c) UPNS.

2.5 SWITCHING SEQUENCE

A switching sequence has been proposed to reduce the switching losses for the full-bridge inverter, shown in Figure 2.3. The circuit of Figure 2.3 consists of two switching legs, SW_{11}/SW_{12} and SW_{21}/SW_{22}. There are 16 different possible combinations of switching. Only four of these combinations are useful for obtaining the PWM pattern across the inverter output. The four useful states of the inverter are as shown in Table 2.1.

Table 2.1: The switching combinations.

Conducting Switches	Output voltage V_o
SW_{11}, SW_{22}	$+V_{dc}$
SW_{12}, SW_{21}	$-V_{dc}$
SW_{11}, SW_{12}	0
SW_{12}, SW_{22}	0

In the proposed switching sequence, two out of the four switches of the inverter are operated at the output frequency, f_o (low frequency), and the other two are switched according to the PWM pattern (high frequency). One way to have positive and zero voltage across the inverter output is to turn on SW_{22} when the PWM switching pattern, V_{PWM} is positive, and by turning on SW_{21} when V_{PWM} is negative (refer to Figure 2.28). Thus SW_{21} and SW_{22} are switched at the reference frequency, f_o, which is generally low. The switching sequence of these two slow switches, SW_{21} and SW_{22}, are:

$$\begin{aligned} SW_{22} &= 1 \quad when\ V_{pwm} > 0 \\ SW_{22} &= 0 \quad when\ V_{pwm} < 0 \\ SW_{21} &= 1 - SW_{22} \end{aligned} \tag{2.23}$$

To generate the PWM pulse pattern across the inverter output, only SW_{11} and SW_{12} should be driven by the proposed switching strategy as follows:

$$\begin{aligned} SW_{11} &= 1 \quad when\ (SW_{22} = 1\ V_{PWM} > 0) \\ SW_{11} &= 0 \quad when\ (V_{PWM} = 0) \\ SW_{12} &= 1 - SW_{11} \end{aligned} \tag{2.24}$$

Switches SW_{21} and SW_{22} can be classified as "*slow*" switches and SW_{11} and SW_{12} can be classified as *"fast"* switches.

Power switches with a lower switching speeds can be used for switches SW_{21} and SW_{22} [59]. Thus the number of fast switches can be reduced from 4 to 2 in a full-bridge inverter reducing the total switching losses.

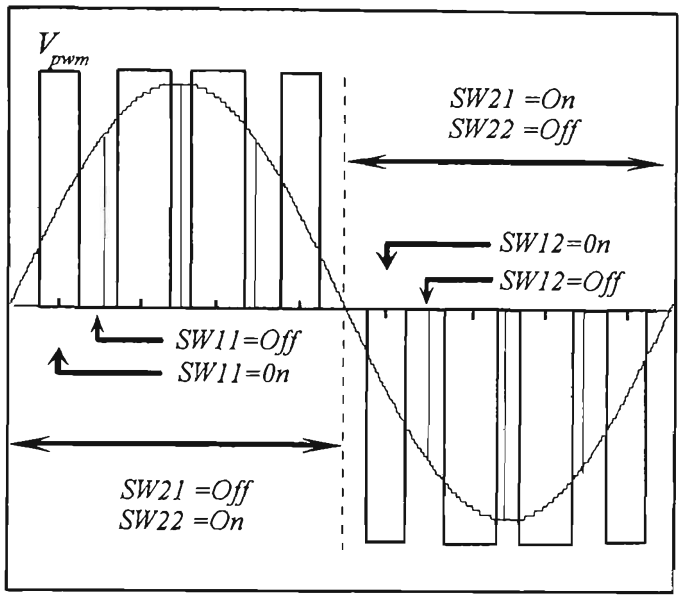


Figure 2.28: Proposed switching sequence.

2.6 CONCLUSIONS

This Chapter presented a novel equal area based PWM switching strategy (EAPWM) which is essentially a non-uniform PWM technique where the centres of the PWM pulses are aligned with the centre of integration (COI) of the corresponding areas of the reference waveform. The simulation results indicate that the equal area based PWM technique is capable of generating an inverter output waveform having reduced low order harmonic content. In particular, it has been shown that EAPWM yields a notable improvement in terms of minimal HDF while producing a higher fundamental voltage magnitude than for conventional techniques at low switching frequency ratios.

The EAPWM switching strategy has considerable practical use for AC variable-speed motor drive applications where harmonics at the output of the inverter pose serious problems to the drive performance. Furthermore, application of the proposed switching strategy and switching sequences in the active power filter can further reduce the switching losses while minimising the harmonic distortion.

CHAPTER 3.

HARMONIC ESTIMATION

3.1 INTRODUCTION

Nonlinear loads in power systems are often dynamic in nature such that the frequency and amplitude of the load current components vary continuously with time and load conditions [60]. These nonlinear load currents flowing through the power system impedances lead to voltage distortion. To mitigate the effects of distortions in power systems an accurate and adaptive measurement technique is required. An adaptive algorithm is proposed to track and estimate the time varying magnitudes and phase angles of load current harmonics. The proposed algorithm simultaneously determines the power system fundamental frequency.

The proposed harmonic estimation process is illustrated in Figure 3.1. It consists of a phase and frequency tracking technique and a parallel filter bank which performs the harmonic estimation. The fundamental power system frequency, f_o, and phase, ϕ_o, are tracked by a phase and frequency estimator. The estimated frequency is then used by a resonator based parallel filter bank (RBFB) to estimate individual harmonic components, $I_1, \ldots I_N$, of the input signal, $i(n)$. The phase and magnitude of each harmonic, filtered out by filter bank, can be calculated using a sliding measurement algorithm [61]. The calculated magnitude of each harmonic is used to find the active power filter reference waveform, i_{ref}, for harmonic reduction and/or reactive power compensation.

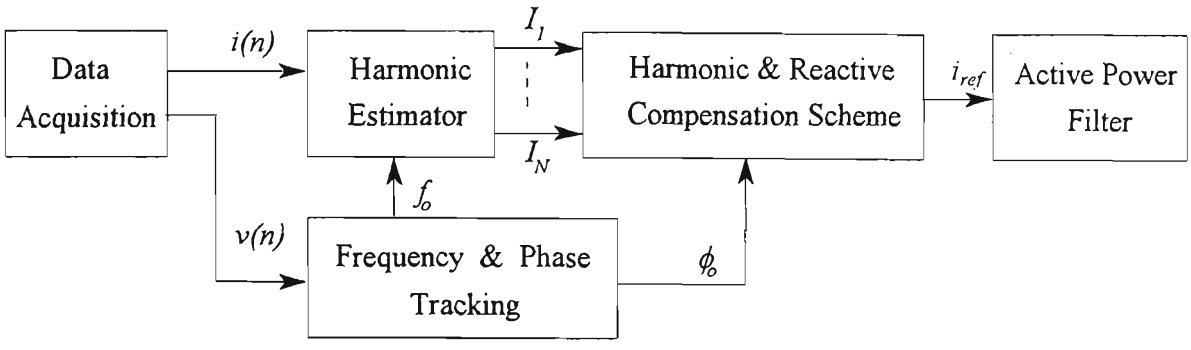


Figure 3.1: Proposed harmonic estimation technique for active power filtering.

This Chapter is organised as follows: Section 3.2 discusses the short term Fourier transform (STFT) which is the most widely used technique for harmonic estimation. Section 3.3 discusses the theory of the frequency tracking techniques considered such as; FM demodulation and adaptive infinite impulse response (IIR) filtering. Section 3.4 presents a resonator based filter bank (RBFB) structure and sliding harmonic measurement [61]. The performance evaluation of the proposed structure is carried out in Section 3.6. The simulation results are presented to illustrate the performance of the frequency tracking techniques described in Sections 3.4 for a non-stationary power system fundamental frequency. The simulation results obtained for FM demodulation technique are discussed and compared with adaptive IIR filtering results. The simulation results for proposed filter bank based sliding measurement technique are compared with those obtained by a short term Fourier transform estimation technique.

3.2 HARMONIC ESTIMATION

As mentioned in Chapter 1, harmonic measurement techniques are classified into off-line and on-line approaches. For off-line measurement of non-stationary signals such as power system voltage and current waveforms, Fourier transform (FT) based techniques have been used [62].

Other techniques such as a artificial neural network (ANN) [63] based estimator, maximum likelihood [64], Kalman filtering [65] and combination of different methods [66] have been reported. However, majority of the harmonic estimation techniques as reported in the literature are based on the Fourier transform [60, 62, 67].

3.2.1 Fourier Transform

In this case a signal is represented in the Fourier transform frequency domain as a summation of weighted orthogonal sine and cosine functions. The weights are referred to as Fourier coefficients. Transformation of data from frequency domain to time domain is done using the Inverse Fourier Transform (IFT).

In practical situations, the discrete Fourier transform (DFT) is used to estimate the Fourier transform of a real signal from a finite number of sampled points. The properties of a continuous Fourier transform are the same as those for the Discrete Fourier Transform. The DFT is defined as:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi kn}{N}} \tag{3.1}$$

where *x(n)* is a sequence obtained by sampling the continuous time signal *x(t)*. The magnitude and phase of *X(k)* are the magnitude and phase of the corresponding frequency components in the frequency domain.

With an *N* sampled data sequence DFT produces an *N* point frequency response, each of these points in the frequency response is called a frequency bin. Depending on the number of points in the sampled data, as well as the sampling frequency, each frequency component of the signal should contribute only to one single frequency of the Fourier transform (frequency bin). More the number of samples, the closer the bins lie together and higher the sampling frequency further apart the bins are.

In order to obtain an accurate DFT result several important assumptions should be considered. These are:

1. the signal should be quasi stationary,
2. the frequency of sampling should be greater than twice the highest harmonic frequency in the signal to be analysed,
3. the sampling frequency should be an integer multiple of the fundamental frequency.

When the above requirements are not satisfied, three of the major problems associated with the use of DFT occurs which are: aliasing, leakage and picket-fence [40, 60, 66, 68, 69]. A brief discussion on these pitfalls is given as follow:

Aliasing occurs when the sampling frequency is not chosen high enough above the highest frequency of interest in the signal ($f_s \geq 2f_{max}$) which consequently causes high frequency components to be folded into low frequency area in frequency domain. To avoid aliasing, the input signal should be band limited to frequencies below one-half the desired sampling rate by low pass filtering (anti-aliasing filter) the continuous signal prior to digital sampling [70].

The "leakage" occurs due to the truncation of the signal in the time-domain such that a fraction of a cycle exists in the waveform instead of complete periods. The DFT assumes that the input signal is periodic. If the input sequence does finish on a whole number of periods a discontinuity occurs and consequently the frequency resulting from the DFT leaks into adjacent frequency bins instead of placing them at the correct frequency bins.

The "picket-fence" effect is referred to the accuracy of the magnitude of each harmonic in DFT results. Since the DFT is discrete only those frequencies that are placed exactly on the discrete points in the frequency domain (f_s/N where N is the size of DFT) are represented accurately by DFT. The resulting frequency spectrum can be considered as the continuous spectrum viewed through a picket fence.

3.2.2 Short Term Fourier Transform

The short term Fourier transform (STFT) is used to evaluate the way the frequency content changes with time. When the input signal is not a stationary signal, ie with time-varying frequency and magnitude, then a short time moving window is required to capture the time-frequency variation of the signal and its frequency components. The STFT is illustrated in Figure 3.2. The input signal $x(n)$ is subdivided into sections, where each section is analysed for its frequency content separately. A variety of windowing techniques can be used to minimise the blocking effects which may arise due to sharp transitions between successive blocks of data [71]. The STFT is defined as:

$$STFT[k,m] = \sum_{n} x[n]W[n-m]e^{-j\frac{2\pi kn}{N}} \tag{3.2}$$

where $W(n-m)$ is the window function.

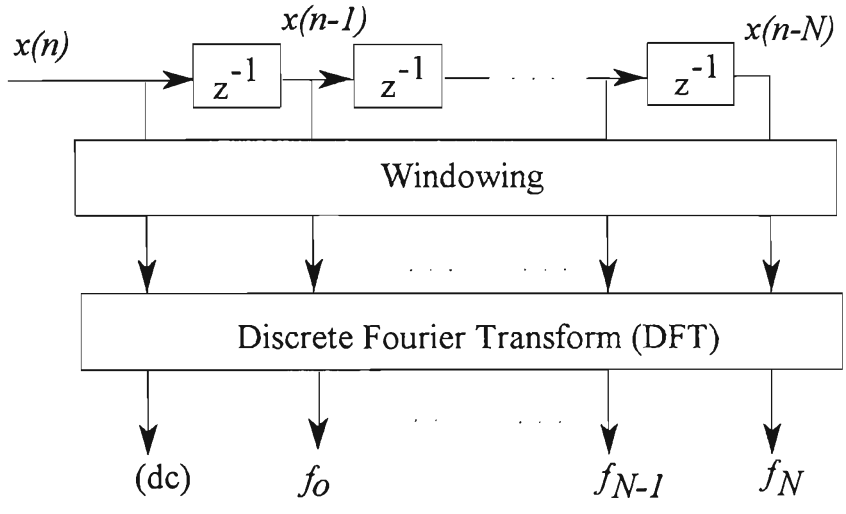


Figure 3.2: Short term Fourier transform.

The frequency resolution for the Fourier transform is given by:

$$f_{resolution} = \frac{f_s}{2N} \tag{3.3}$$

where N is the number of samples in the window and f_s is the sampling frequency. It is clear from Equation (3.3) that the frequency resolution can be increased by increasing the number of data samples. Larger data blocks result in increased computational burden and longer processing delays. As an example, consider the situation where a frequency resolution of 1 Hz is desired while the sampling frequency is 3200Hz. In this case, N is equal to 1600 which means that the block of data contains 32 full cycles of the fundamental frequency. It is clear that this would not be satisfactory for online real-time applications.

3.3 Filter Bank Based Harmonic Measurement

As an alternative to Fourier transform methods, filter bank harmonic estimation technique can provide high resolution in time and frequency [72]. An adaptive frequency estimator is proposed (Figure 3.3) to estimate the fundamental frequency. The estimated fundamental frequency (f_o) is used to adapt the parameters of filter bank which provides the separated harmonic components.

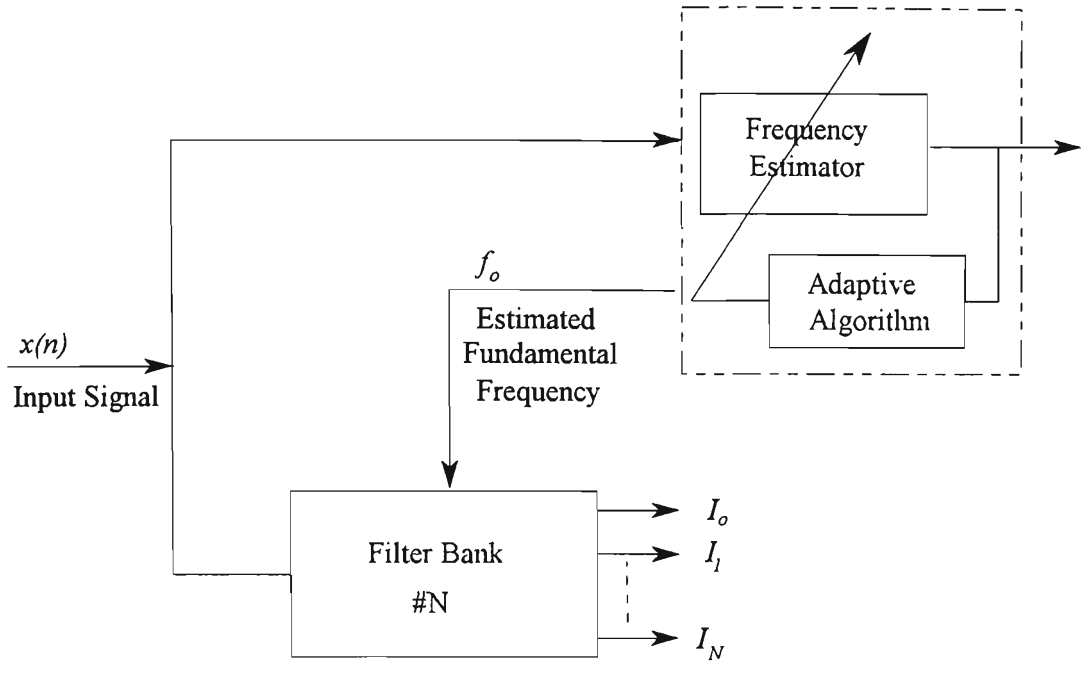


Figure 3.3: Filter bank based sliding measurement of power system harmonics.

3.3.1 Filter bank Structure

The structure of the proposed filter bank based harmonic estimation scheme is shown in Figure 3.4. The filter bank consists of parallel digital resonators with a common feedback loop referred to as a resonator based filter bank [72-74]. The transfer function from the input signal, *x(n)*, to the residual error signal, *e(n)*, is equivalent to an IIR band pass filter whose zero transmission frequencies are at ω_k for $k=1, \ldots, N$. Also, the transfer function from the input to the output of each filter is exactly unity at the resonant frequency of the corresponding resonator and zero at the frequencies of all the other resonators [72, 74]. For the proposed filter bank structure illustrated in Figure 3.4, the transfer function of each resonator is given by [72]:

$$H_R^k(z) = \frac{2z^{-1}\left(a_k - z^{-1}\right)}{1 - 2a_k z^{-1} + z^{-2}} \tag{3.4}$$

where $a_k=cos(\omega_k)$ and ω_k is equal to the k^{th} harmonic angular frequency. The transfer function from the input, *x(n)*, to the output of each resonator, $y_k(n)$, is equivalent to an IIR band-pass filter as follows:

$$H_{BP}^k(z) = \frac{gH_R^k(z)}{1 + g\sum_{j=1}^{N} H_R^j(z)} \tag{3.5}$$

$$H_{BP}^{k}(z) = 2g\frac{a_k z^{-1} - z^{-2}}{1 - 2a_k z^{-1} + z^{-2}} H(z) \tag{3.6}$$

where

$$H(z) = \frac{1}{1 + g\sum_{j=1}^{N} H_R^j(z)} \tag{3.7}$$

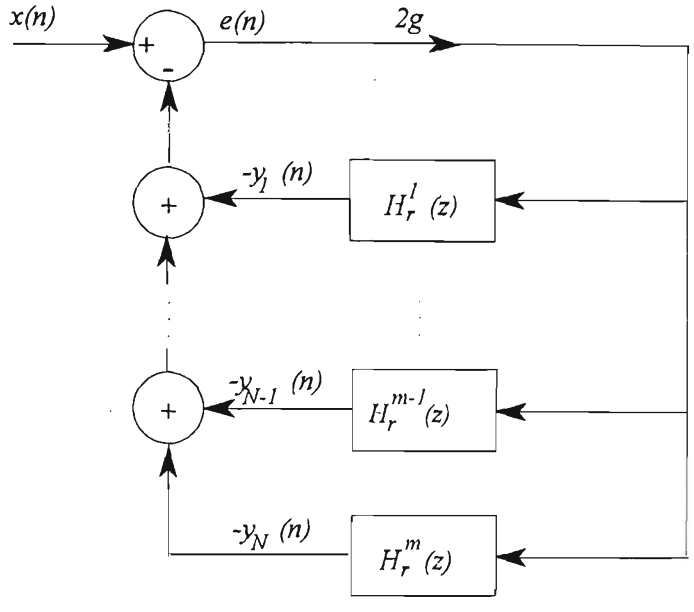


Figure 3.4: Resonator based filter bank.

For stability purposes, the feedback gain, g, must satisfy the following inequality [75]:

$$0 < g < \frac{1}{N} \tag{3.8}$$

where N is the number of band-pass filters. The bandwidth of each filter in filter bank is controlled by the parameter g. Figures 3.5 and 3.6 show the magnitude and phase responses of the band-pass filter for different values of g. It can be seen that the phase and magnitude response of each band-pass filter is exactly zero and unity respectively at the resonant frequency.

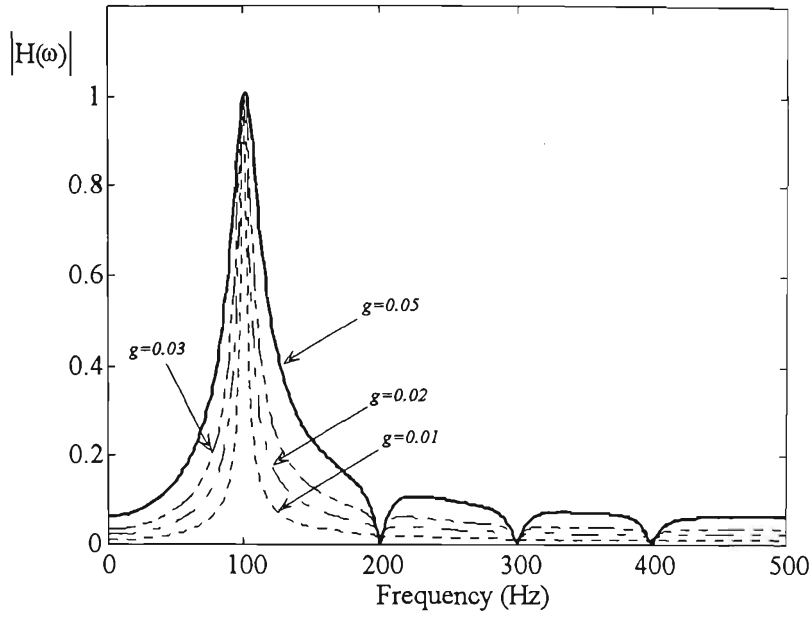


Figure 3.5: Transfer function magnitudes of the filter bank for: f_l=100 Hz and g = 0.01 (dotted) , g = 0.02(dash-dot), g = 0.03(dash-dot-dot), g = 0.05(solid line).

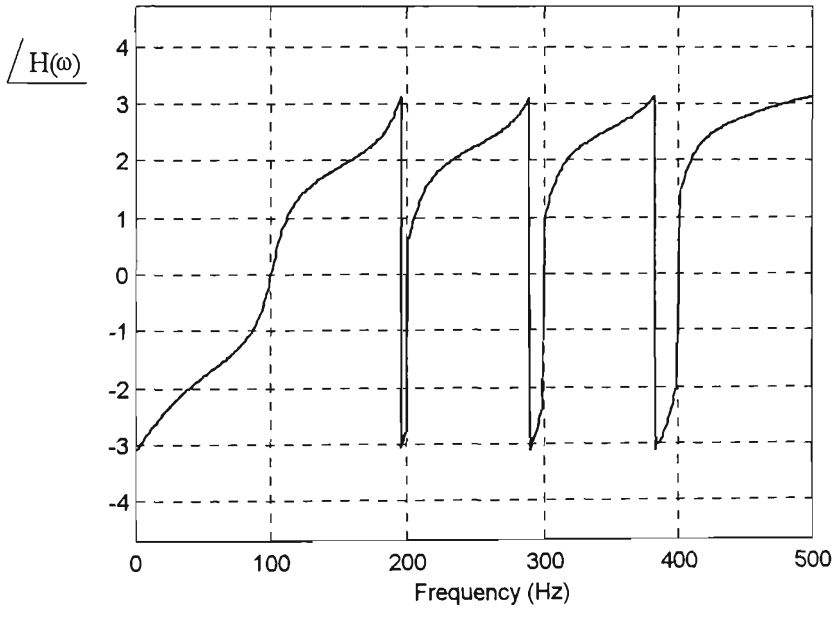


Figure 3.6: The phase transfer functions of the filter bank for f_l=100 Hz and, g = 0.05.

The resonant frequency of the k^{th} band-pass filter is given by:

$$f_k = \frac{1}{2\pi}\cos^{-1}(a_k) \tag{3.9}$$

The resonator frequency of each filter should be adapted to match the frequencies of the input data. When the filter has converged, the isolated input sinusoids are available at the outputs of the resonators. Figure 3.7 shows the magnitude response of the filter bank for

$N=4$ and frequencies of 32, 100, 150, 200 Hz. As seen in Figure 3.7, the zero transmission frequencies of each filter in filter bank are located at the bandpass frequencies of other filters.

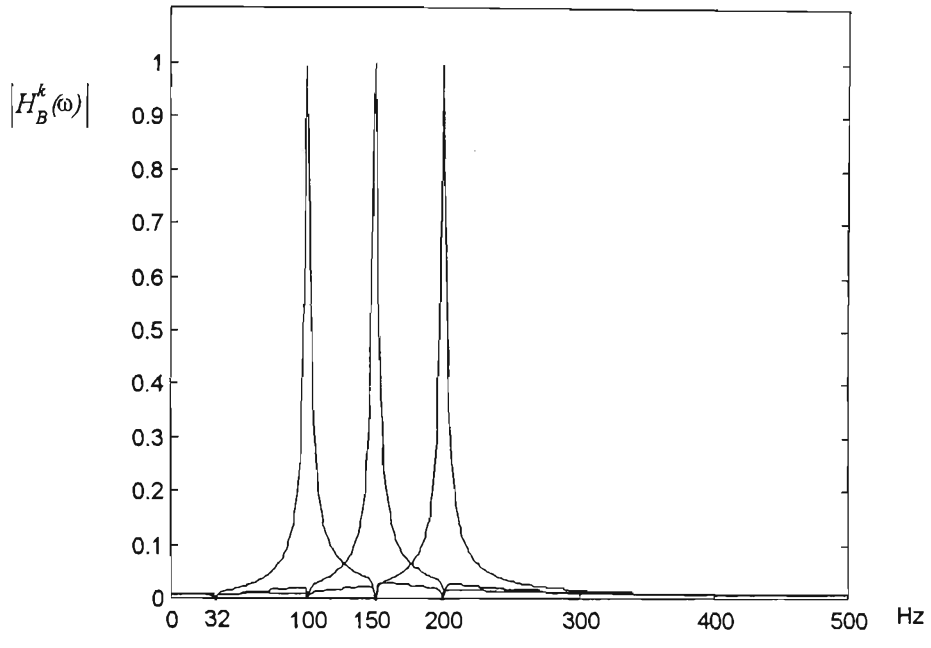


Figure 3.7: The magnitude transfer functions the filter bank for $N = 4$ and $g = 0.01$: f_1=32 Hz, f_2=100 Hz, f_3=150 Hz, f_4=200 Hz [72].

By being able to place the band-pass frequency of each filter at any arbitrary frequency a very good flexibility in terms of the frequency resolution and sampling frequency can be achieved when it is compared to DFT. For example, with a sampling frequency of 1000 Hz and the input signal with the frequencies of 32, 50, 100, 150 Hz, the required resolution for DFT is 2 Hz (the prime factor of 32, 50, 100, 150 Hz). In other words, to estimate the Fourier coefficients accurately, at least 500 samples are needed which results in an increase in acquisition time and longer processing delays.

The resonator frequencies of second-order IIR resonators (Equation(3.6)) should be adapted to match the frequencies of the harmonic components in the input signal. We only consider the case where the harmonic components are integer multiples of the fundamental frequency. For those frequency components which are not known such as interharmonics a separate adaptive frequency estimation technique can be used to track them and assign an extra filter in the filter bank for their retrieval.

3.3.2 Sliding Algorithm

In order to estimate the phase and magnitude of a sinusoid at the output of each band-pass filter a sliding constrained notch filter (CNFT) algorithm is employed [72]. Assuming that the input signal is real valued, that is:

$$x(n) = \sum_{k=1}^{N} \left(c_k \cos \omega_k n + d_k \sin \omega_k n \right) + v(t) \tag{3.10}$$

where $v(t)$ is a zero mean white noise. The output signal of the k^{th} filter is given by:

$$y_k(n) = c_k \cos \omega_k n + d_k \sin \omega_k n \tag{3.11}$$

Evaluating Equation (3.11) at $(n-1)^{th}$ sampling time gives:

$$y_k(n-1) = c_k \cos(\omega_k (n-1)) + d_k \sin(\omega_k (n-1)) \tag{3.12}$$

By solving the resulting linear Equations (3.11) and (3.12), a sliding algorithm can be derived as follows:

$$C_k(n) = y_k(n) = c_k \cos \omega_k n + d_k \sin \omega_k n \tag{3.13}$$

$$\begin{aligned} D_k(n) &= \frac{-1}{\sin \omega_k} [y_k(n-1) - \cos \omega_k y_k(n)] \\ &= d_k \cos \omega_k n - c_k \sin \omega_k n \end{aligned} \tag{3.14}$$

The Fourier coefficients of the output signal can be obtained as follows [72]:

$$\begin{bmatrix} c_k(n) \\ d_k(n) \end{bmatrix} = \begin{bmatrix} \cos \omega_k n & -\sin \omega_k n \\ \sin \omega_k n & \cos \omega_k n \end{bmatrix} \begin{bmatrix} C_k(n) \\ D_k(n) \end{bmatrix} \tag{3.15}$$

The amplitude (A_m) and phase (ϕ_k) of each component are calculated as:

$$A_m = \sqrt{c_k^2 + d_k^2}; \qquad \phi_k = -\tan^{-1}\left(\frac{c_k}{d_k}\right) \tag{3.16}$$

Manipulation of Equations (3.13) and (3.14) leads to the following expression:

$$C_k^2(n) + D_k^2(n) = c_k^2 + d_k^2 = A_m^2 \tag{3.17}$$

This means that the amplitude can be updated at every sample time without computing Equation (3.15).

Note that Equations (3.13), (3.14) and (3.15) are evaluated at the time instant when the transient response of the filter has elapsed. However, in situations where the sinusoidal parameters (phase and amplitude) are time varying, Equations (3.13), (3.14) and (3.15) can be computed at any sample time to update the estimates. For such cases, the rate of parameter variation must be slower than the required acquisition time of the filter.

The residual error signal, *e(n)*, of the filter bank structure (Figure 3.4) can be monitored to identify transient periods caused by frequency and/or magnitude changes in load current. In steady state conditions this error converges to a minimum value while during transient periods it reaches a maximum value.

3.4 FREQUENCY ESTIMATION

Online estimation of the of load current harmonics in time-varying conditions requires an accurate frequency and phase estimation of the fundamental component. The estimated fundamental frequency is used to adjust the centre frequency of each filter in the filter bank. Two methods, namely; adaptive IIR filtering and FM demodulation techniques are evaluated in the next Section to meet the above requirement.

3.4.1 Adaptive IIR Filtering

Adaptive infinite impulse response (IIR) filtering is widely used for estimating the frequency of unknown sinusoids buried in noise [76]. In this technique shown in Figure 3.8, a bandpass IIR filter is used. The band-pass frequency is adaptively varied such that the mean square error of the filter is minimised [77]. The error signal $e(n)$ is defined as:

$$e(n) = x(n) - y(n) \tag{3.18}$$

where *y(n)* is the output of the bandpass filter and *x(n)* is the input signal. In this project an IIR bandpass filter [78] has been adopted which is computationally more efficient when compared to adaptive IIR filter structures [72] proposed in [79-81]. The transfer function of this IIR band pass filter is given by:

$$H_{BP}(z) = (1-r)\frac{1-z^{-2}}{1+raz^{-1}+(2r-1)z^{-2}} \tag{3.19}$$

where r is a parameter which controls the bandwidth of the filter and should be in the range $0.5< r <1$ to ensure that the filter is stable. Figure 3.9, shows the magnitude response of the filter for various values of r. The centre frequency of filter, f_p, is then given by:

$$f_p = \frac{1}{2\pi}\cos^{-1}\left(\frac{-a}{2}\right) \tag{3.20}$$

where $-2< a <2$. When the band-pass frequency is placed at the location of the input frequency, the error of the filter output will be minimised. The input frequency can then be easily estimated from parameter a.

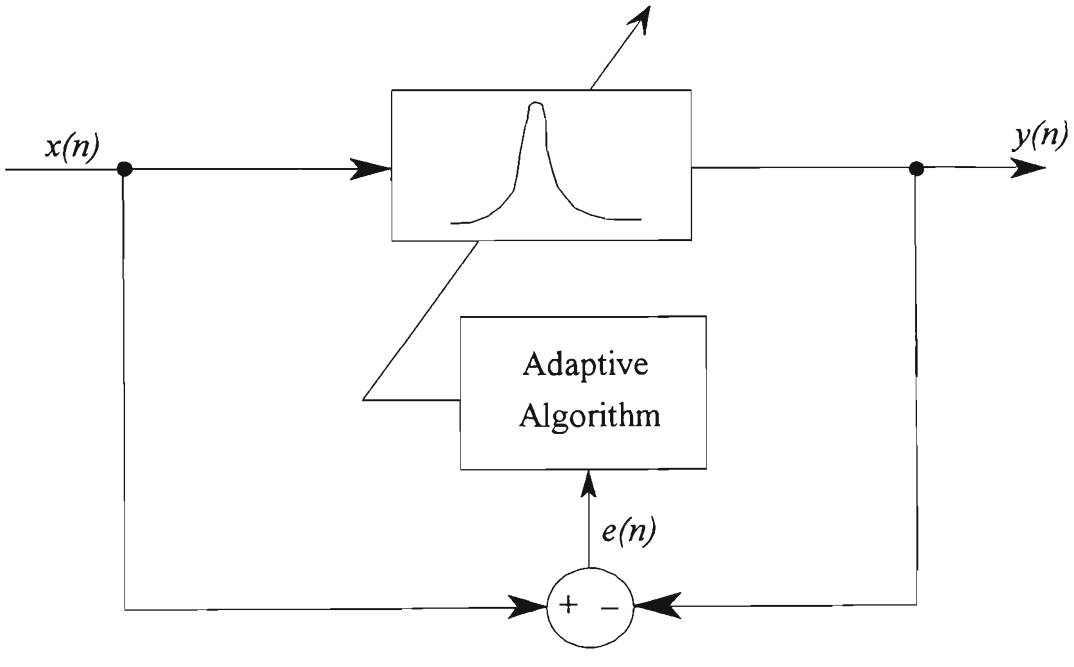


Figure 3.8: Adaptive IIR Filtering.

Various adaptive algorithms have been proposed to adjust the filter parameter, a, which controls the centre frequency of the bandpass filter. A Gradient decent algorithm [82] is adopted in this project which is simple to implement due to its low complexity.

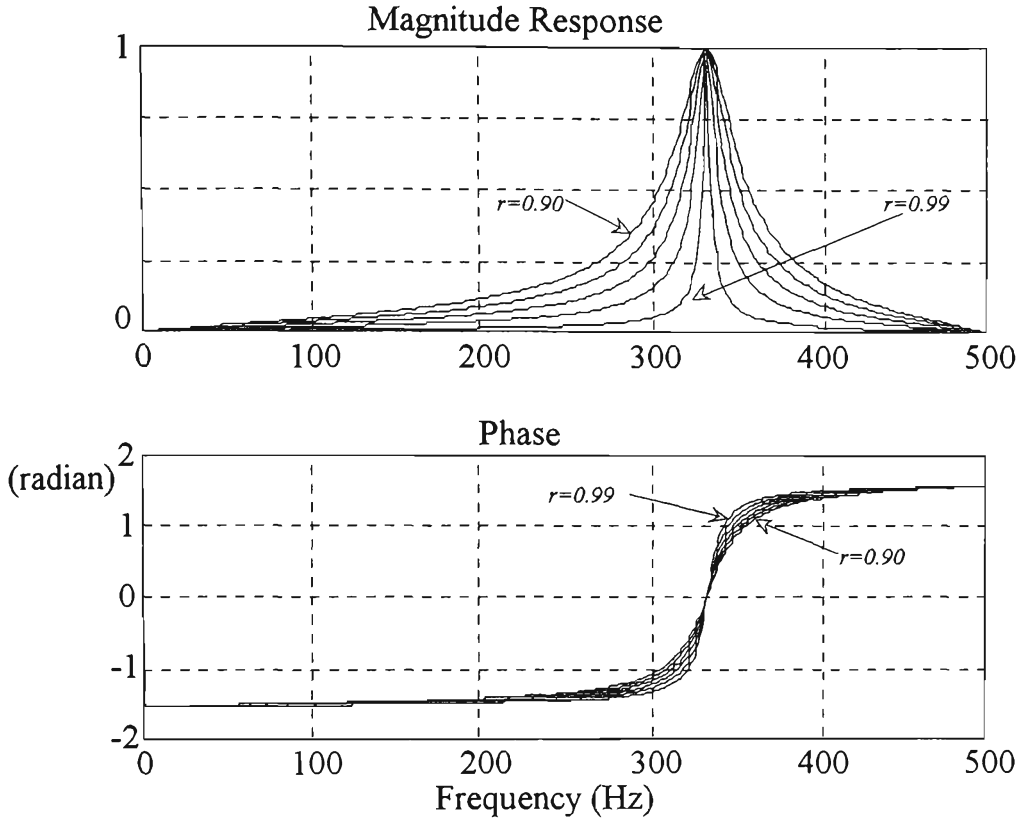


Figure 3.9: Frequency response of IIR filter for: f_p=320 Hz and r = 0.9-0.99.

3.4.1.1 Gradient Decent Algorithms

The goal of the Gradient algorithm is to search for the values of a which minimises the variance of the error signal $\xi = E[e^2(n)]$. The recursive gradient-based expression for updating the coefficient a is given by [83]:

$$a(n+1) = a(n) - \mu\nabla_a \tag{3.21}$$

where μ is a step size which controls the algorithm convergence rate and ∇_a is the partial derivative of the mean squared error with respect to a. A normalised factor is incorporated in to Equation (3.18) as follows:

$$a(n+1) = a(n) - \mu\frac{\nabla_a}{\varepsilon + \Gamma} \tag{3.22}$$

where ε is a small positive real number to ensure that division by zero does not occur. Γ is a smoothed estimate of the power of the ∇_a and is given by:

$$\Gamma(n+1) = \gamma\,\Gamma(n) + (1-\gamma)\nabla_a^2 \tag{3.23}$$

where γ is a forgetting factor in the range of $0 < \gamma < 1$ and ∇_a is given as [72]:

$$\nabla_a = 2e_i(n)\frac{\partial y}{\partial a} = -2e(n)y^f(n) \tag{3.24}$$

where $y^f(n)$ is an estimate for $\frac{\partial y(n)}{\partial a}$ can be expressed in the following recursive form:

$$y^f(n) = -r\,y(n-1) - r\,a\,y^f(n-1) - (2r-1)\,y^f(n-2) \tag{3.25}$$

The flow-graph of the filter implementation using "Direct Form II Transposed" [70] is shown in Figure 3.10.

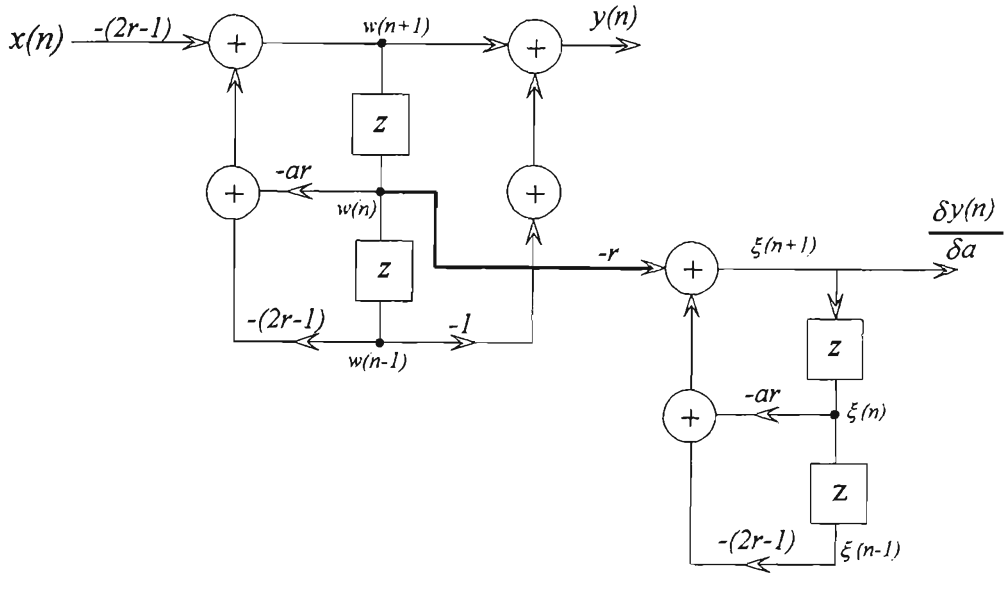


Figure 3.10: The flow-graph of the filter implantation.

3.4.2 Frequency Demodulation Technique

Frequency modulation (FM) and demodulation techniques are well established and understood when implemented using analog circuits. Recently, state-of-the-art digital technology has allowed radio-frequency (RF) signals to be processed digitally [84]. Modulated RF signals are digitally sampled and then demodulated in real time using signal processing techniques A digital FM demodulator is proposed to track the variation of the fundamental power system frequency (signal in FM) from 50 Hz (carrier in FM) [85].

In the frequency demodulation technique it is assumed that the frequency variation with respect to 50 Hz, Δf, has been modulated with the power system voltage waveform (50

Hz carrier). Figure 3.11 shows the block diagram of the proposed FM demodulation technique for fundamental frequency tracking. Consider the input signal as:

$$x(n) = A\cos(\omega_0 n + \Phi(n)) + \varepsilon(n) \tag{3.26}$$

$$\Phi(n) = 2\pi\Delta f n \tag{3.27}$$

where A is the magnitude of the signal at the fundamental frequency ($\omega_o = 2\pi f_o$) and Φ(n) is the instantaneous phase due to the frequency variation. Note Δf is an unknown parameter. $\varepsilon(n)$ is the sum of the noise and harmonics in the input signal.

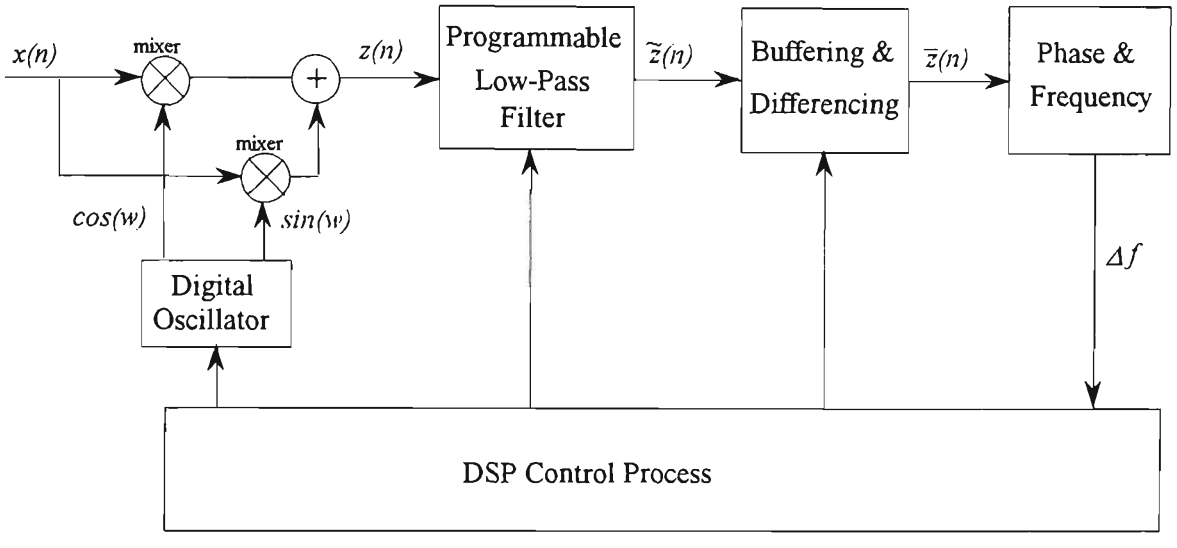


Figure 3.11: Digital FM demodulator frequency tracking.

As shown in Figure 3.11, the output of the mixers, $z(n)$, can be formed as follows:

$$\begin{aligned} z(n) &= x(n)\left[\cos(\omega_0 n) + j\sin(\omega_0 n)\right] \\ &= \frac{A}{2}\left[e^{j(2\omega_0 n + \Phi(n))} + e^{j(\Phi(n))} + e^{j(\tilde{\Phi}(n))}\right] \end{aligned} \tag{3.28}$$

where $\tilde{\Phi}(n)$ is the contribution of noise $\varepsilon(n)$, on the instantaneous phase Φ(n). The frequencies of the signals which carry the phase information lie in the range DC and $2f_o$. The high frequency component at $2f_o$ (the first term in Equation (3.28)) can be removed by a low pass filter with cut-off frequency, f_{cut}, above the bandwidth of Δf [70]. The low pass filter should possess a linear phase and constant group delay. At the output of the low pass filter we have:

$$\tilde{z}(n) = \frac{A}{2} e^{j\phi(n)} + \tilde{\varepsilon}(n) \tag{3.29}$$

where $\tilde{\varepsilon}(n)$ is the sum of the filtered noise sequences from *z(n)* and the attenuated signal at high frequency. When the signal-to-noise (SNR) ratio is high, it can be shown that:

$$\Phi(n) \cong angle(\tilde{z}(n)) \tag{3.30}$$

is a good estimate of $\Phi(n)$. From Equation (3.29), the estimate for the frequency variation can be found by:

$$\bar{z}(n) = \tilde{z}(n+1) * \tilde{z}^{*}(n-1) \tag{3.31}$$

$$\bar{z}(n) \approx \frac{A^2}{4} e^{j(\phi(n+1)-\phi(n-1)+\tilde{\phi_e}(n))} + \tilde{\varepsilon}(n) \tag{3.32}$$

where $\tilde{z}^{*}(n-1)$ is the conjugate of the $\tilde{z}(n-1)$. Finally, the frequency deviation is calculated as:

$$\Delta\tilde{f} = \frac{\Delta\Phi(n)}{4\pi\Delta t} = \frac{f_s}{4\pi} angle(\bar{z}(n)) \tag{3.33}$$

3.4.2.1 Low Pass Filtering

As mentioned above, a low pass filter with linear phase and constant group delay is required to remove the high order components in the frequency demodulation technique. Finite impulse response (FIR) filters with constant group delay and linear phase introduces no phase distortion which is an essential requirement for this technique.

The main disadvantage in using an FIR filter is its high computational burden and more importantly its delay. A high order FIR filter is more accurate and robust to noise but increases the computational burden and filtering delay. The order of a FIR, N_{FIR}, is determined based on the sampling frequency of the input data acquisition system and required band pass characteristics. To reduce the order of the FIR filter the sampling frequency should be reduced and a signal with lower bandwidth (equal to the maximum harmonic frequency buried in signal) should be used.

3.4.2.2 Decimation

In order to retrieve the higher order harmonic components of the signal and to avoid aliasing problems, the power system voltage and current waveforms are usually sampled at high sampling frequencies causing the harmonic components to be closely spaced in the frequency domain. In most cases, the processing effort required to implement the system is proportional to the number of samples.

Decimation in time domain can reduce the number of samples and consequently the required calculations. Usually, when decimation is performed, an anti-aliasing filter is applied before down-sampling to alleviate the effects of aliasing introduced from the operation of down-sampling. In this regard, the original input signal should be low-pass filtered before decimation. The resulting bandwidth and sample-rate reduction allows real-time calculations involved in processes such as adaptive digital filtering and FM demodulation to be effectively carried out. Also decimation after low pass filtering places the lower order harmonics, eg. the fundamental, in the middle of the signal bandwidth where the accuracy of the adaptive algorithm is at its maximum.

3.5 SIMULATION RESULTS

Simulations using MATLAB [58] package were developed to verify the proposed frequency estimation and filter bank harmonic measurement techniques.

3.5.1 Frequency Estimation

Simulation results are presented to illustrate the performance of the adaptive IIR filter and FM frequency demodulation techniques for frequency tracking. For this simulation a waveform with a time-varying fundamental frequency in the presence of white noise with harmonic components up to the 7^{th} order has been generated. A sampling frequency of 800 Hz is chosen which is greater than twice the highest frequency in the signal (ie. 7^{th} harmonic).

Two cases have been considered for time-varying frequency changes as shown in Figure 3.12. In the first case, the fundamental frequency is modulated by a multi-step frequency change from 50 to 50.5 Hz and in the second case, a sinusoidal frequency deviation with a low swing frequency of 5 Hz has been added to the fundamental frequency.

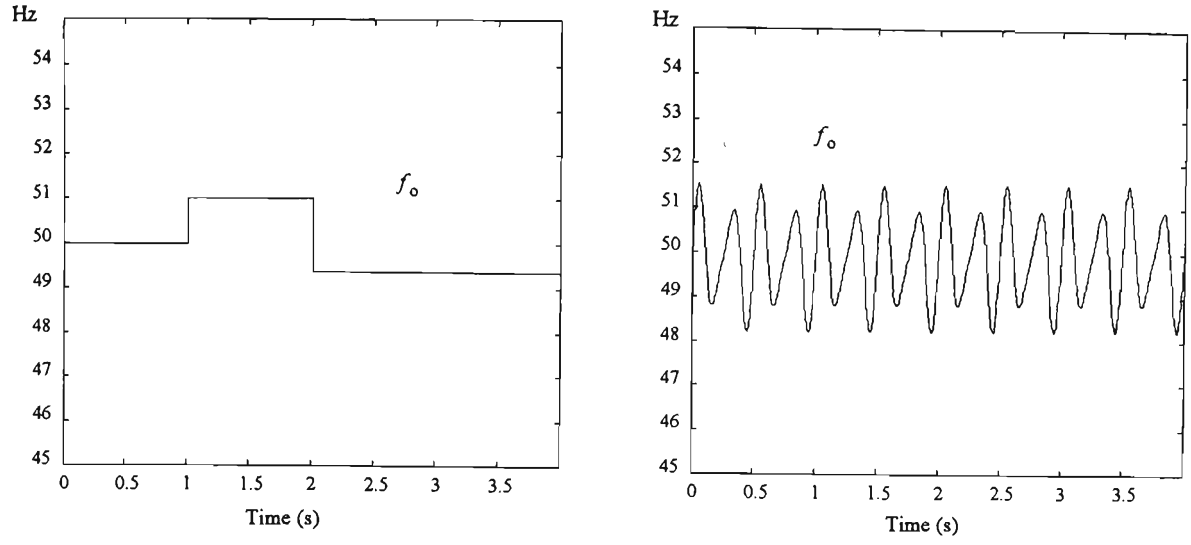


Figure 3.12: Fundamental frequency variation with time:
(a) step changes, (b) sinusoidal changes.

3.5.1.1 Adaptive IIR Filter

Figures 3.13 (a) and (b) show the estimated fundamental frequency for given input test signal for different signal-to noise-ratios. The simulation results show that the adaptive IIR filter provides an accurate estimate of the fundamental frequency after the transient has decayed. It can be noted that the maximum error of the frequency estimates occurs at the beginning of the transient, and lasts for 0.3 sec.

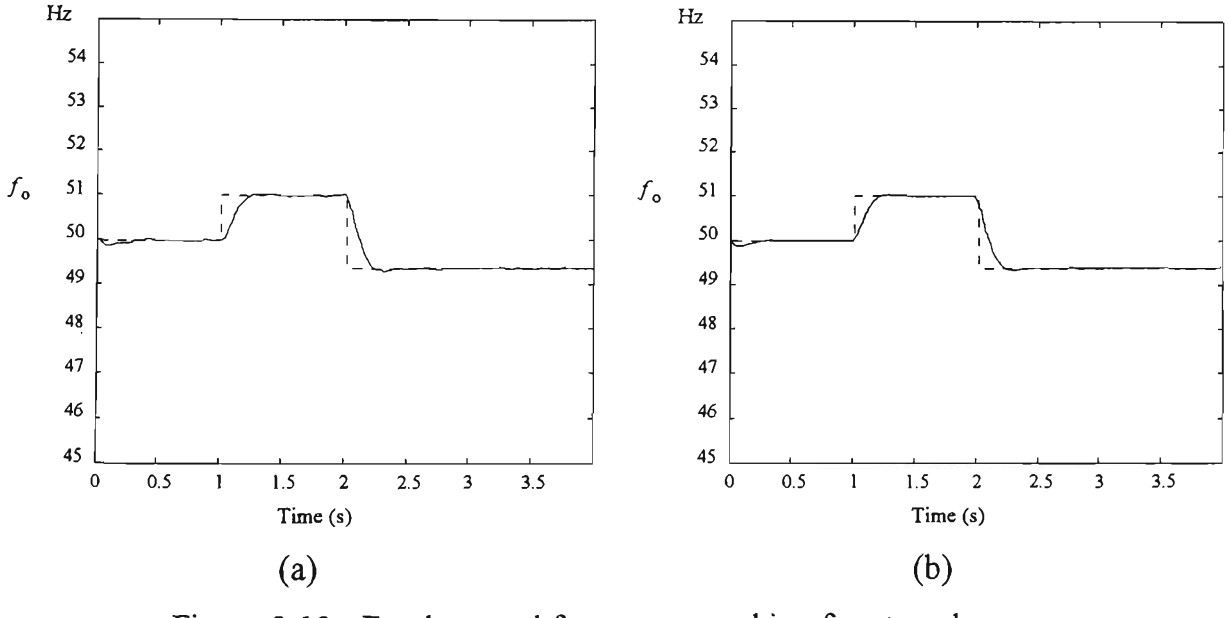
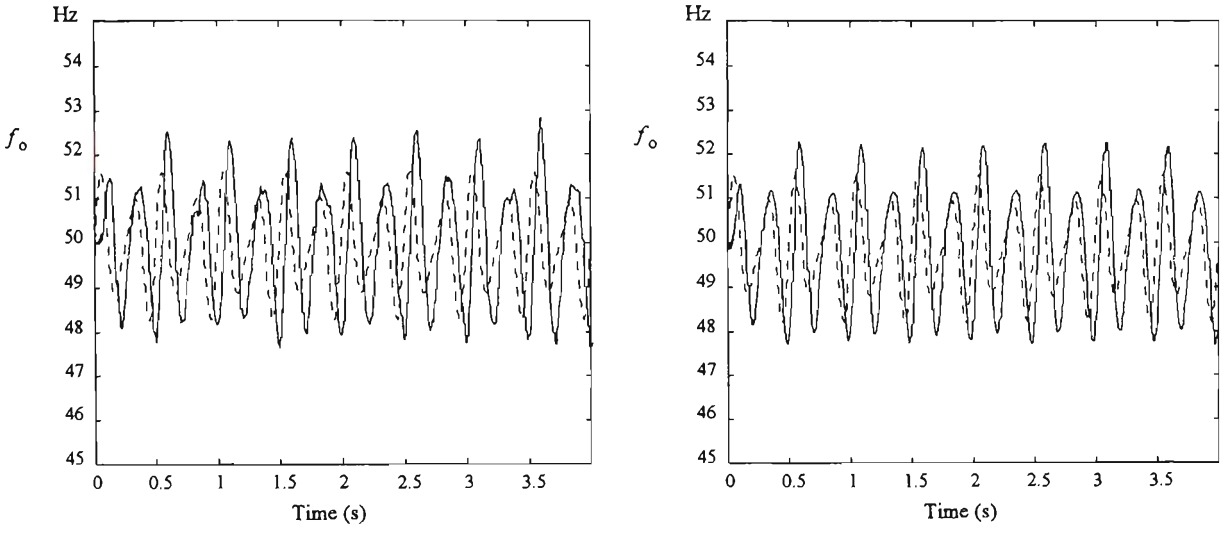


Figure 3.13: Fundamental frequency tracking for step changes:
(a) μ=0.01, Γ=1, γ=0.9, SNR= 25 dB, (b) μ=0.03, Γ=1, γ=0.9, SNR=40 dB.

Figure 3.14 shows the performance of adaptive IIR filter in tracking the sinusoidal time-varying frequency variation. Smaller values for μ in the adaptive algorithms give stable but tracking with a delay. Higher value for μ causes an oscillation around the desired signal.



(a) (b)

Figure 3.14: Fundamental frequency tracking sinusoidal changes:
(a) μ=0.01, Γ=1, γ=0.9, SNR= 25 dB, (b) μ=0.03, Γ=1, γ=0.9, SNR=40 dB.

3.5.1.2 FM Demodulation (FMD)

Figure 3.15 shows the performance of the FM demodulation technique for a step change in response to the same test signal conditions as described in Section 3.5.1. As there is no adaptation process in this technique, the delay in response is only due to the order of FIR filter used for low pass filtering. In contrast to adaptive IIR filtering, in FM demodulation technique there is no adaptive tracking which means that the estimated signal in high SNR condition is a replica of actual frequency variation.

As it can be seen in Figure 3.15, the FM demodulation gives improved performance in terms of accuracy and the delay of tracking when it is compared to the adaptive IIR filtering technique. For example, the delay of tracking in the FM demodulation technique is about 0.15 second (Figure 3.15) when it is compared to 0.3 seconds in the case of adaptive IIR filtering as illustrated in Figure 3.13.

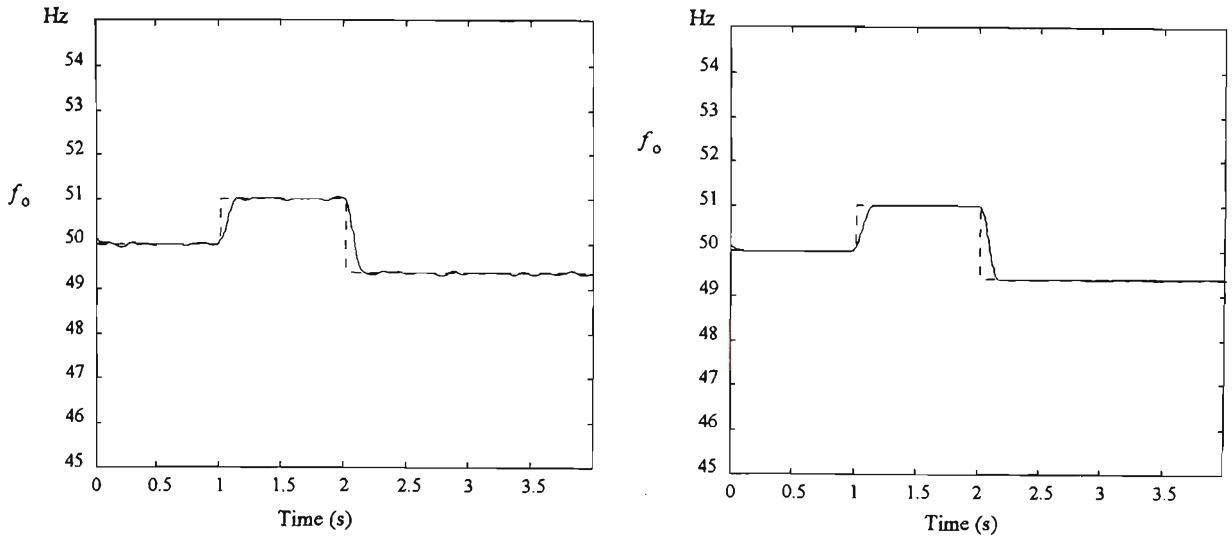


Figure 3.15: Fundamental frequency tracking for step changes:
(a) f_{cut} =5 Hz, N_{FIR}=50, SNR=25 dB, (b) f_{cut} =5 Hz, N_{FIR}=30, SNR=40 dB.

Figure 3.16 shows the performance of the FM demodulation technique for sinusoidal changes in the fundamental frequency for two test signals with different SNRs. Figure 3.16 (a) shows the frequency tracking results using a 50th order FIR filter and a SNR=25 dB. As shown by Equations (3.29) and (3.30), the contribution by the noise, $\tilde{\varepsilon}(n)$, on the estimated phase, $\tilde{\Phi}(n)$, is limited by low pass filter performance. High order FIR (ideal low pass filter) is required when SNR is low which increases the computational burden and delay of tracking (Figure 3.16 (a)).

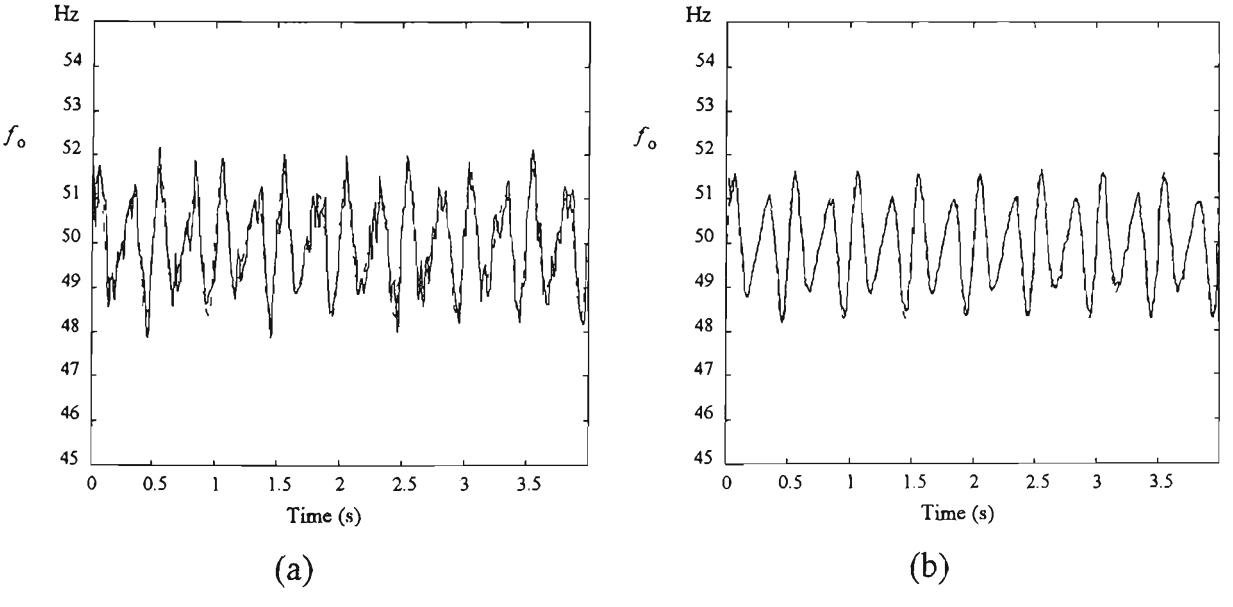


Figure 3.16: Fundamental frequency tracking for sinusoidal changes:
(a) f_{cut} =5 Hz, N_{FIR}=50, SNR=25 dB, (b) f_{cut} =5 Hz, N_{FIR}=30, SNR=40 dB.

3.5.2 Harmonic Estimation

A performance evaluation of the proposed harmonic estimation and measurement technique have been carried out by digital simulation. Two simulations with the same input signal are used to compare the proposed filter bank sliding harmonic estimation with short term Fourier transform. The input signal consists of a non-sinusoidal load current waveform with a time-varying fundamental frequency and magnitude. The harmonic components of the load current are assumed to be *"odd"* and integer multiples of the fundamental frequency up to the 29^{th} order. A sampling frequency of 3200 Hz is chosen which is more than twice the highest frequency component in the input signal. The variation of the fundamental magnitude and frequency of the test load current are shown in Figures 3.17 and 3.18 respectively.

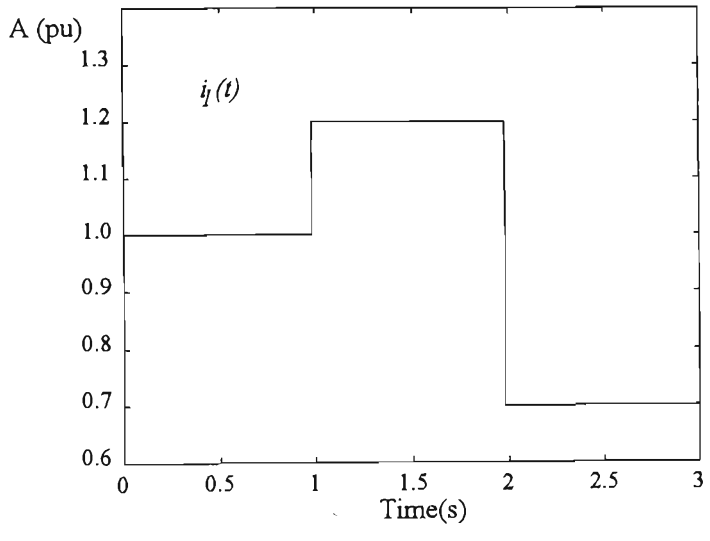


Figure 3.17: The magnitude variation of test load current signal.

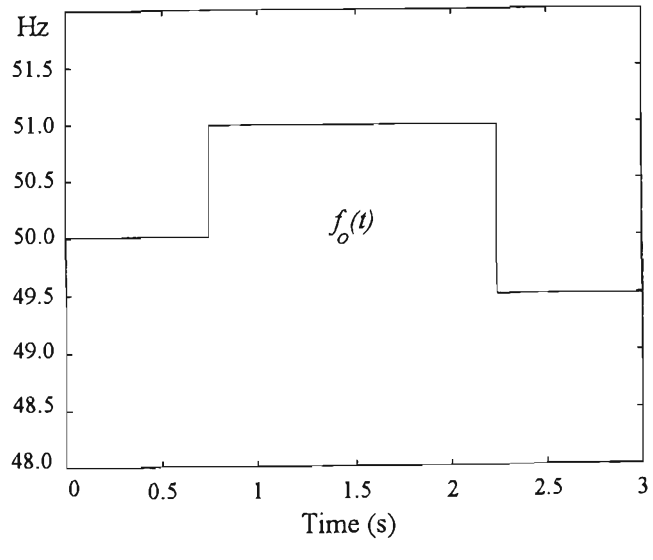


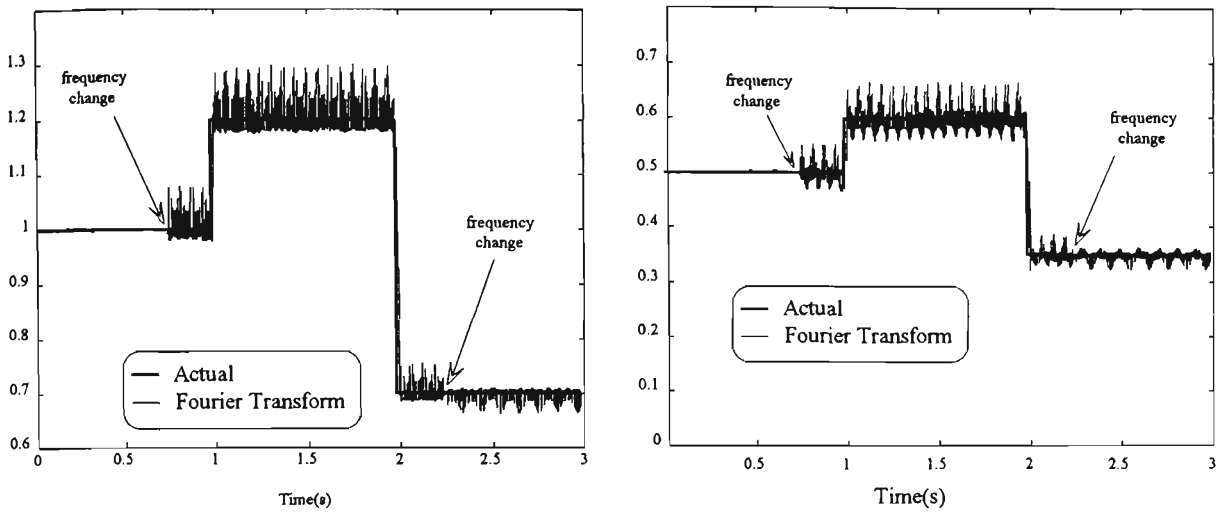
Figure 3.18: The fundamental frequency variation of test load current signal.

3.5.2.1 Short Term Fourier Transform

The short term Fourier transform (STFT) has been implemented for performance comparison purposes. With a sampling frequency of 3200 Hz, a 64 sample wide Hamming window is used [70]. With extra processing, the magnitude and phase of each harmonic is calculated using the imaginary and the real parts of the corresponding STFT results. Depending on the application, the STFT output can be modified and the reference waveform is generated using the inverse FFT (IFFT).

Simulation results of the short term Fourier transform for a given non-linear load current waveform are shown in Figures 3.19-3.21. The magnitude and phase information of the harmonic components are determined assuming that the fundamental frequency is 50 Hz and the harmonic components are integer multiples of the fundamental. As illustrated in Figures 3.19-3.21, the short term Fourier transform can track the step changes in the magnitude of the harmonic components for low order harmonic components accurately. However, where there is a deviation in the fundamental frequency, a constant error can be seen in STFT results. As there are no non-integer harmonic components in the test signal, and sampling frequency meets the Nyquist criteria, the error is due to leakage from one frequency component to the adjacent ones in STFT results.

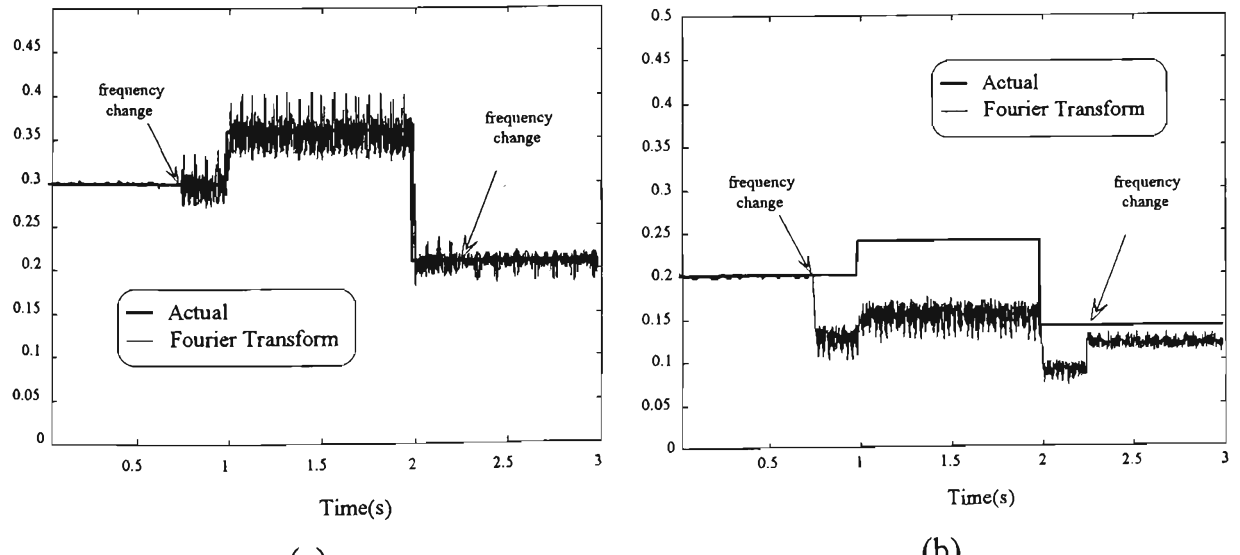
When there is a frequency deviation in the fundamental frequency of the supply system (50 Hz), its effect is propagated to the harmonics in proportion to the harmonic order. It results in an error in the estimation of all harmonic components (leakage). Figure 3.19 shows the estimated and actual magnitudes for fundamental and third harmonic. As seen in Figure 3.19, when a frequency step change occurs at $t = 0.75$ (sec), the estimated magnitudes show a constant error (bias). However, the trajectory of step changes in magnitude is being tracked (with a bias error). For the second step change of frequency which takes place at $t = 2.25$ (sec), again the magnitude shows a bias error.



(a) (b)

Figure 3.19: Actual and estimated amplitude: (a) Fundamental, (b) 3rd order harmonic.

Figure 3.20 shows the estimated and actual magnitudes for 5th and 25th harmonics. Similar to Figure 3.19, the trajectory of step changes in the magnitude of the signal at t = 1 and t = 2 seconds have been tracked. However the leakage error can still be seen as a bias error on estimated magnitudes. At t = 2.25 another frequency deviation (second step change) in fundamental frequency occurs which is less than the first step change. As it can be seen form Figure 3.20 (b) the bias error after the second frequency step change is significantly reduced due to smaller frequency deviation. However, estimated magnitudes for both low and high order harmonic components continue to show a bias error.



(a) (b)

Figure 3.20: Actual and estimated amplitude: (a) 5th, (b) 25th order harmonic.

Figure 3.21 shows the estimated magnitude for 26th and 29th harmonic components. As there were no *"even"* harmonic components in the test load current waveform, the magnitude of 26th harmonic component is estimated to be zero up to the time of first frequency step change (t = 0.75) and non-zero after that. As illustrated in Figure 3.21 (a) the STFT shows a bias error for 26th harmonic which is due to the leakage from neighbouring frequency component, 25th (Figure 3.20-b). This is one of the main pitfalls of STFT (FFT) technique which concludes that STFT is not suitable for harmonic estimation in a time-varying situation.

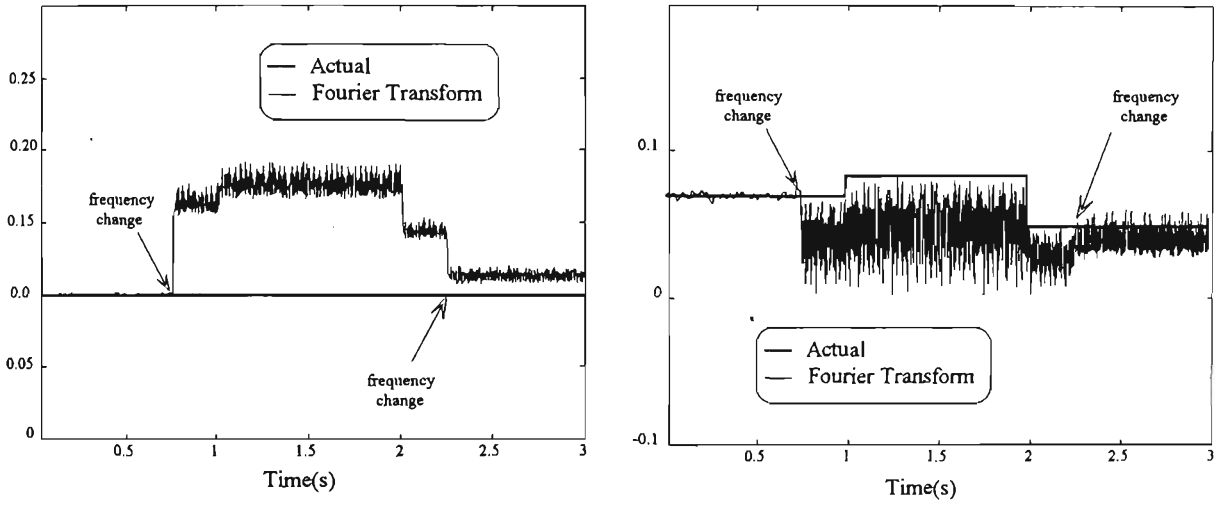


Figure 3.21: Actual and estimated amplitude: (a) 26th, (b) 29th order harmonic.

3.5.2.2 Filter Bank harmonic estimation and measurement

Figure 3.22 shows the proposed system for harmonic estimation and measurement. The estimated frequency is applied to the filter bank to retrieve the individual harmonics up to the N^{th} order. Figure 3.23 shows the actual and estimated segments of the fundamental waveform.

The results indicate that this technique can track the variation in frequency and magnitude of the signal quite well. In steady state conditions the waveforms in filter bank outputs are undistorted versions of the input harmonic components and there is no phase error propagation as in the case of the cascade line enhancer [62].

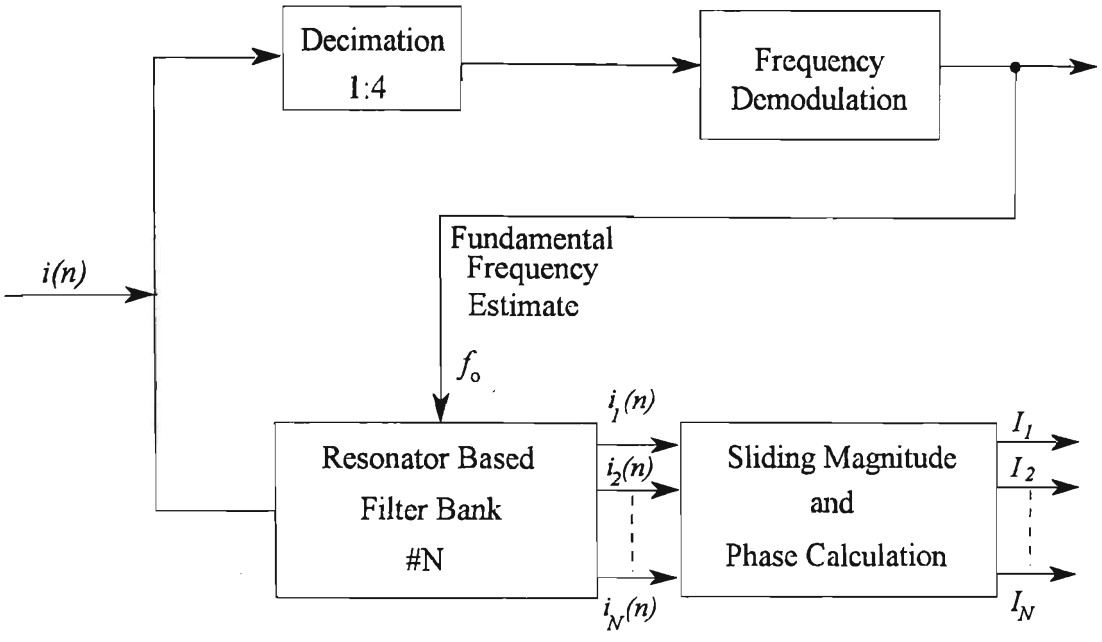


Figure 3.22: Proposed technique for sliding measurement of power system harmonics.

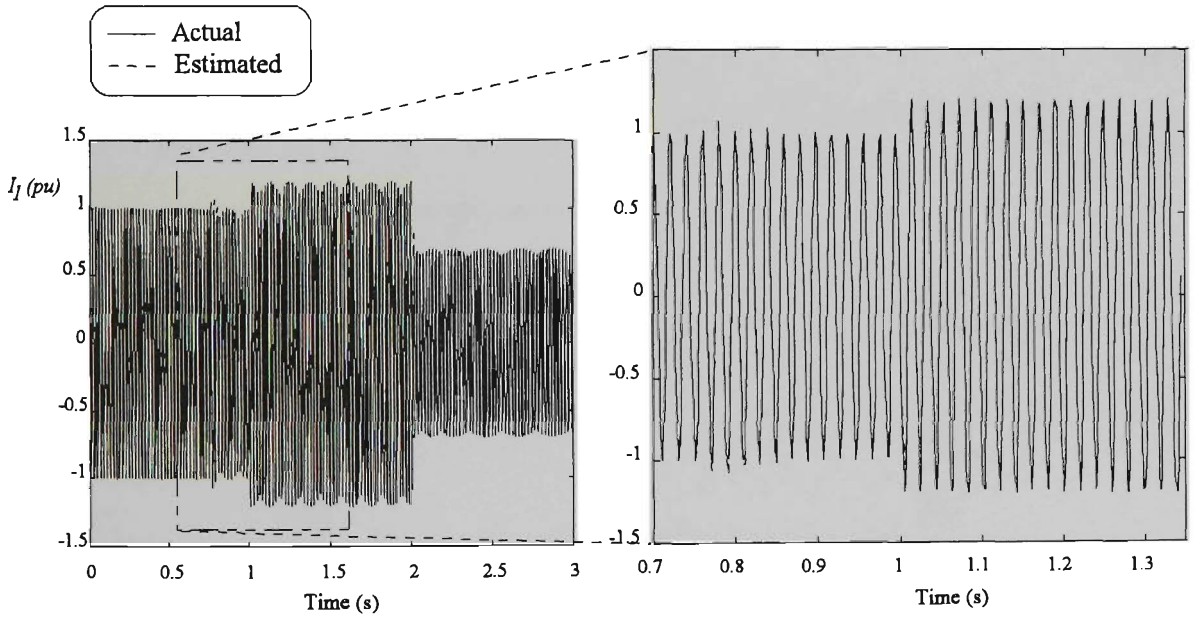
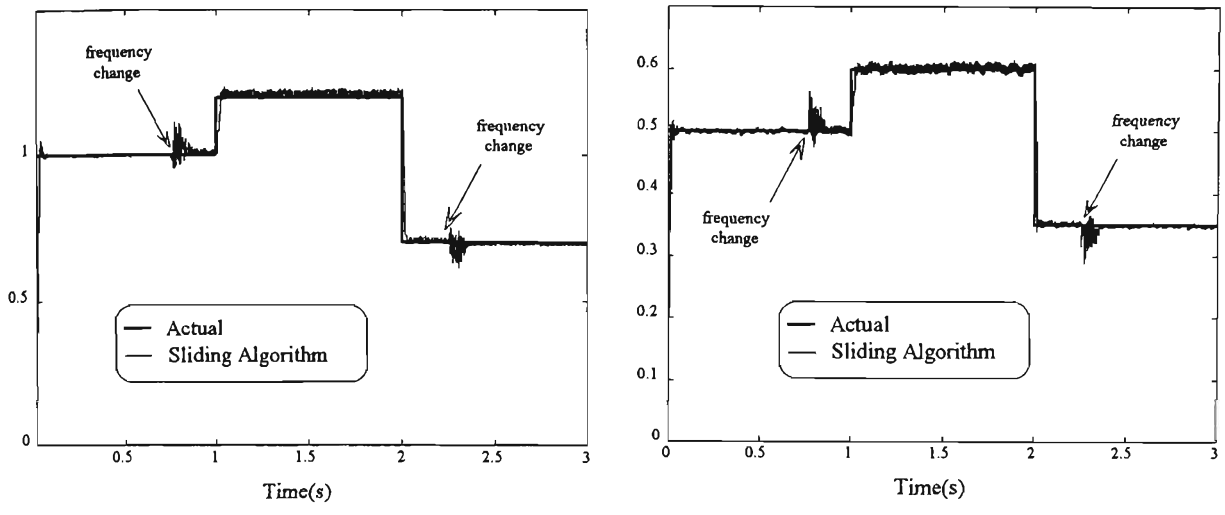


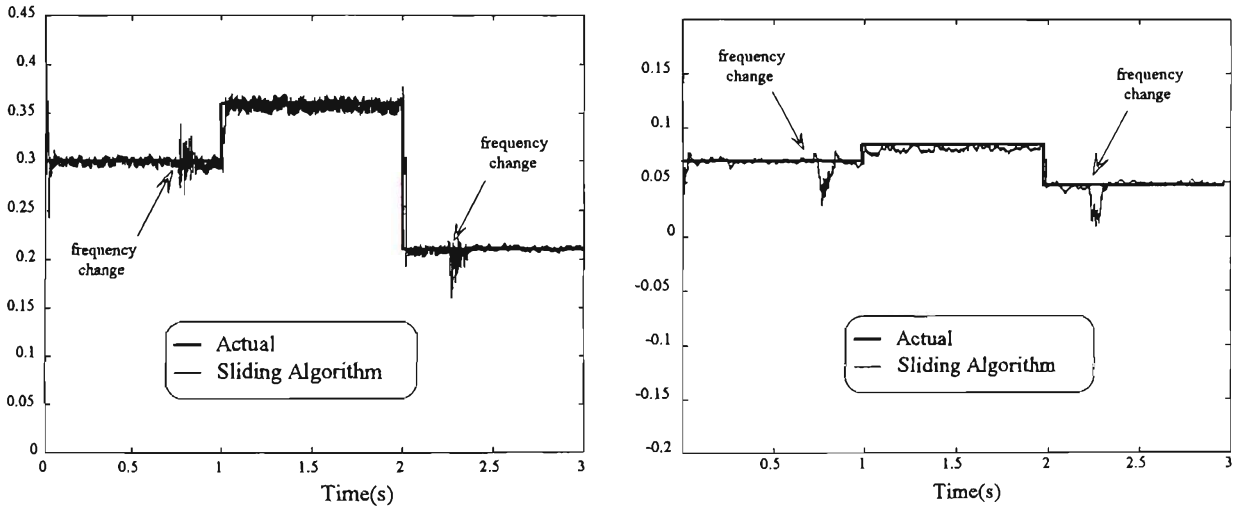
Figure 3.23: Actual and estimated fundamental waveforms.

The magnitude and phase of each harmonic waveform can be calculated by the using the sliding algorithm. Figures 3.24-3.25 show the estimated magnitude of fundamental, 3rd, 5th and 29th order harmonics. As illustrated in Figure 3.24, the amplitude of the fundamental and 3rd order harmonic are retraced after each disturbance caused by a change in the signal frequency and magnitude.



(a) (b)

Figure 3.24: Actual and estimated amplitude: (a) Fundamental, (b) 3rd order harmonic.



(a) (b)

Figure 3.25: Actual and estimated amplitude: (a) 5th, (b) 29th order harmonics.

The simulation results show that the sliding algorithm for harmonic magnitude calculations is capable of tracking changes in the input signal magnitude and frequency. The harmonic magnitude is estimated accurately when the transient in the output of the filters has decayed. For some online applications such as active power filters, this transient behaviour destabilises the process of harmonic reduction. Therefore, during these transient periods the harmonic reduction should be reduced or temporarily stopped. As mentioned before, the transient period can be detected using the residual error signal, *e(n)* in filter bank structure.

3.5.2.3 Computational Burden

From a computational burden point of view, the total computational burden of STFT for each incoming sample consists of an N point windowing and FFT, phase and magnitude calculations for N harmonics and finally an inverse FFT and windowing to construct the reference waveform from the modified FFT coefficient. To compare the computational burden of the filter bank based technique with STFT technique, the number of floating point operations (FLOPS) for simulations of this case study have been used. As shown in Table 3.1 the number of FLOPS for STFT is much higher than for the filter bank based technique.

Table 3.1: Computational burden in terms of FLOPS.

Short term Fourier transform				
Windowing	*FFT*	*Magnitude*	*IFFT*	*Total*
323	5558263	2779131	5558263	13895981
Filter bank sliding measurement				
Frequency Tracking	*Harmonic estimation*	*Sliding measurement*		*Total*
948284	3129244	3083388		7160916

3.6 CONCLUSION

In this chapter a new adaptive structure based on the combination of resonator filter bank and FM demodulation frequency tracking was proposed for estimation of the fundamental and retrieval of harmonic components of load current. The phase and gain of each filter at the frequency of interest are equal to zero and one, respectively. Hence, the harmonic components are available at the output of each filter with zero phase shift and with same magnitude of the input components. The sliding CNFT algorithm was employed to calculate the phase and amplitude of the estimated harmonic components.

In order to track the input frequencies for the filter bank parameterisation, two frequency estimation techniques, adaptive IIR filtering and FM demodulation, have been considered. Simulation results for frequency tracking for time-varying situations have been presented and compared. The simulation results were shown to be better for FM demodulation when compared with the adaptive IIR filtering techniques.

A performance evaluation of the proposed technique for harmonic estimation of a nonlinear load current waveform was carried out. The simulation results for filter bank and STFT techniques were presented for a non-linear load current with time-varying frequency and magnitude. The simulation results show that the proposed filter bank structure provides better performance over a wide range of harmonic orders. It was also shown that the proposed technique is computationally more efficient when compared with the STFT.

CHAPTER 4.

ACTIVE POWER FILTER IMPLEMENTATION

4.1 INTRODUCTION

Active power filters are used in power systems for harmonic compensation, reactive power compensation and voltage control. This Chapter discusses the implementation details associated with the proposed frequency and harmonic estimation techniques for the active power filtering system. By combining the above techniques with limits imposed by the harmonic standards, compensation of harmonics and reactive power can be carried out which lead to an APF with a reduced power rating. The proposed active power filter provides flexible and selective harmonic reduction for nonlinear loads.

Partial and selective harmonic compensation and power factor correction of the load current for steady state and time varying situations have been implemented. A digital signal processor platform has been selected for all control strategies as well as PWM switching control. A functional system configuration of the proposed DSP-based active power filter is shown in Figure 4.1. The DSP performs the following tasks:

1. data acquisition of the supply voltage, load current, APF filter current and voltage waveforms,
2. estimation of the mains supply voltage phase and frequency,
3. estimation of the load current harmonic components,

4. calculation of the compensating current reference waveform for active power filter incorporating the recommendations as stipulated by the harmonic standards on the level of injected harmonics, and
5. generation of the PWM pattern and control of the inverter.

As shown in Figure 4.1, the inputs to the DSP based controller include; the measured load current (i_{load}), AC supply voltage (v_s), active filter current (i_{apf}) and voltage of the DC link (V_{dc}) of the inverter.

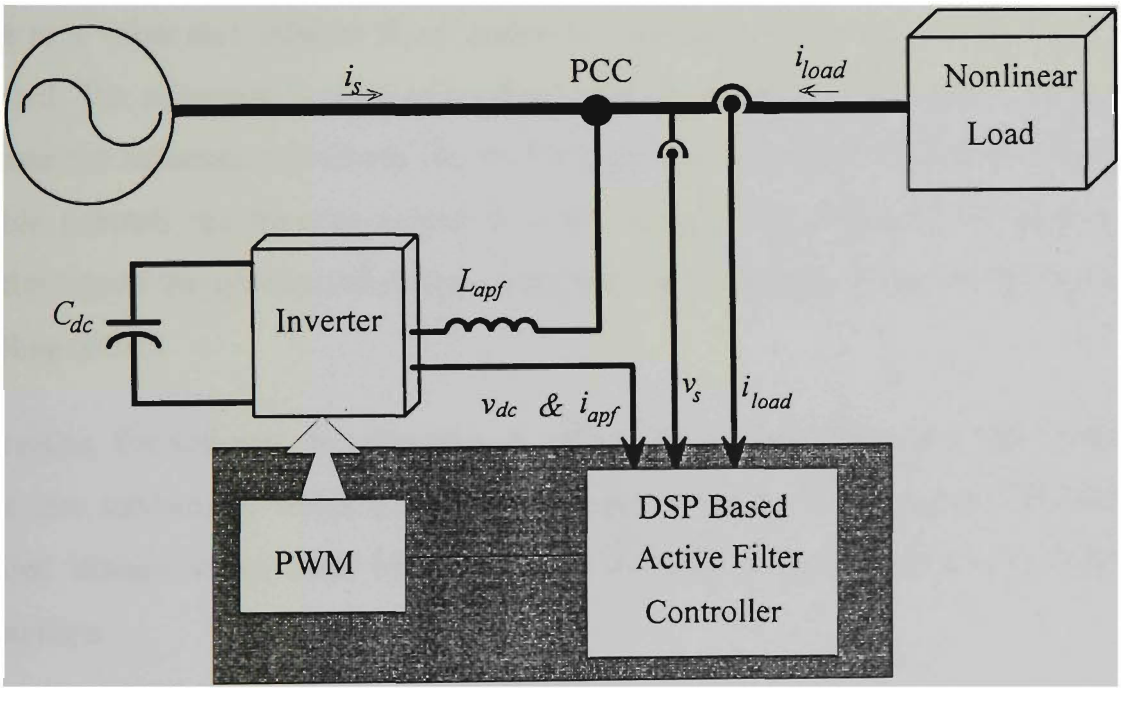


Figure 4.1: Functional block diagram of the proposed active power filter.

This Chapter is organised as follows: Section 4.2 discusses in detail the proposed control strategy for the active power filter. It includes the harmonic estimation, frequency tracking and reference waveform generation. In Section 4.3 the DSP implementation of the system, including data acquisition and digital filtering on the DSP are presented. Section 4.4 describes the hardware specification for the power circuit of the inverter including the PWM and protection system of the APF. Finally, the software simulation results on the developed prototype APF hardware are presented in Section 4.5.

4.2 CONTROL STRATEGY

The flowchart of the control strategy implemented on the DSP is shown in Figure 4.2. Control strategy is started by sampling the load current, supply voltage, active power filter and DC link voltage waveforms. The phase and frequency deviation of the supply voltage are estimated and applied to the harmonic estimation module. All integer-multiple harmonics of the supply frequency are estimated. The estimated harmonics are checked against the level set by the harmonic standard to be implemented [3, 5]. If the magnitude of harmonics exceed the recommended limits, then the level of compensation is set to a value that reduces those harmonics just below the limit as set out by the standard. The estimated harmonics together with the level of compensation are used to generate the reference waveform for the PWM pattern generator. The PWM switching module controls the inverter output in order to track the reference waveform. The inverter injects the synthesised reference current into the supply at the point of common coupling (PCC).

In practice, the software development of each section of this flowchart can be broken down into subroutines which can be individually tested to ensure correct operation. A detailed discussion of each block in the flowchart is presented in the following subsections.

4.2.1 Data Acquisition

The current and voltage input waveforms sampled by the DSP must be processed in real time for successful active filtering to occur. Therefore, the execution of control strategy software must be finished before the next samples are captured. Adhering to Nyquist's theorem, the signals must be sampled at twice the maximum frequency of interest that is present in the current waveform [70].

In order to match the power of the DSP for required calculation, the sampling frequency is set to be 64 samples per fundamental cycle. This gives a maximum sampling period of 316 μs (3200 Hz). During this period of sampling, the DSP can execute the frequency estimation module, harmonic estimation module and the PWM pattern generation. Following sections present the implementation of the frequency estimation, harmonic estimation and PWM switching.

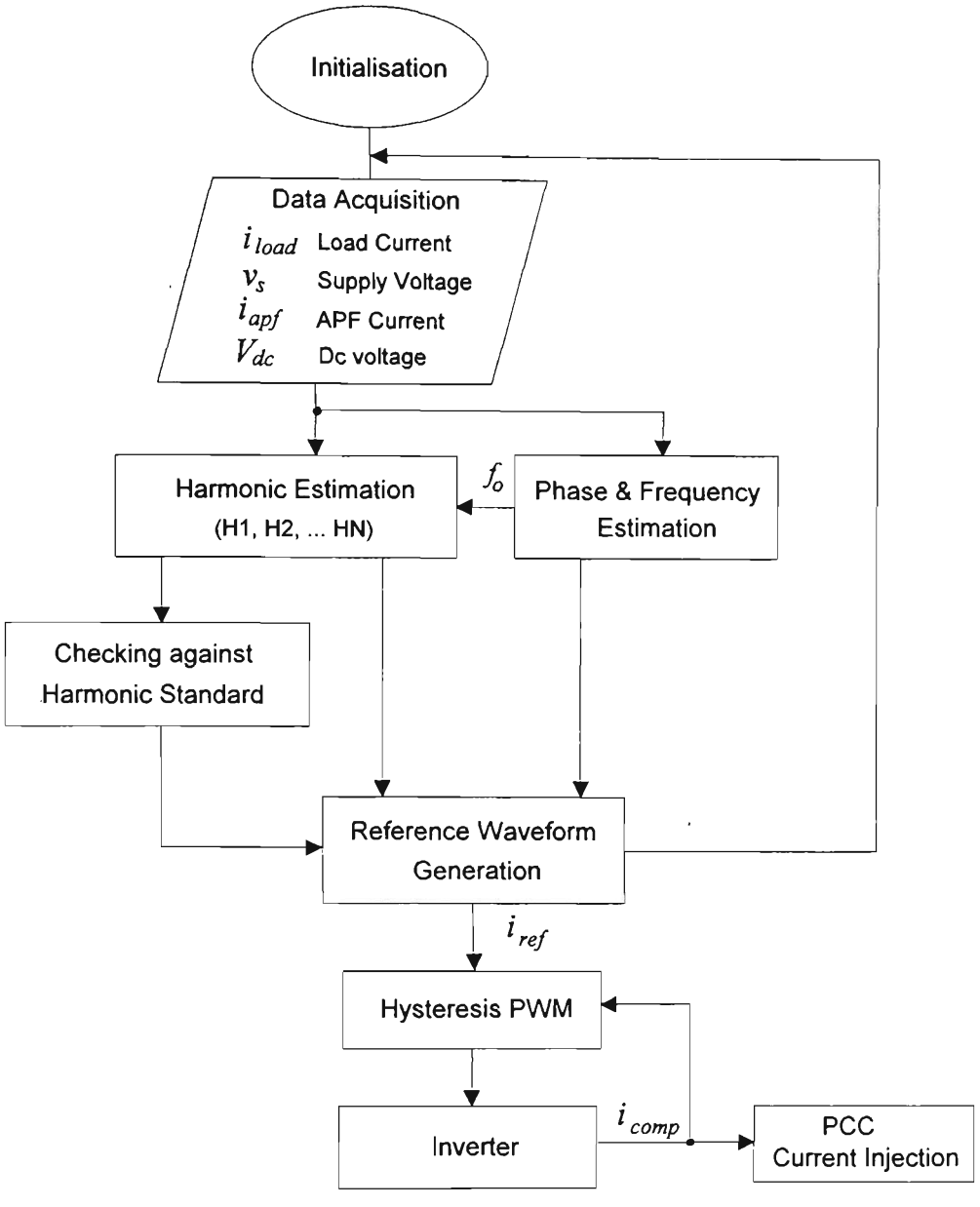


Figure 4.2: Flow chart of control strategy.

4.2.2 Frequency Tracking

As stated in the Chapter 3, two frequency estimation techniques were applied to the estimation of the phase and frequency variation of the supply voltage. The simulation results and comparison were provided to illustrate the performance of both algorithms in tracking the fundamental frequency for step and slow changes. The FM demodulation technique has been chosen for frequency tracking in this project due to its accuracy and fast response in time-varying situations.

To implement the FM demodulation frequency tracking shown in Figure 4.3 (also discussed in Section 3.4.2 of Chapter 3), two software based oscillators of the internal

clock of the DSP have been used. The outputs of the mixers are passed through programmable finite impulse response (FIR) low-pass filters to isolate the instantaneous phase of input signal.

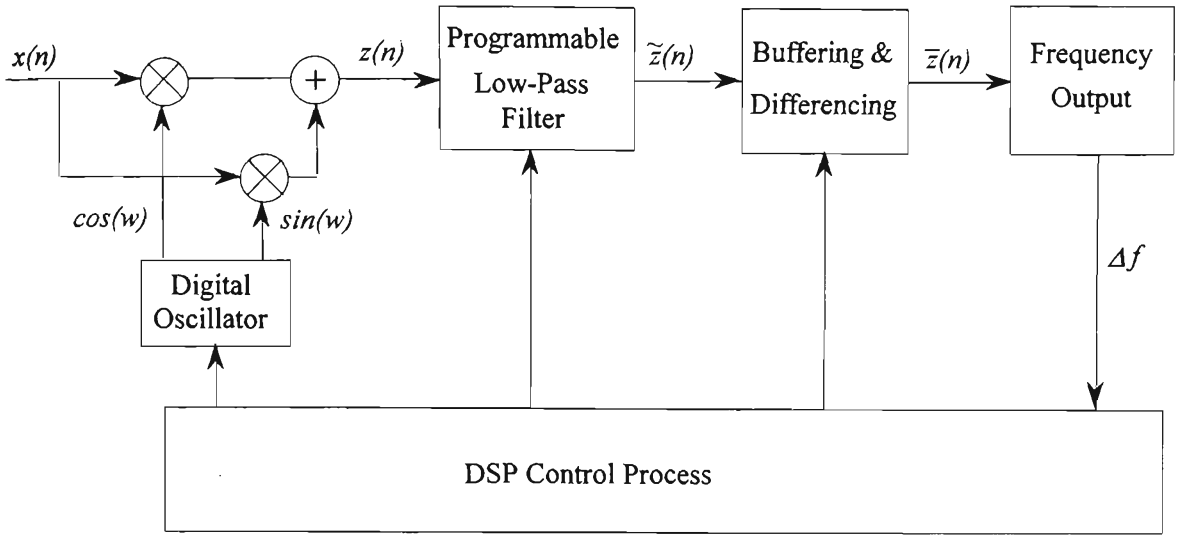


Figure 4.3: Digital FM demodulator.

4.2.2.1 FIR Filtering

In order to process the frequency tracking in real time, a reduction in the sampling rate is necessary. On the other hand, due to the possibility of aliasing, the reduced sampling rate must still meet the Nyquist's criteria. Therefore, the input signal should be low pass filtered before decimation.

To track the power system fundamental frequency, the voltage waveform is sampled at a sampling frequency of 800 Hz and then low pass filtered and decimated with the factor of 4. To implement the FM demodulation frequency tracking module an FIR filter design from MATLAB [58] was used to find the FIR filter coefficients. The order of the FIR filter is found to be 72 with a cut-off frequency (3 dB attenuation) at 20 Hz, and a rejection frequency of 45 Hz. The attenuation at 45 Hz is 80 dB.

The pseudo code of the implemented FM demodulation module is given in Appendix A. The code has been optimised to reduce the computational time as well as the memory storage of the programs.

4.2.3 Harmonic Estimation and Prediction

4.2.3.1 Harmonic Estimation

In this project, due to the sampling frequency of 3200 Hz, load current harmonic components at a maximum frequency of 1600 Hz can be retrieved. The bandpass filter parameters of IIR filters in filter bank are set to the frequency of corresponding harmonic component. The estimated frequency deviation from frequency tracking module is used to adjust the filter bank parameters. Any prior knowledge of the load current frequency characteristics such as frequency contents can be used to reduce the number of filters in the filter bank and consequently reduce the computational burden.

4.2.3.2 Harmonic Prediction

In implementing the proposed harmonic estimation on the DSP, it is exposed to a fundamental problem. That is, at the n^{th} sampling instant, the reference waveform for $(n+1)^{th}$ instant, $y_{ref}(n+1)$, is not available. In other words, the error between the n^{th} and $(n+1)^{th}$ reference current instants should be predicted using the present and previous reference values. The error between the n^{th} and $(n+1)^{th}$ instant for each harmonic can be regarded as the phase error or the delay of the associated filter in the filter bank. Then the phase error can be predicted for each harmonic individually. This phase error can be decomposed into sums of phase errors for all harmonic components. Consider the output of the filter bank:

$$\begin{aligned} y_{ref}(n+1) &= \sum_{k=1}^{N} c_k \cos(\omega_k (n+1) + \phi_k) \\ &= \sum_{k=1}^{N} c_k \cos(\omega_k n + \phi_k + \omega_k T_s) \end{aligned} \tag{4.1}$$

where T_s is the sampling period. Each harmonic in Equation (4.1) can be simplified as:

$$\begin{aligned} c_k \cos(\omega_k n + \phi_k + \omega_k T_s) = c_k \cos(\omega_k n + \phi_k) * \cos(\omega_k T_s) \\ - c_k \sin(\omega_k n + \phi_k) * \sin(\omega_k T_s) \end{aligned} \tag{4.2}$$

where $cos(\omega_k T_s)$ and $sin(\omega_k T_s)$ in Equation (4.2) can be accessed using look-up tables. Implementing this method on a DSP will result a reduction in execution time. The only calculations for each sampling instant are the calculation of the following terms:

$$c_k \cos(\omega_k n + \phi_k) \quad \text{and} \quad c_k \sin(\omega_k n + \phi_k) \tag{4.3}$$

where $c_k \cos(\omega_k n + \phi_k)$ is the measured harmonic waveform at the instant n and $c_k \sin(\omega_k n + \phi_k)$ is its derivative over the sampling period. A simplified version of the derivative of the sampled signal can be calculated at each sampling time as follows:

$$c_k \sin(\omega_k n + \phi_k) \approx c_k\left(\cos(\omega_k n + \phi_k) - \cos(\omega_k (n-1) + \phi_k)\right) * {}^{1}\!/_{\omega_k T_s} \tag{4.4}$$

Equation (4.4) can be implemented for every new sample with minimum computational burden. Equations (4.2) and (4.4) are valid when there is no sharp frequency or magnitude variation. Further reduction in computational burden can be achieved by performing the phase error correction only on dominant harmonic components.

4.2.3.3 IIR Filter Bank

The important parameters of each filter in the filter bank shown in Figure 4.4 are the centre frequency parameter *a*, and the gain of feedback loop, *g*. The parameter *g* can be chosen as a constant for a selected load taking into account the overall system performance including the response time of system and number of harmonic filters in the configuration. Furthermore, the residue signal, *e(n)*, can be further processed to find any particular interharmonic frequencies using the adaptive notch filtering technique as mentioned in Chapter 3.

The main part of the harmonic estimation module is the extraction of the *N* harmonics from the load signal. The residual signal, which may include noise, a DC component, sub-harmonics and interharmonics, corresponding to the $(N+1)^{th}$ output of the filter bank. The pseudo code for the harmonic estimation module is given in Appendix A.

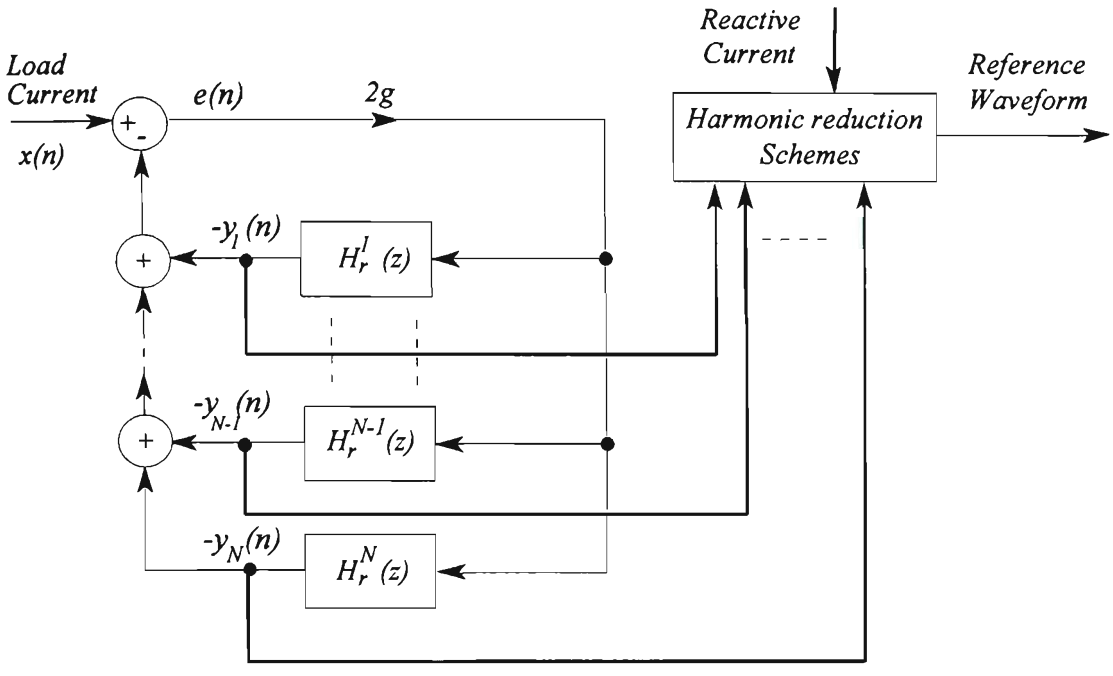


Figure 4.4: Filter bank harmonic estimation and generation of APF reference waveform.

4.2.4 Active Power Filter Reference Waveform

4.2.4.1 Power Calculation

The instantaneous power, p_{apf}, of the active power filter can be expressed as follows:

$$p_{apf}(t) = i_{apf}(t) * v_s(t) \tag{4.5}$$

This power includes the compensation power which is reactive and the switching losses of the inverter. When the AC supply voltage, v_s, contains harmonic components, the total active power delivered from the active power filter is increased due to the active power corresponding to these harmonic components.

The Fourier series of the load current and supply voltage can be given as:

$$i_{load}(t) = \sum_{n=1}^{\infty} i_n \; ; \quad v_s(t) = \sum_{n=1}^{\infty} v_n \tag{4.6}$$

where v_n and i_n, are the harmonic components given by:

$$v_n = \sqrt{2} V_n \sin(\omega_n t + \phi_n) \tag{4.7}$$

$$i_n = \sqrt{2} I_n \sin(\omega_n t + \delta_n) \tag{4.8}$$

The instantaneous power of the load can be expressed as:

$$p(t) = v_s(t) * i_{load}(t) \tag{4.9}$$

$$p(t) = v_s(t) * i_{load}(t) = \sum_{n=1}^{\infty}\sum_{m=1}^{\infty} 2V_n I_m \sin(\omega_n t + \phi_n) * \sin(\omega_m t + \delta_m) \tag{4.10}$$

where $p(t)$ can be separated into average, $\bar{p}$, and oscillatory, $\tilde{p}$, components.

$$p(t) = \bar{p} + \tilde{p}(t) \tag{4.11}$$

$$\bar{p} = \sum_{n=1}^{\infty} V_n I_n \cos(\phi_n - \delta_n) \tag{4.12}$$

$$\tilde{p}(t) = \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} V_m I_n \cos\left((\omega_m - \omega_n)t + \phi_m - \delta_n\right)\right] + \sum_{m=1}^{\infty}\left[\sum_{n=1}^{\infty} -V_m I_n \cos\left((\omega_m + \omega_n)t + \phi_m + \delta_n\right)\right] \tag{4.13}$$

Usually, the level of harmonics in the supply voltage of a power system network is low and are below the values recommended by the relevant harmonic standards. However, when the supply voltage is distorted a series active power filter is required to filter the supply voltage harmonic components. Thus, the only power delivered by the active power filter to the power system would be the oscillatory component with zero average $\tilde{p}$ and the switching losses of the active filter power.

4.2.4.2 DC Link Voltage Controller

Normally active power filters deliver only reactive power to the power system as the background voltage distortion on mains network is very small. The switching losses and other losses cause a voltage reduction on the DC link capacitor. Therefore, the reference current waveform for active power filter, $i_{ref}(t)$, includes harmonic of the load current, $\sum_{h}^{N} i_h(t)$, the reactive current of the load, $i_{reactive}(t)$, and the current required to compensate for the voltage reduction in the DC link capacitor, $i_{losses}(t)$. Therefore:

$$i_{ref}(t) = i_{reactive}(t) + \sum_{h=1}^{N} i_h(t) + i_{losses}(t) \tag{4.14}$$

The DC bus stabiliser maintains a specified voltage level across the capacitor in order to follow the reference current control. The average energy loss in the DC link capacitor due to the inverter switching losses in one fundamental period can be determined as:

$$\Delta e = \tfrac{1}{2} C_{dc}\left[V_{dc\_ref}^2 - V_{dc}^2\right] = \tfrac{1}{2} I_{losses} * V_s * T_s \tag{4.15}$$

$$I_{losses} = C_{dc}\left[V_{dc\_ref}^2 - V_{dc}^2\right] / V_s * T_s \tag{4.16}$$

where I_{losses} is the magnitude of $i_{losses}(t)$ in Equation (4.14) can be easily used to drive an expression for i_{losses} as the losses in the switches correspond to an in phase current with respect to the fundamental supply voltage.

4.2.5 Harmonic Compensation Schemes

The reference current waveform for the active power filter can be constructed from the estimated harmonics. The order and the magnitude of the harmonics in the reference waveform is determined by the adopted harmonic compensation scheme. There are many different control methodologies that can be used to generate the active power filter reference current. They are distinguished by how the current reference signal for the harmonic compensation is derived from the measured quantities. Three harmonic compensation schemes have been employed in this project. These are full, selective and harmonic standard based compensation schemes.

4.2.5.1 Full Compensation Scheme

In the full compensation scheme the active power filter reference waveform, $i_{ref}(t)$ includes all retrieved harmonics from the harmonic estimation module for compensation. It can also include the reactive power for power factor correction. The reference waveform for full compensation scheme can be calculated as:

$$i_{ref}(t) = K_{reactive} * i_{reactive}(t) + \sum_{h=2}^{N} i_h(t) \tag{4.17}$$

where $K_{reactive}$ is a constant which controls the level of fundamental reactive power compensation.

4.2.5.2 Selective Harmonic Compensation Schemes

In selective harmonic compensation schemes, the most important and dominant low order harmonics can be chosen to be compensated. In these schemes the APF reference waveform is determined as follow:

$$i_{ref}(t) = K_{reactive} * i_{reactive}(t) + \sum_{h=j}^{N} i_h(t) \qquad (j = j_1, j_2, j_3, j_4, \cdots) \qquad (4.18)$$

where $j_1, j_2, \ldots j_M$ are the order of the selected harmonic components for compensation.

4.2.5.3 Compensation Based On Harmonic Standards

In compensation schemes based on harmonic standards, all the load harmonic components are reduced to a level allowed by the harmonic standards. In other words, all harmonic components are subject to a reduction up to the value that is given by the harmonic standards.

The magnitude of each estimated harmonic waveform is compared against the recommended values by harmonic standard. If they exceed the recommended values they will be reduced to those values. The active power filter reference waveform is calculated as follows:

$$i_{ref}(t) = K_{reactive} * i_{reactive}(t) + \sum_{h=2}^{N} I_h^{ref} * i_h(t) \qquad (4.19)$$

where I_h^{ref} is the reference load current weighting for each harmonic component and is determined as follows:

$$\begin{aligned} &if\,(I_h > K_h^{std} * I_1)\ \ then \\ &\qquad I_h^{ref} = (1 - \frac{K_h^{std} * I_1}{I_h}) \\ &else \\ &\qquad I_h^{ref} = 0.0 \end{aligned} \qquad (4.20)$$

where K_h^{std} is the recommended value for h^{th} harmonic component which is allowed in the supply system. I_h is the estimated magnitude for h^{th} harmonic order.

To find the value of K_h^{std} for harmonic current distortion, the impedance of a supply system should be determined. This impedance depends upon the frequency of the current flowing, the resistance, inductance and the capacitance of the system, and the connected loads. When the information is not available on system impedances, it is assumed that the system impedance is inductive and hence directly proportional to frequency, and that there are no resonance effects [4]. The guidelines for the calculation of the K_h^{std} for DC drives is given in Appendix C [4].

4.2.5.4 PWM Waveform Generation

Once the reference waveform is calculated, the PWM switching pattern for the inverter can be generated using a hysteresis current-controlled PWM technique. In this technique the PWM waveform is generated by comparison of the inverter current with the reference current. The frequency of switching depends on the sampling frequency and the magnitude of the isolation inductance in the output of APF. Rate of change of the reference current waveform should be less than that of the APF output circuit, so that effective current injection is possible.

In PWM applications, increasing the inverter operating frequency helps to get a better synthesised current waveform. However, the actual performance of the active filter becomes limited by the isolation inductance once a sufficiently high switching frequency is achieved.

Figure 4.5 shows the hysteresis current control employed in this project. The hysteresis band of the PWM switching strategy is described as:

$$\begin{aligned} &if\ (i_{comp}(t) - i_{ref}(t)) > \Delta I_{high} \quad then \\ &\quad S_{11} = S_{22} = 0, \quad S_{21} = S_{12} = 1; \\ &if\ (i_{comp}(t) - i_{ref}(t)) < -\Delta I_{low} \quad then \\ &\quad S_{11} = S_{22} = 1, \quad S_{21} = S_{12} = 0; \end{aligned} \tag{4.21}$$

In Equation (4.21), $i_{ref}(t)$ is the desired compensation current reference signal and i_{comp} is the actual inverter output current. When the error between the i_{ref} and i_{comp} is positive and exceeds the upper boundary, ΔI_{high}, of a specified hysteresis band, the comparing unit output goes high, firing the upper switches of the inverter leg. When I_{comp} becomes

greater than i_{ref} and the error exceeds the lower boundary, ΔI_{low}, of the hysteresis band, the comparing unit goes low, firing the lower switches of the inverter leg. The analogue interpretation of the method described by Equation (4.21) can be readily implemented on a DSP.

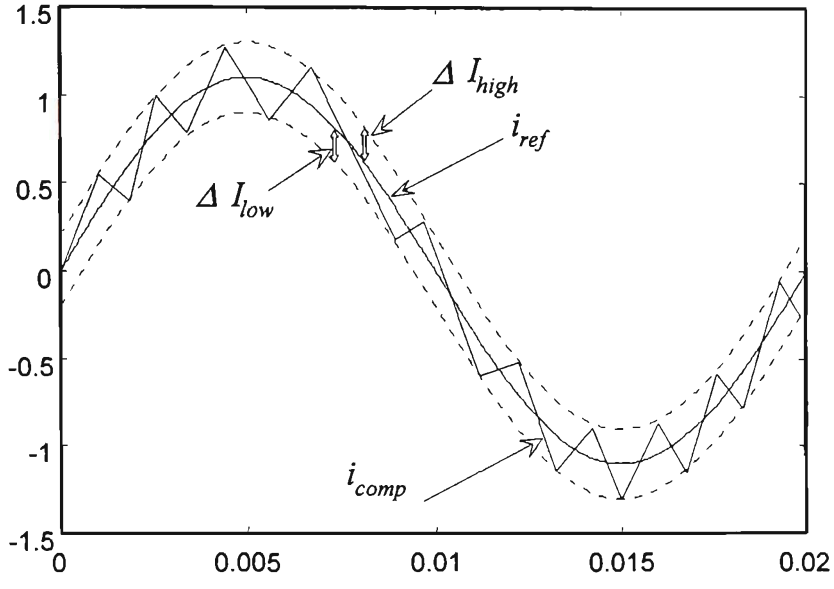


Figure 4.5: Hysteresis current control.

4.3 HARDWARE CONFIGURATION

Physically, the prototype system is partitioned into 4 separate boards according to their functions. These boards are the IGBT switches, the IGBT drivers, the current and voltage data acquisition and the DSP board controller which is housed in a personal computer.

The circuit diagram of the proposed active power filter is shown in Figure 4.6. The capacitor and inductance on the load side are employed to establish a nonlinear load. The inverter consists of two IGBT modules, the gate drive interface circuitry and the protection circuitry. The inverter is a voltage-source (VSI) type. The PWM current control as given by in Equation (4.21) forces the VSI inverter to behave as a controlled current sources.

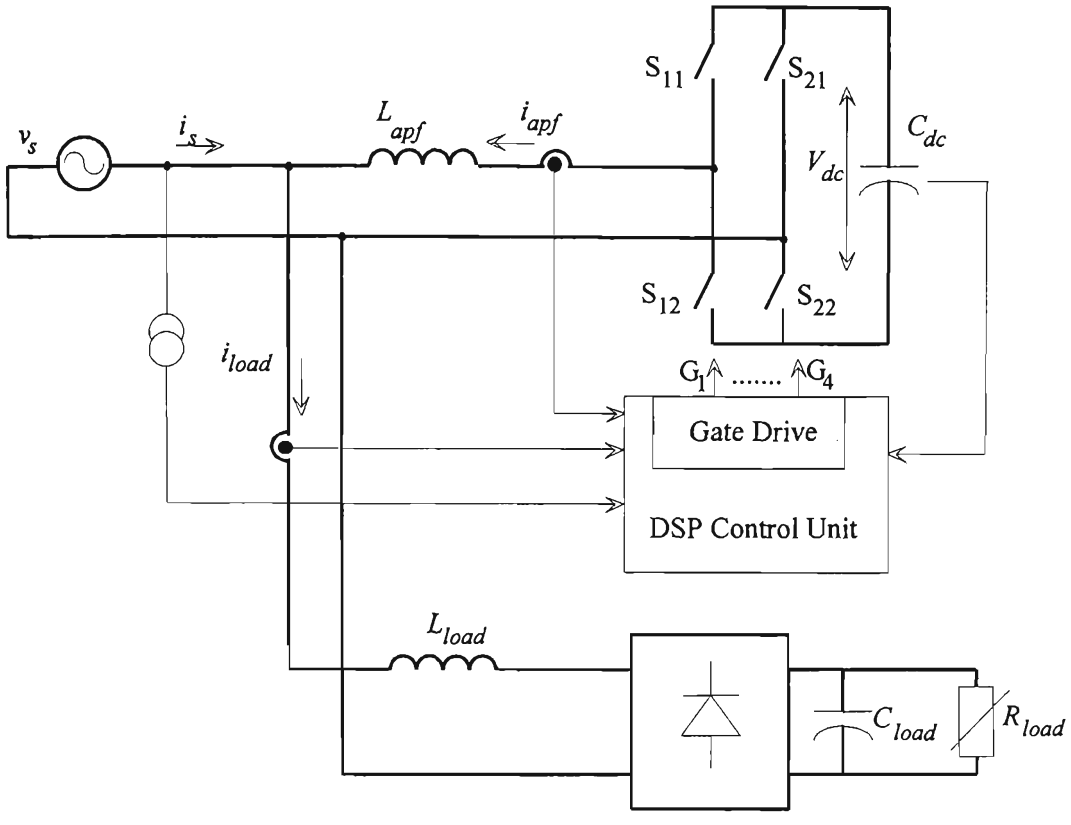


Figure 4.6: The circuit diagram of the proposed active power filter.

4.3.1 IGBT Voltage Source Inverter

A single-phase, full-bridge inverter is built using two identical IGBT inverter poles. Each pole of the inverter consists of IGBTs with free-wheeling diodes packed in one module from SEMIKRON [86]. These modules are capable of carrying up to 50 A at 600 V. A hybrid double IGBT driver is used for each pair of IGBT inverter modules. The driver comprises the pulse generator as well as short circuit current protection for the two IGBTs in a half bridge connection.

4.3.1.1 Isolation Inductance

In Figure 4.6 the isolation inductance, L_{apf}, provides the isolation and filtering between the output of the voltage source inverter and the power system where the active filter is connected. The isolation inductance allows the output of the active filter to look like a current source to the power system. It also makes it possible to charge the DC capacitor to a voltage greater than the peak value of the AC supply voltage. The isolation inductance also functions as a commutation impedance. It limits the magnitude of current transients during commutation and prevents the semiconductor switching devices from seeing an excessive rate of current change.

A large isolation inductance will reduce the switching frequency of the hysteresis current-controlled PWM. An L-C combination filter can be used to remove the high frequency components of the active power filter current in the output of the active filter circuit.

4.3.1.2 Current Sensing

A multi-range Hall effect current transducer senses the load and inverter currents [87]. A schematic diagram of the current sensing and conditioning circuitry using this module is shown in Figure 4.7. The output of the module is a current that is converted to a voltage by the measuring resistor R1. This voltage is followed by an active amplifier that has two functions. First, it amplifies the voltage to a level suitable for the ADC by adjusting the resistor R6. The second function of the amplifier is to provide a zero adjustment to eliminate any possible DC offset through potentiometer R3 since the system performance is degraded by any DC offset.

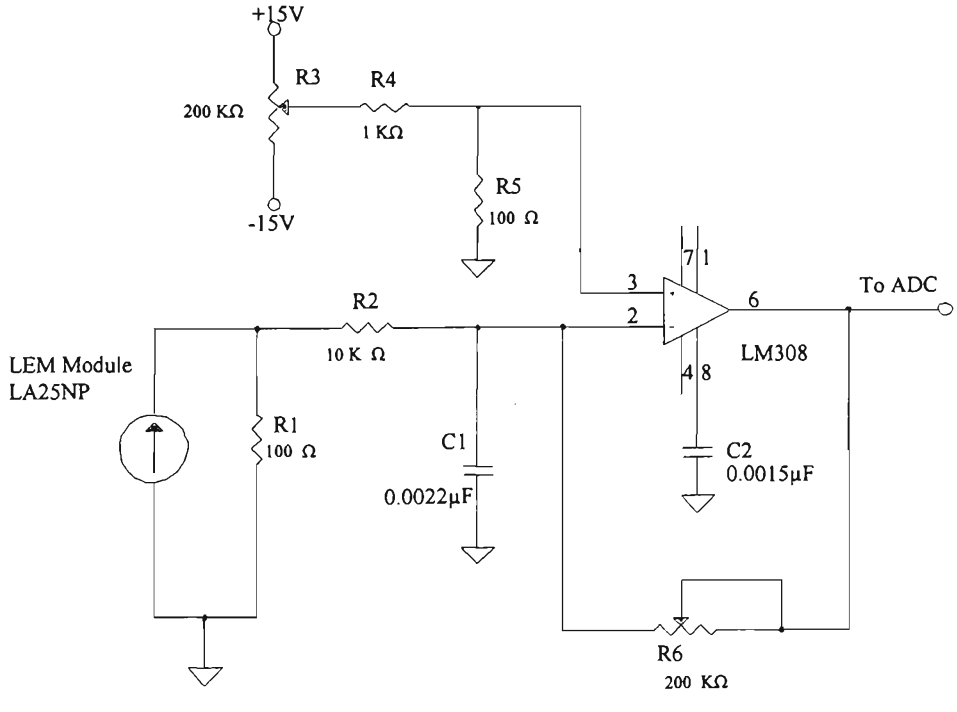


Figure 4.7: The schematic diagram of the current sensing and conditioning circuitry.

4.3.1.3 Voltage Sensing

A Hall effect voltage transducer is used which is a transducer for the measurement of voltages and provides galvanic isolation between the primary (high voltage) and the secondary (electronic) circuits [88]. For this device, to measure the input voltage, a current proportional to voltage should be collected through an external resistor which is

installed in series with the primary circuit of the transducer as shown in Figure 4.8. The rest of the voltage sensing circuit is similar to the current sensing circuit shown in Figure 4.7.

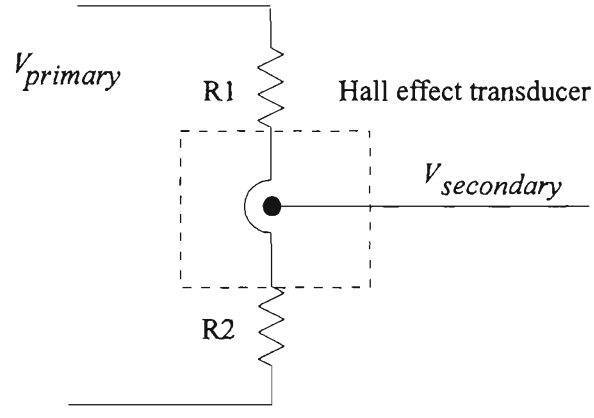


Figure 4.8: The schematic diagram of the voltage attenuation circuit.

4.3.2 DSP Hardware

Extensive calculations required for each part of the proposed strategy needs a powerful computational platform. A digital signal processor (DSP) is the most promising option when cost and ease of implementation are considered.

4.3.2.1 DSP Configuration

A ADC64 PCI Bus DSP Data Acquisition Card has been used in this project [89]. The ADC64 is a PCI Bus compatible DSP data acquisition card incorporating a Texas Instruments TMS320C32 [90] floating point DSP processor. The ADC64 is hosted in an IBM personal computer.

The prominent features of this ADC64 DSP system include 30 ns per instruction execution time, 16 bit analog input/output capability, 16 bits of digital input/output capability and 512K bytes on-board SRAM for storing the program and data.

4.3.2.2 Data Acquisition

Two channels of the digital to analog converter (DAC) are used for monitoring purposes. The DACs used are 16-bit DAC0800, interfaced to the ADC64 DSP through an Input/Output (I/O) port B.

There are 8 analog to digital convertors (ADCs) on the ADC64 which may be triggered to sample simultaneously. Four channels of these ADCs are used to obtain samples of the load current i_{load}, the DC link voltage V_{dc}, the active filter current i_{comp}, and the source voltage, v_s. These ADCs are interfaced to the ADC64 system through the memory mapped peripheral connector. The ADC used in the DSP board are 16-bit ADS7805 which have a normal input range from +10V to -10V. The block diagram of the interfacing ADC is shown in Figure 4.9.

The decoded addresses for ADC0, ..., ADC3 (corresponding to channel 1,2,...,8) start from 0x810000 up to 0x810003. Four digital outputs (DIO1, .., DIO4) are used to output the pulsewidth of the hysteresis PWM patterns from the DSP to the IGBT gate drivers.

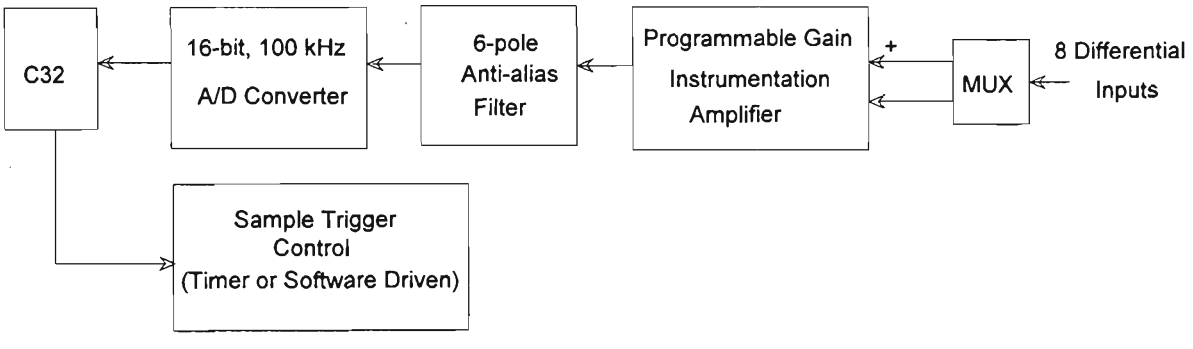


Figure 4.9: Block diagram of ADC64 data acquisition system.

4.4 SOFTWARE SIMULATION

In order to predict and investigate the behaviour of the proposed active power filter hardware, the Simulator for Power Electronic Circuits and Systems (SPECS) program has been used [91]. The availability of a micro-controller in this software enables a designer to implement most of the programming on the DSP or real micro-controller in software simulations. Figure 4.10 shows the simulated active power filter circuit on SPECS program. Ideal switches have been used for simulation of IGBTs in the inverter. The losses in inverter switches are simulated using a resistor connected across the DC link capacitor.

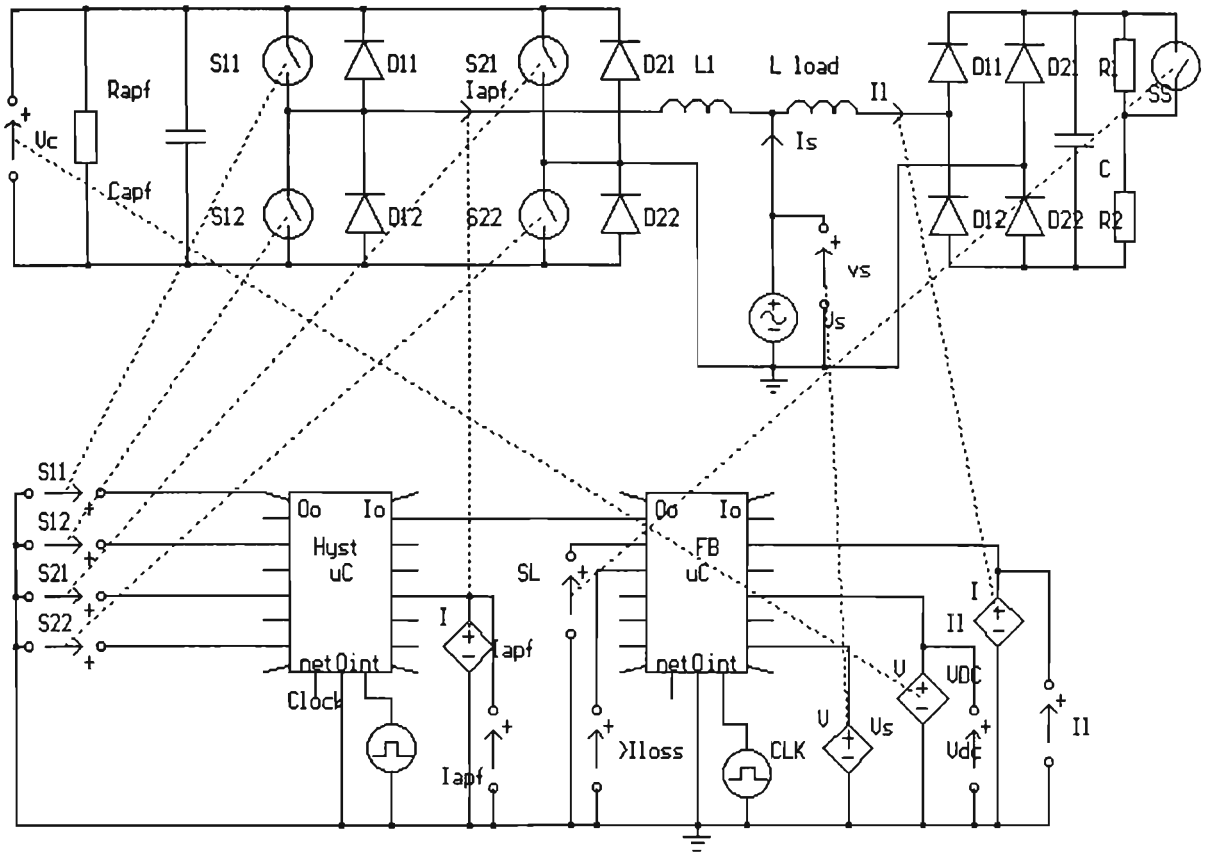


Figure 4.10: The simulated hardware on SPECS.

As in real hardware, the load and supply currents in the simulation are detected and converted to a voltage to be applied to the DSP or micro-controllers. The listing of the micro-controller programs are given in Appendix B. The parameters of the simulated system are given in Table 4.1.

Table 4.1: The simulated system parameters.

Load		**Active power filter**	
L_{load}	10 mH	L_{apf}	8 mH
R_{load}	20 Ω	$V_{dc\text{-}ref}$	110 V
C_{load}	200 μF	C_{dc}	4400 μF
f_o	50 Hz	f_{sw}	3200 Hz

The value of the isolation inductance has been determined based on the maximum *di/dt* of the load current and the maximum switching frequency of the hysteresis current-controlled PWM technique. This value is equal to the value used in the actual hardware. Both the harmonic estimation and PWM switching strategy have been programmed into the micro-controllers.

4.4.1 Steady State Condition

Figure 4.11 shows the active power filter performance for full harmonic compensation scheme. It shows the DC link voltage, V_{dc}, the source current, i_s, the load current, i_{load}, and the APF compensating currents, i_{apf}, in steady state.

Figure 4.11 shows that the proposed control strategy is capable of compensating for the harmonic components in steady state. It is clear that the DC link voltage is effectively controlled. Figure 4.12 shows the frequency spectrum of the DC link voltage. The 100 Hz and 200 Hz harmonic components corresponding to the voltage ripple on DC link are seen to be under of 2%.

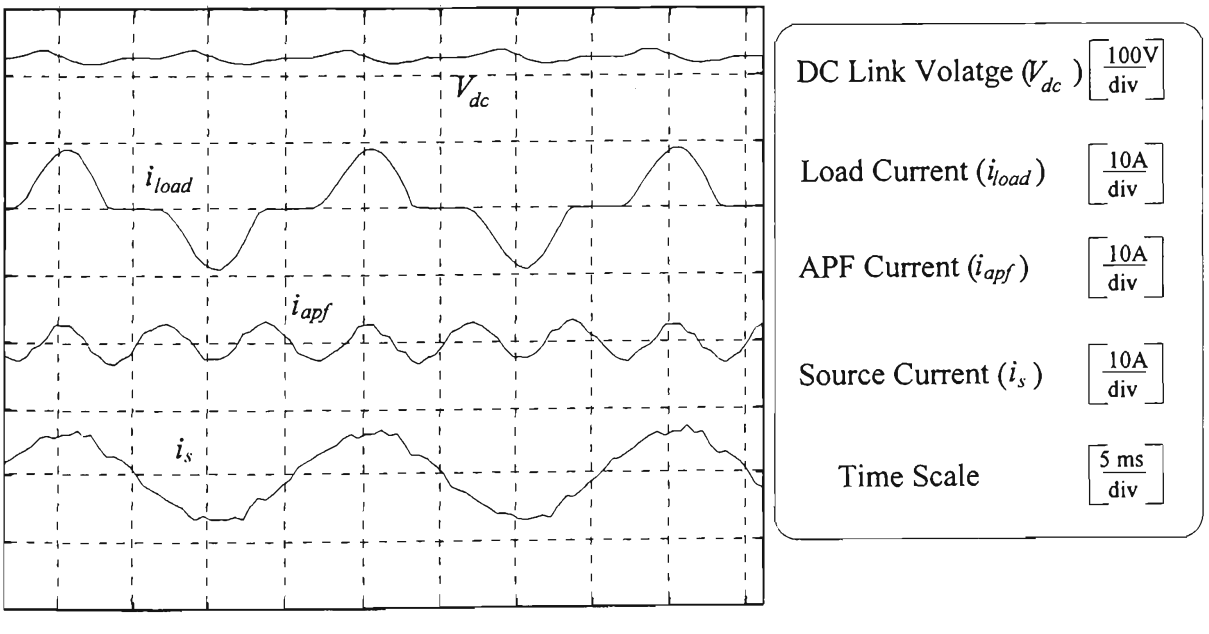


Figure 4.11: The steady state performance of active power filter.

Figures 4.13, 4.14 and 4.15 show the harmonic spectra of the load, source and active filter current waveforms respectively. Figure 4.13 shows harmonics in the load current up to 32nd harmonic. Figure 4.14 shows that the APF is capable of effectively eliminating of the low order harmonics. The THD of the AC source current is reduced from 47.84% to 8.67% after compensation.

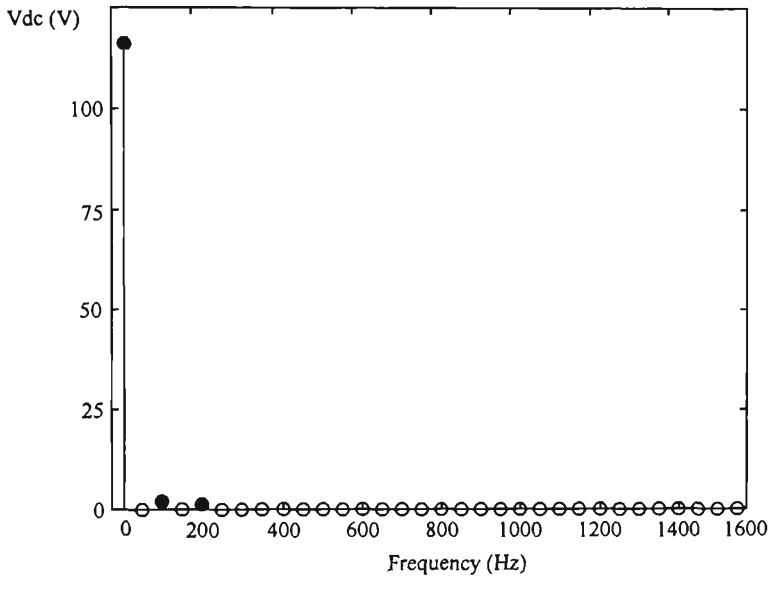


Figure 4.12: DC link voltage frequency spectrum.

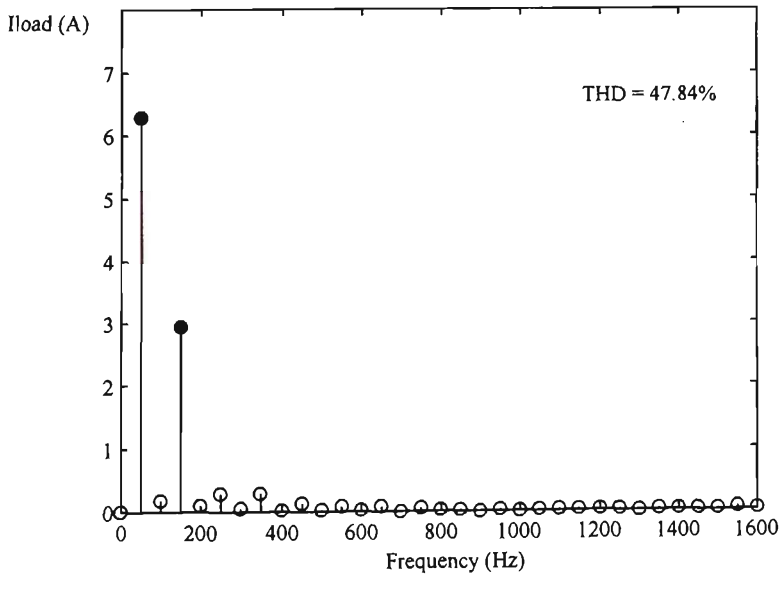


Figure 4.13: Load current frequency spectrum.

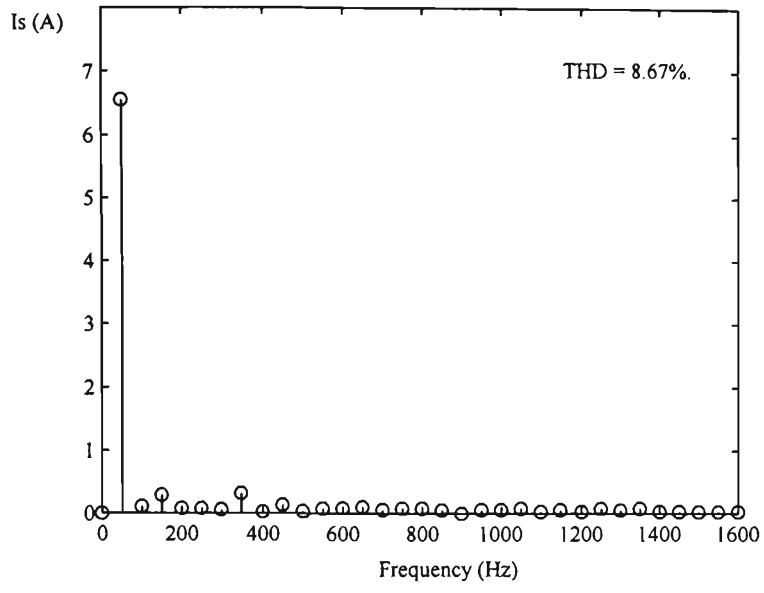


Figure 4.14: AC supply source current frequency spectrum after compensation.

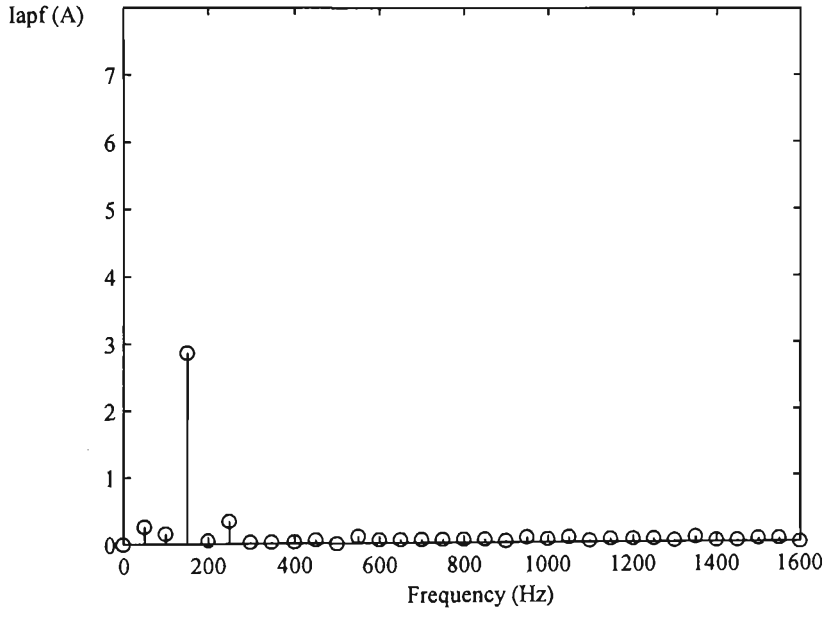


Figure 4.15: Active power filter current frequency spectrum.

4.4.2 Transient Condition

Figure 4.16 shows the performance of the APF following an increase of 30% in the load current. Following this disturbance, the steady state condition is reached within one cycle. The APF current increases to supply the increased load current demand by taking the energy instantaneously from DC bus capacitor. The DC bus capacitor voltage recovers within three cycles. The ripple in the DC bus capacitor voltage is quite small and can be reduced further by increasing the capacitor value if necessary.

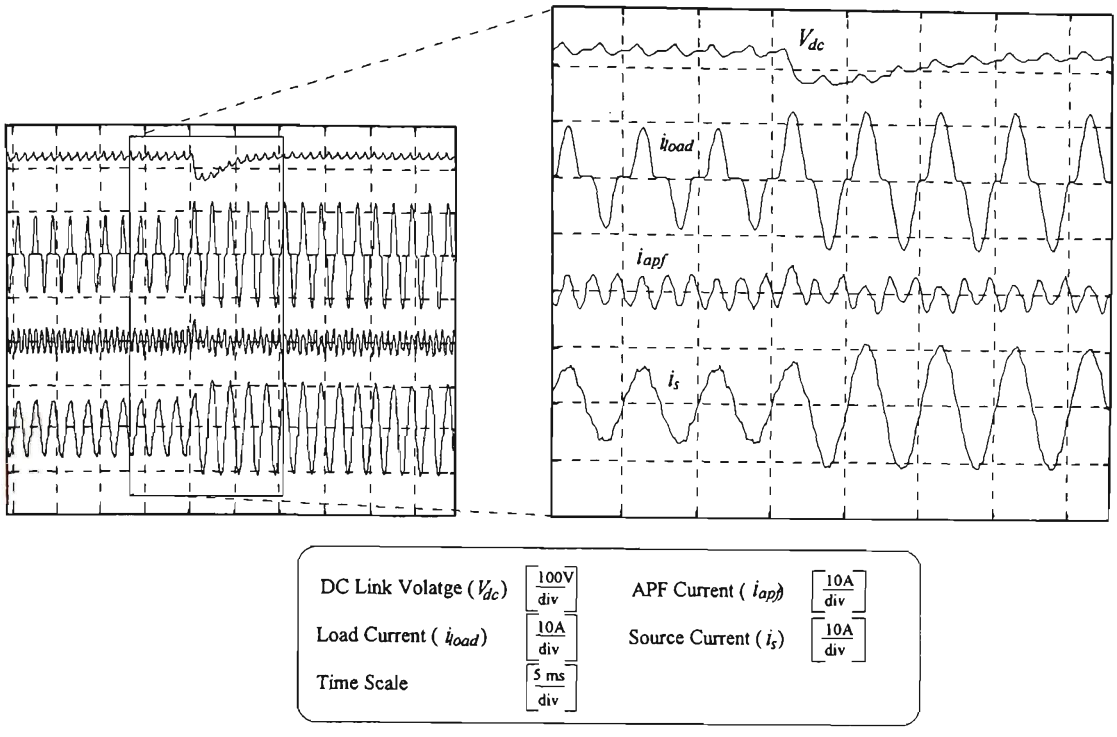


Figure 4.16: Transient performance of active power filter after a load change.

4.5 CONCLUSIONS

This Chapter presented the detail implementation of a new control strategy for active power filters (APF). The proposed control strategy included frequency tracking, harmonic estimation and harmonic reduction schemes. Some important technical issues regarding the implementation of the proposed control strategy on a DSP platform have been presented. A phase prediction method has been incorporated within the harmonic estimation module to compensate for the phase error of each estimated harmonic due to the computational delay and data acquisition system. The phase prediction technique corrects the reference current waveform by predicting the individual harmonic waveform so that the APF output current can be as close to its reference as possible.

Three harmonic reduction schemes; namely full, selective and partial harmonic compensation, for the calculation of the APF reference current have been considered. The selective and partial harmonic reduction schemes are designed to reduce the harmonic components of the load up to recommended values set by harmonic standards.

The APF reference current is determined from estimated harmonic components of the load current after applying one of the proposed harmonic reduction schemes. It further includes reactive compensation current and DC link voltage stabiliser control.

Some technical issues related to the laboratory prototype active power filter hardware design and the DSP implementation of the proposed control strategy have been discussed. A hysteresis based PWM current control is employed to generate the switching signals for the APF inverter. A single-phase diode rectifier with a capacitor input filter supplying a resistive load is used as a non-linear load in the simulation of the prototype hardware. Simulation results of the prototype APF have been presented to confirm the effectiveness of the new control scheme for the steady state and transient conditions. The source harmonic current components are effectively reduced and the dynamic response of DC link voltage control loop was shown to be satisfactory.

CHAPTER 5.

EXPERIMENTAL RESULTS

5.1 INTRODUCTION

In Chapter 3, harmonic estimation and frequency algorithms have been developed for harmonic estimation and measurement of the nonlinear load current. Simulation results were provided to illustrate the effectiveness of the algorithms in the estimation of the frequency components of a time-varying input signal. Even though the simulation results of the proposed control strategies are expected to closely represent the actual behaviour, they should be verified through experimental results. The experiments are performed to demonstrate the feasibility of the proposed method and to examine the theoretical results.

In this Chapter the results presented in Chapters 2 and 3 are verified based on the prototype active power filter implemented in Chapter 4. The test conditions maintained for verifying the proposed PWM switching technique and the proposed active power filter control strategy are presented in Section 5.1.1. Section 5.2 presents the experimental results for the proposed equal area based PWM (EAPWM) switching technique for synthesising a sinusoidal waveform. The experimental results for the harmonic estimation and the frequency tracking in the steady state and transient situations are presented in Section 5.3. Performance of the active power filter for selective and partial harmonic reduction schemes are given in Section 5.4.

5.1.1 Test Conditions

A shunt active power filter circuit has been set up to evaluate both the proposed PWM switching strategy, EAPWM, and the proposed active power filter (APF) control strategy. A single-phase inverter with IGBT switches rated at 600 V (DC) and 50 A is used in these experiments.

The EAPWM is only tested for the inverter applications with fixed load. The main reason for this is the limited computational capability of the DSP board in handling the control strategy and PWM pattern generation in a time varying conditions. Note that EAPWM has been evaluated via simulation and shown to yield improved performance for both fixed and variable load conditions.

5.2 Equal Area Based PWM Technique (EAPWM)

The experimental verification of the proposed switching strategy was carried out on the inverter used in the APF circuit after making some modifications. The block diagram of the test system is shown in Figure 5.1. In this configuration, the output of the inverter is connected to an R-L load and the inverter is supplied by a diode rectifier with capacitor filter.

The DSP controller shown in Figure 5.1 consists of several functional blocks. The PWM generation module is implemented with TMS320C32 processor. The PWM patterns are stored in RAM. The time resolution of the PWM pattern is 78 μs which is equal to 256 PWM points per cycle. For on-line operation, the PWM patterns can be recalculated and stored in memory using a given modulation index (M) and a switching frequency ratio (p). Table 5.1 lists some of the parameters of the constructed PWM inverter system and load.

The EAPWM switching strategy is implemented using C language on DSP platform. The pulsewidths and positions are calculated for a given switching frequency ratio and the modulation index. The calculated PWM patterns are stored in a look-up-table (LUT) and used to control the switches in the inverter. The PWM pattern stored in LUTs can be updated every cycle for new values of the fundamental frequency, the modulation index and the switching frequency ratio.

Table 5.1: Load and Inverter filter data.

Load		**Inverter**	
L_{load}	10 mH	L_{apf}	10 mH
R_{load}	30 Ω	V_{dc}	100 V
f_o	50 Hz	C_{dc}	4400 μF
V_s	80 V	f_{sw}	200-1000 Hz

The switching sequences proposed in Chapter 2 are applied on the PWM patterns to reduce the switching losses in the IGBTs. The IGBT switches, S_{22} and S_{12} (designated slow switches) are switched with line frequency (f_o =50 Hz) and the switches S_{11} and S_{21} (designated fast switches) with the frequency of PWM ($f_{sw}=p * f_o$).

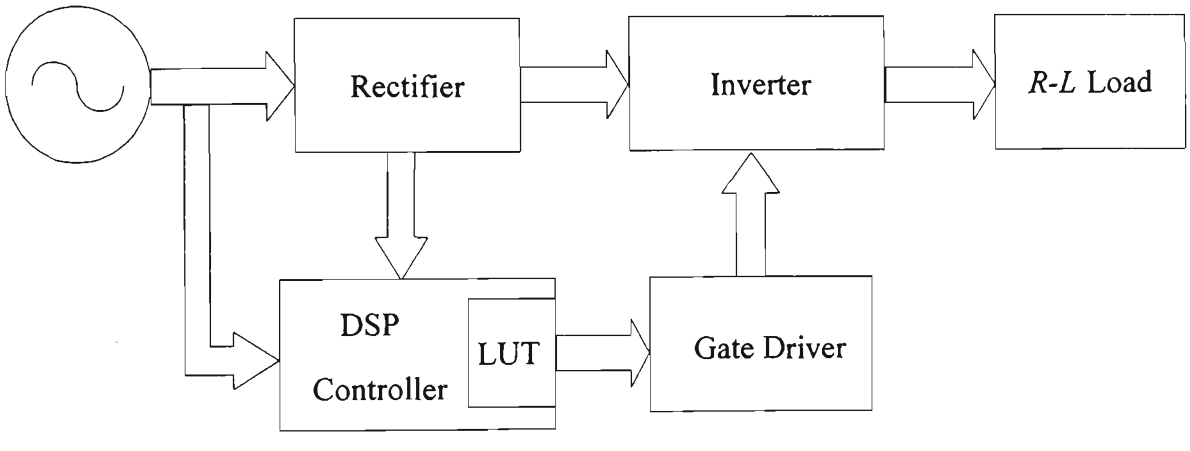


Figure 5.1: The schematic of the EAPWM test configuration.

5.2.1 PWM Operation

Figure 5.2 shows the experimental results for two selected switching frequency ratios which were used to produce simulation results of Chapter 2. The modulation index M is set to 1 which gives the maximum pulsewidth without pulse overlapping. The ripple (distortion) of the inverter current output is naturally higher for the lower switching frequency (Figure 5.2-b). The low pass filtering characteristics of the R-L load is

another important factor for the reduction of the harmonic distortion in inverter output current.

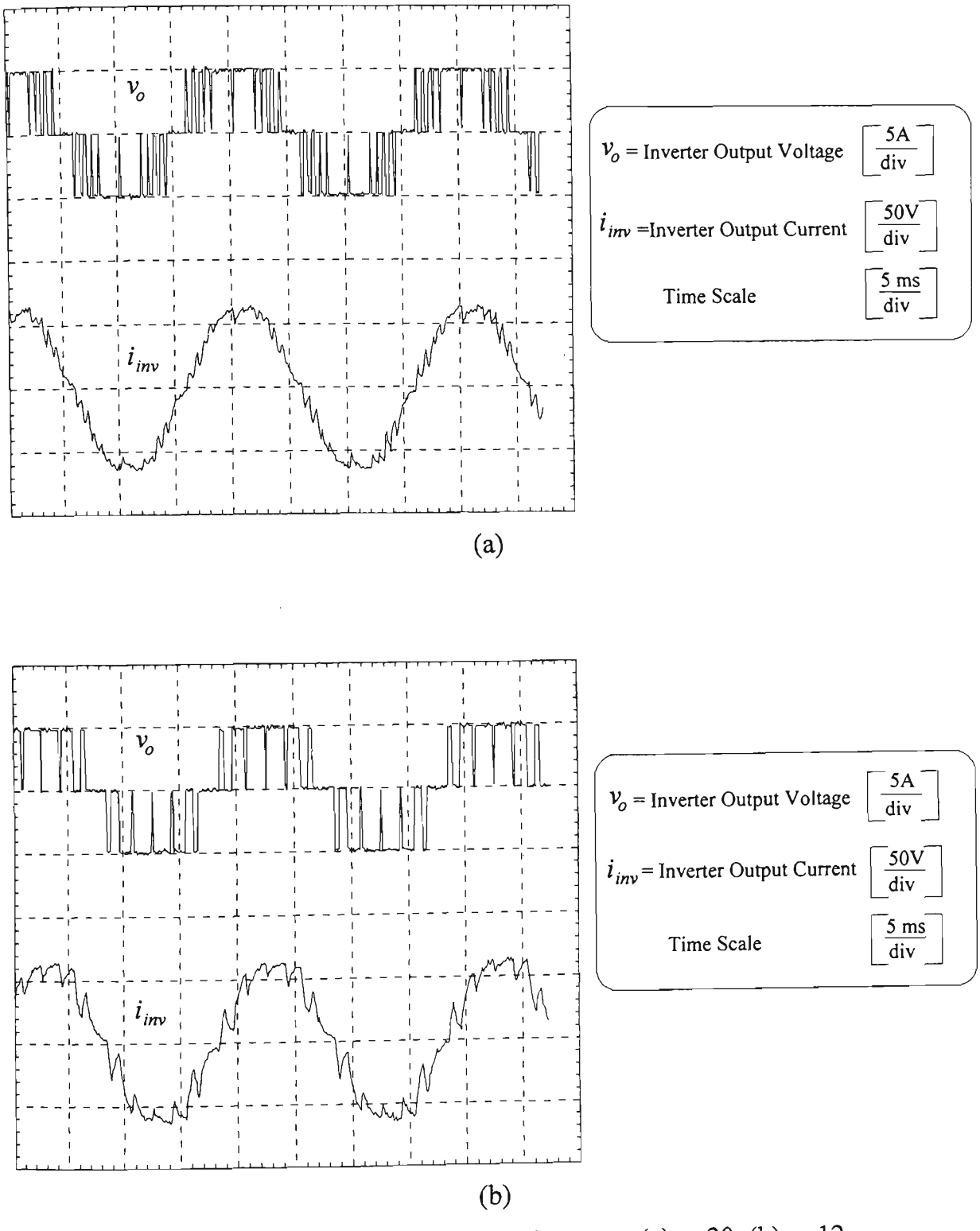
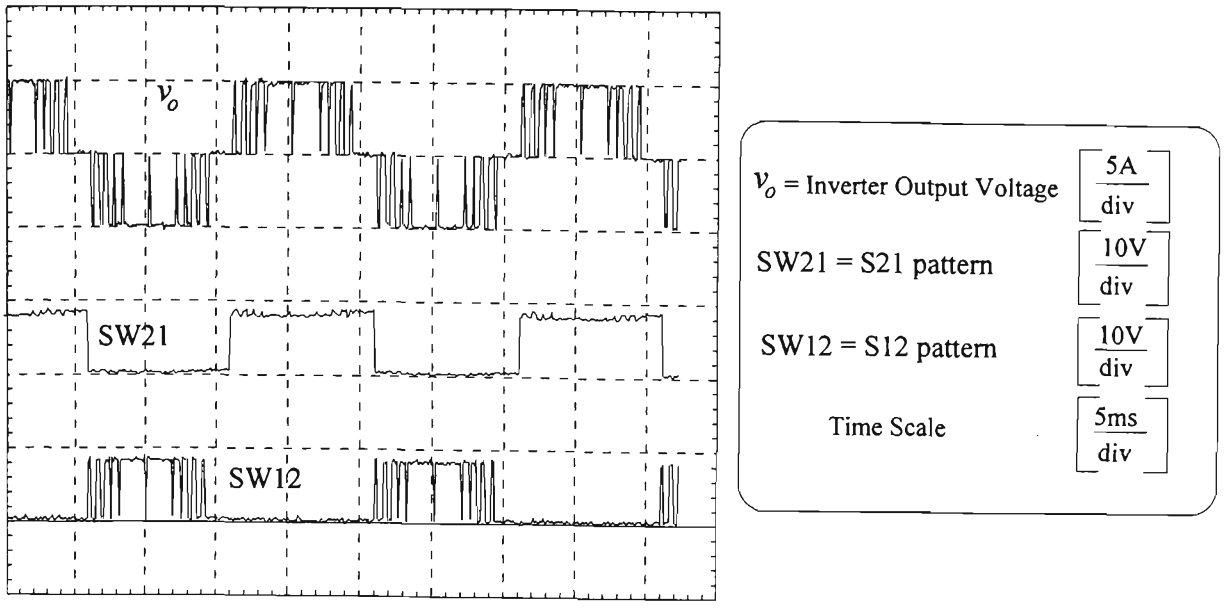
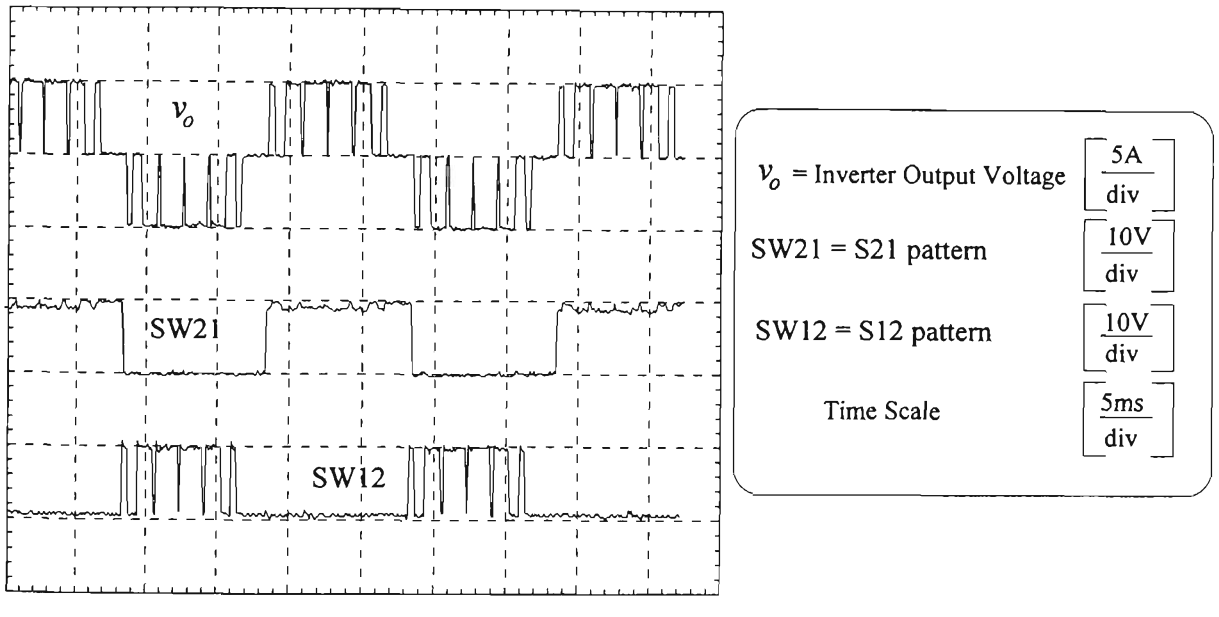


Figure 5.2: The inverter voltage and current: (a) p=20, (b) p=12.

Figure 5.3 illustrates the output PWM pattern and the proposed hybrid switching sequence, discussed in Section 2.5. As shown in this figure, the switches, SW_{21} and SW_{22}, are switched at the fundamental frequency, f_o and the switches, SW_{11} and SW_{12}, are switched at the switching frequency, pf_o.



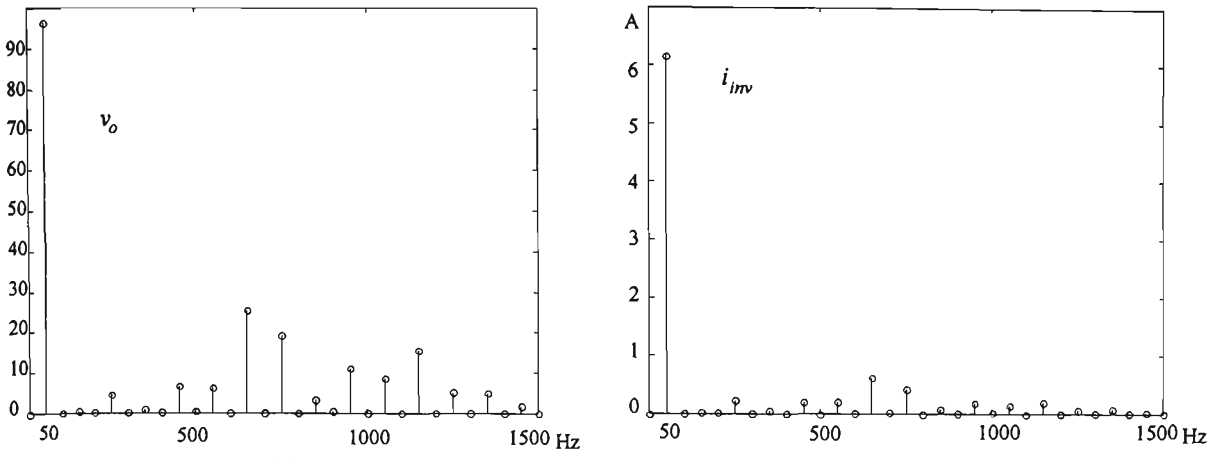
(a)



(b)

Figure 5.3: The inverter voltage and switching patterns for SW_{21} and SW_{12}: (a) p=20, (b) p=12.

Figure 5.4 shows the frequency spectrum of the inverter output voltage and inverter output current for a frequency ratio of *12*. The frequency spectrum of the output voltage shows the low order harmonics 5^{th}, 7^{th}, 9^{th} and 11^{th}. As a result of the switching frequency ratio of 12, the 13^{th} harmonic (650 Hz) is the highest harmonic component in the frequency spectrum. As shown in Figure 5.4-b, the harmonic distortion of the inverter output current is reduced significantly by the presence of the R-L load.



(a) (b)

Figure 5.4: Frequency spectrum of : (a) the inverter output voltage, (b) load current (p=12, M=1.0).

5.2.2 Harmonic Distortion

The experimental results for the harmonic evaluation of the proposed PWM technique are presented in this Section. The harmonic distortion factor, defined by Equation (2.22) is used to evaluate the harmonic distortion in the inverter output voltage waveform.

The variation of harmonic distortion factor (HDF) versus the modulation index are shown in Figures 5.5-a and 5.5-b for two selected frequency ratios. The modulation depth is varied in the range 0.1 to 1.1. The HDF is seen to decrease as the modulation index is increased. On the average HDF shown by Figure 5.5-b stay below the value of HDF shown in Figure 5.5-a. The values of HDF over most of the modulation depths closely agree with the simulation results given Figures 2.21 and 2.22 in Chapter 2.

Figure 5.6 shows the variation of fundamental voltage over a range of the modulation depths, from 0.1 to 1.1. It can be noticed that a near linear relationship exists between the modulation depth and the fundamental voltage.

The variation of HDF with the fundamental voltage for experimental and simulation results are shown in Figure 5.7. For p=8 and 12 the experimental results are in close agreement with the simulation results considering the accuracy involved with the experimental measurements. For higher frequency ratios the number of pulses increases and their pulsewidths narrow down. This results in an error in measuring the exact position of the pulses accurately from the test circuit which is evident from Figure 5.7 (b).

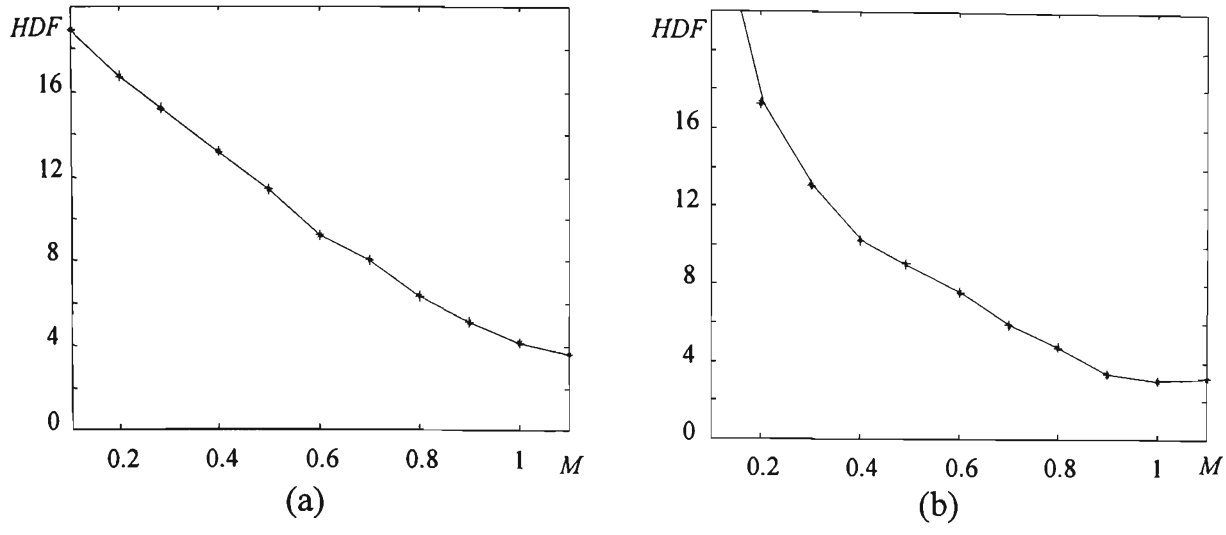


Figure 5.5: HDF versus modulation depth for frequency ratios: (a) p=8,(b) p= 12.

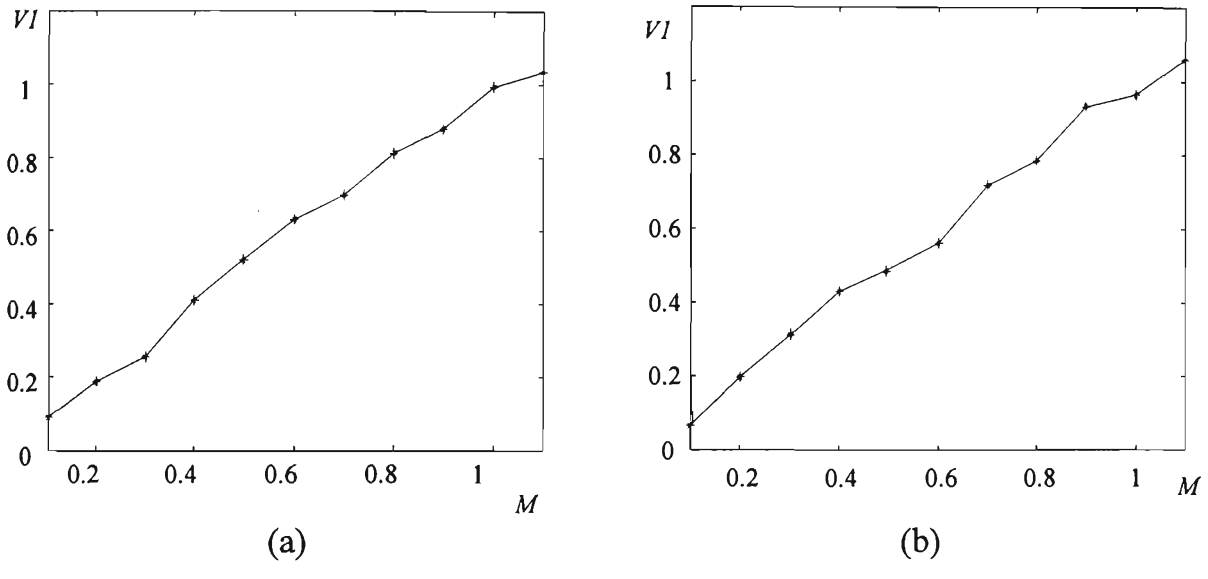


Figure 5.6: Per Unit fundamental voltage (V_1) versus modulation depth (M) for: (a) p=8, (b) p=12.

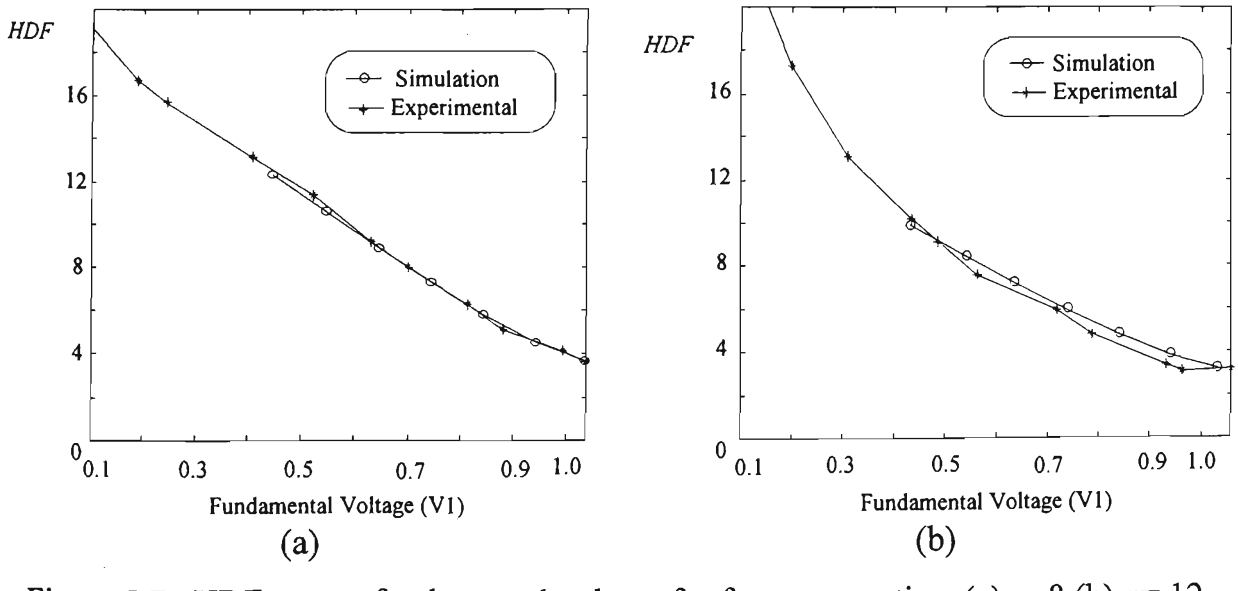


Figure 5.7: HDF versus fundamental voltage for frequency ratios: (a) p=8,(b) p= 12.

5.3 HARMONIC AND FREQUENCY ESTIMATION

The proposed techniques for frequency tracking, harmonic estimation and selective harmonic compensation are evaluated by considering the experimental results presented in this Section.

5.3.1 Frequency Estimation

In order to evaluate the performance of the FM demodulation (FDM) based frequency estimation technique a waveform from an external signal generator is used. The aim is to examine the performance of the frequency estimator which is used for filter bank parameterisation. The FM demodulation technique has been tested for the slow varying and the transient frequency tracking.

Figure 5.8 shows the performance of the FM demodulation module in tracking the signal frequency for a step change from 50 Hz to 51.66 Hz. Although step changes in the fundamental frequency is not common in power system operation, this example shows the effectiveness of this system in frequency tracking. When the noise level and harmonic distortion in the input signal are low, the order of the FIR filter employed in this technique can be reduced which further improves the performance of the frequency tracking in terms of accuracy and tracking delay (Section 3.4.2.1 of Chapter 3).

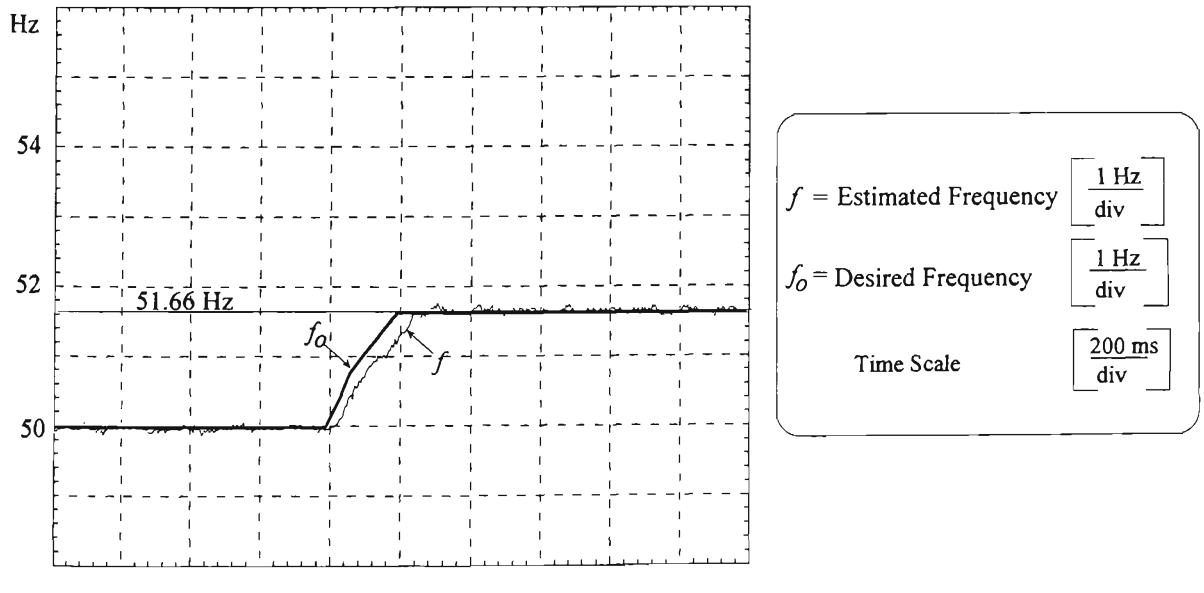


Figure 5.8: The estimated frequency and the voltage waveform.

5.3.2 Harmonic Estimation with Filter Bank

The experimental results in relation to the performance evaluation of the proposed technique are presented in this Section. A non-sinusoidal load current waveform has been decomposed into the fundamental and harmonic components using the filter bank module. The estimated waveforms at the output of the filter bank can be used to calculate the phase and magnitude of each harmonic if required. However, this is not necessary as the reconstruction of the reference waveform requires only the instantaneous magnitude of the harmonic components. The phase of the supply voltage and the fundamental load current waveforms have been determined using the phase and frequency tracking module.

The initial bandpass frequencies of the filter bank are set to the integer multiples of the fundamental frequency. The load current and supply voltage are sampled at a frequency of 3200 Hz. The load current is decomposed into fundamental and harmonic waveforms. Using the estimated harmonic component waveforms, the reference waveform can be reconstructed by instantaneous addition of the estimated components. Figures 5.9-5.11 show the digital snapshots of the estimated harmonic waveforms of a non-linear load in steady state.

Figure 5.9 shows the fundamental and 3^{rd} harmonic load current waveforms. It shows the phase delay, ϕ, of the fundamental current waveform with respect to the supply voltage. The estimated waveforms are used to reconstruct the reference waveform for harmonic reduction which includes the harmonic waveforms and the reactive component of the fundamental. The phase of the fundamental current is estimated by the phase and frequency tracking module. Figures 5.10-5.11 shows the estimated significant harmonic current waveforms for the case illustrated in Figure 5.9.

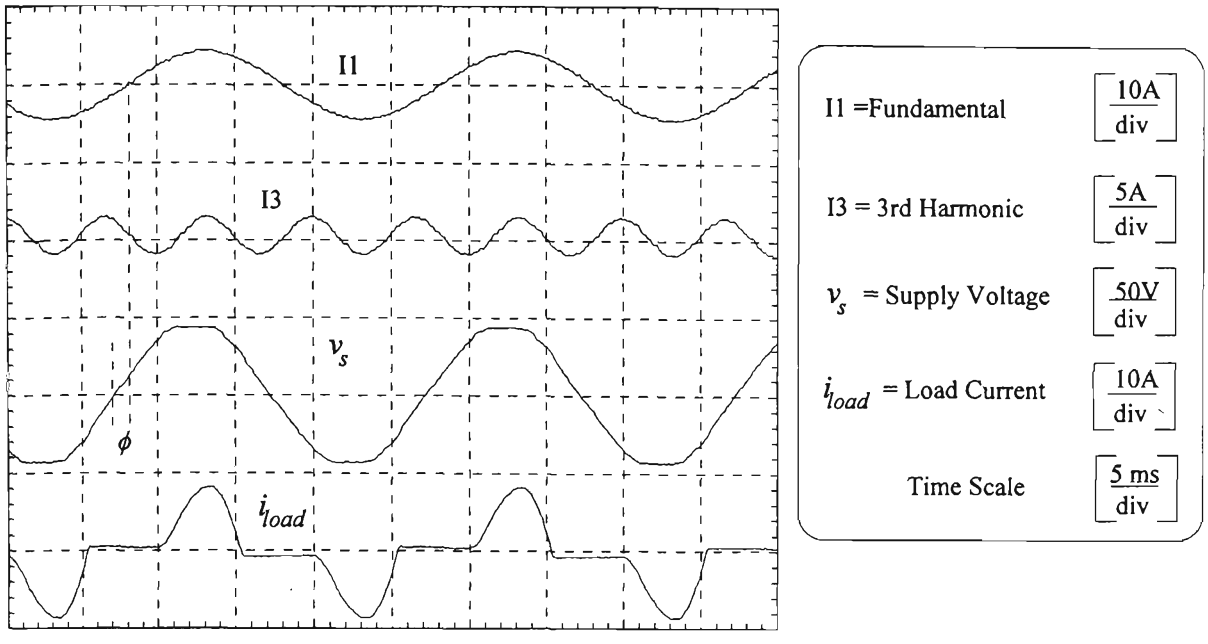


Figure 5.9: The estimated fundamental current (I_1), 3[rd] harmonic (I_3), in relation to supply voltage (V_s) and load current (I_{load}).

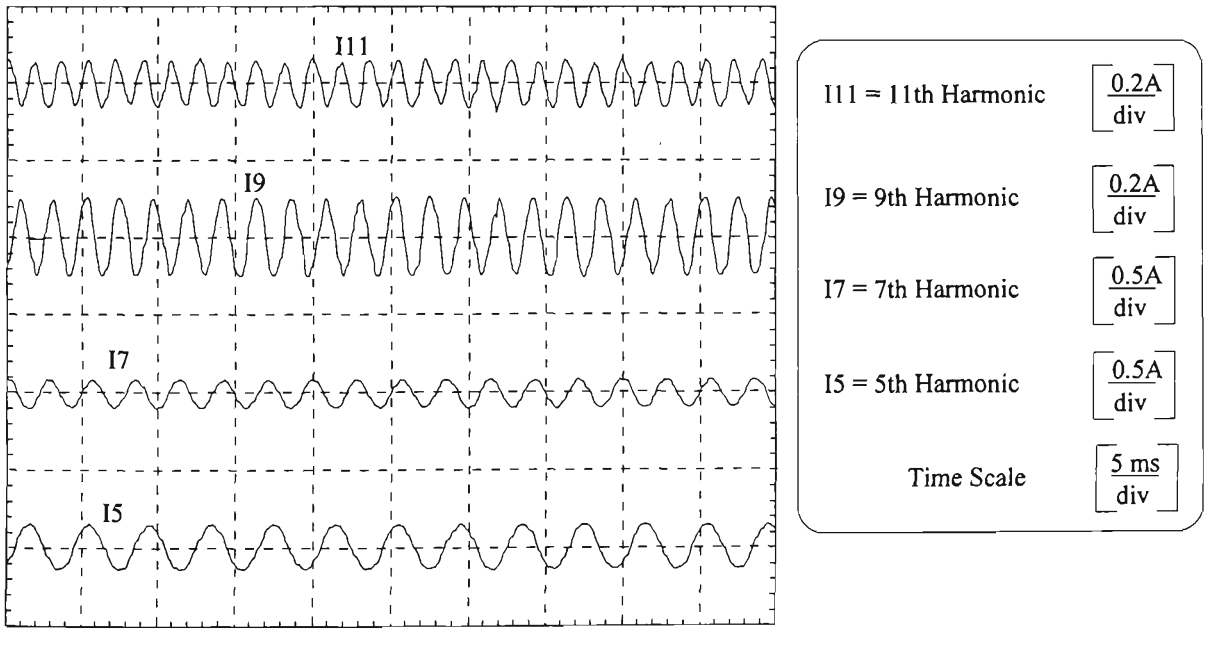


Figure 5.10: The estimated current harmonic waveforms: 11[th], 9[th], 7[th] and 5[th].

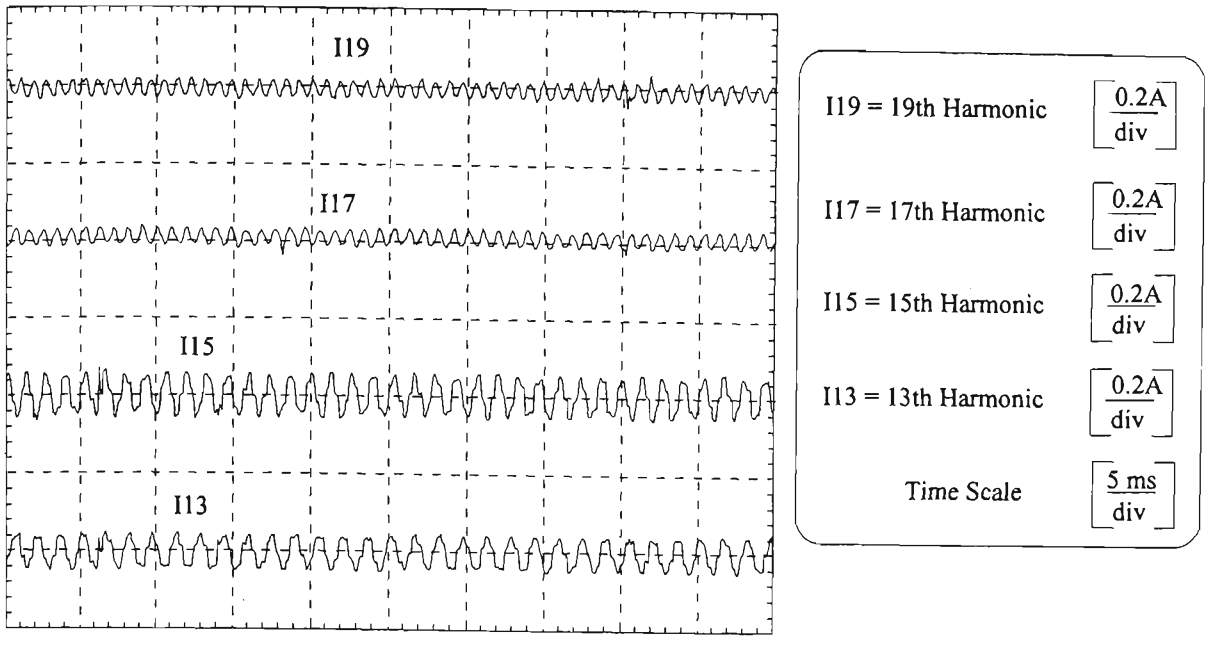


Figure 5.11: The estimated current harmonic waveforms: 19^{th}, 17^{th}, 15^{th} and 13^{th}.

The band-pass frequency of each filter in the filter bank can be placed on any frequency ranging form 0 Hz to half the sampling frequency (Nyquist limitation). For harmonic estimation, the band-pass frequency of each filter should be placed on integer-multiple frequencies of the fundamental. Therefore, the number of filters in filter bank will be limited by computational capability of the processor. In these experiments, 32 filters in the filter bank have been used.

The computational burden of the control strategy for harmonic estimation and reduction determines the maximum sampling frequency. A sampling frequency of 3200 Hz chosen in these experiments is normally high enough to retrieve significant harmonic components of the non-sinusoidal load current. During each sampling period, ie 312 μs, the DSP (TMS320C32-60 MHz) implements the harmonic estimation module, frequency tracking and reference waveform generation. The time slices of each process are given in Table 5.2.

Table 5.2: Computational burden of proposed control strategy.

Data acquisition	Phase & frequency tracking	Harmonic estimation & measurement	Reference waveform & PWM generation	Total
20 μs	130 μs	100 μs	40 μs	290 μs

5.4 HARMONIC COMPENSATION

In this Section the experimental results for harmonic compensation are presented. Three harmonic compensation schemes have been employed in this project. These are full, selective and harmonic standard based compensation schemes.

5.4.1 Full Harmonic Compensation

In this experiment, no harmonic limits are applied in relation to harmonic compensation. The experimental results for full compensation are presented in Figure 5.12. It shows the load current and source current waveforms after the compensation. The active power filter current, i_{apf}, includes all harmonic components of the load current. Injecting the active filter current into the point of common coupling (PCC) using the PWM switching strategy introduces some high frequency components which can be easily removed by an extra high pass-filter.

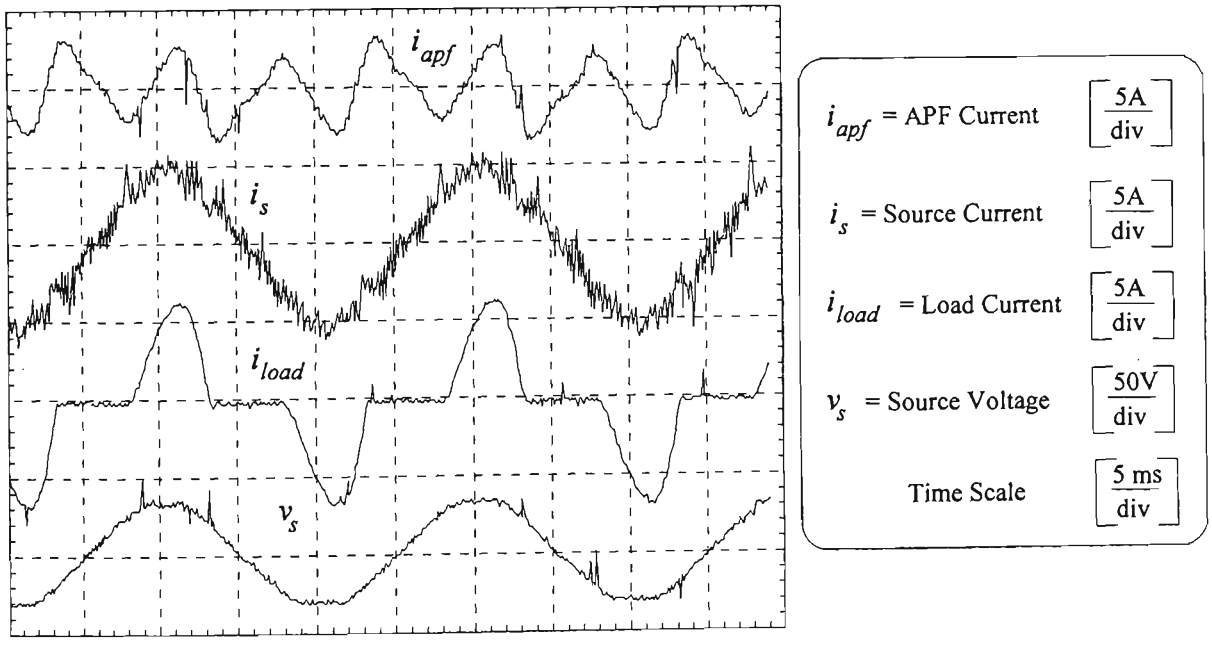


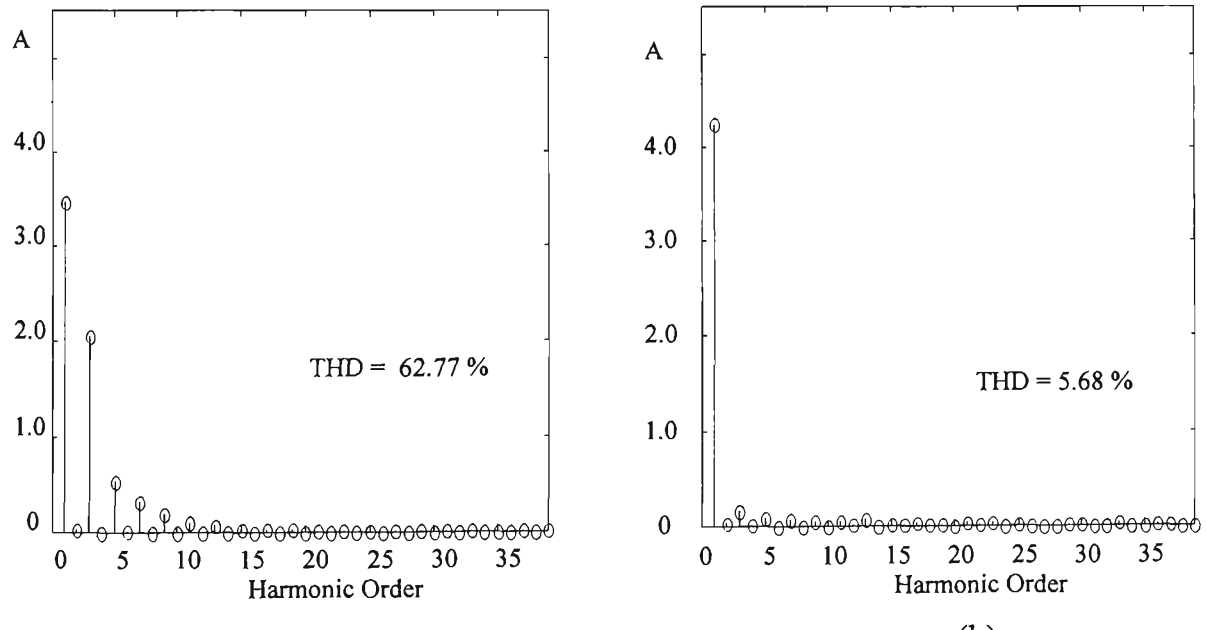
Figure 5.12: Full harmonic compensation scheme.

Figure 5.13 (a) shows the frequency spectrum of the source current waveform before compensation. As shown in Figure 5.13 (a), the odd harmonics are the dominant harmonic components. Figure 5.13 (b) shows the frequency spectrum of the source current after harmonic compensation. As seen in this figure the low order harmonics have been effectively reduced. The fundamental current after compensation is slightly

higher than the fundamental before harmonic compensation. This is due to the fundamental current taken by the inverter to compensate for the switching losses.

The compensation process includes all retrieved harmonics from the harmonic estimation modules. The source current waveform shows some high frequency distortion due primarily to the PWM switching. This high frequency distortion in the output is a function of the switching frequency of the PWM strategy employed. To have an exact replica of the reference waveform in the output of the active filter inverter, a smaller value of isolation inductance, L_{apf}, should be used. On the other hand, a smaller isolation inductance increases the switching frequency in the Hysteresis PWM technique employed in these experiments. In the case of low isolation inductance, a high pass filter in the output of the inverter suppresses the high frequency components.

The total harmonic distortion (THD) of the source current in this experiment is calculated to be 62.8% before compensation and 5.6% after compensation which is satisfactory for an average switching frequency of 4 kHz of the inverter.



(a) (b)

Figure 5.13: The frequency spectrum of source current;
(a) before and (b) after compensation.

5.4.2 Selective Compensation

In this Section the experimental results for selective harmonic compensation are presented. In this selective harmonic compensation one or a set of harmonic components

can be compensated. Figures 5.14-5.22 show the experimental results for the three selective compensation schemes. In these schemes 3rd, 5th, 7th harmonic components are compensated separately or in a combined fashion.

5.4.2.1 3rd harmonic cancellation

Figure 5.14 shows the experimental results for 3rd harmonic cancellation. The magnitude of the 3rd harmonic current component is about half of the fundamental one. The APF reference current waveform only includes the 3rd harmonic and a small fundamental current to compensate for the switching losses. As the 3rd harmonic is the largest harmonic component of the load current, the source current after compensation is close in its shape to a sinusoidal. The APF reference waveform only includes a low frequency component of the 3rd harmonic and a small fundamental component which is drawn by the voltage stabiliser to compensate the switching losses of the inverter. This low frequency components of the reference waveform further reduces the switching frequency of the Hysteresis PWM.

Figure 5.15 shows the harmonic spectrum of the source current before and after compensation. As the 3rd harmonic is the main and largest component of the load current a significant drop in total harmonic distortion (THD) occurs after compensation (from nearly 62% to 15%).

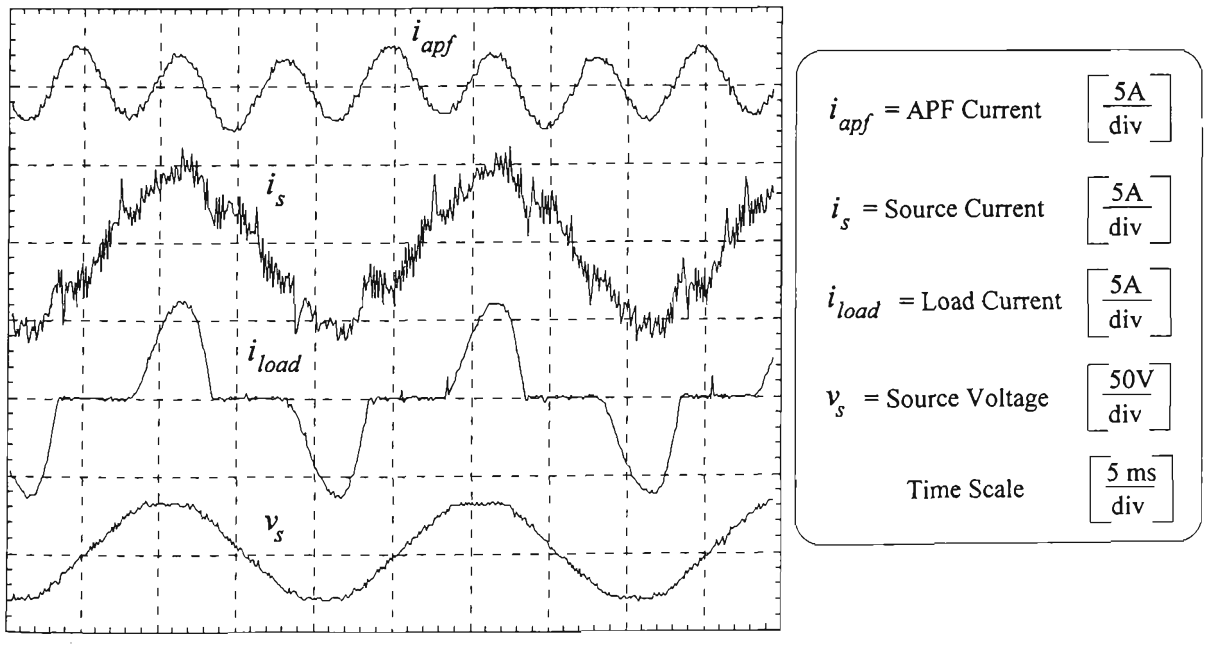


Figure 5.14: Selective harmonic compensation; 3rd harmonic.

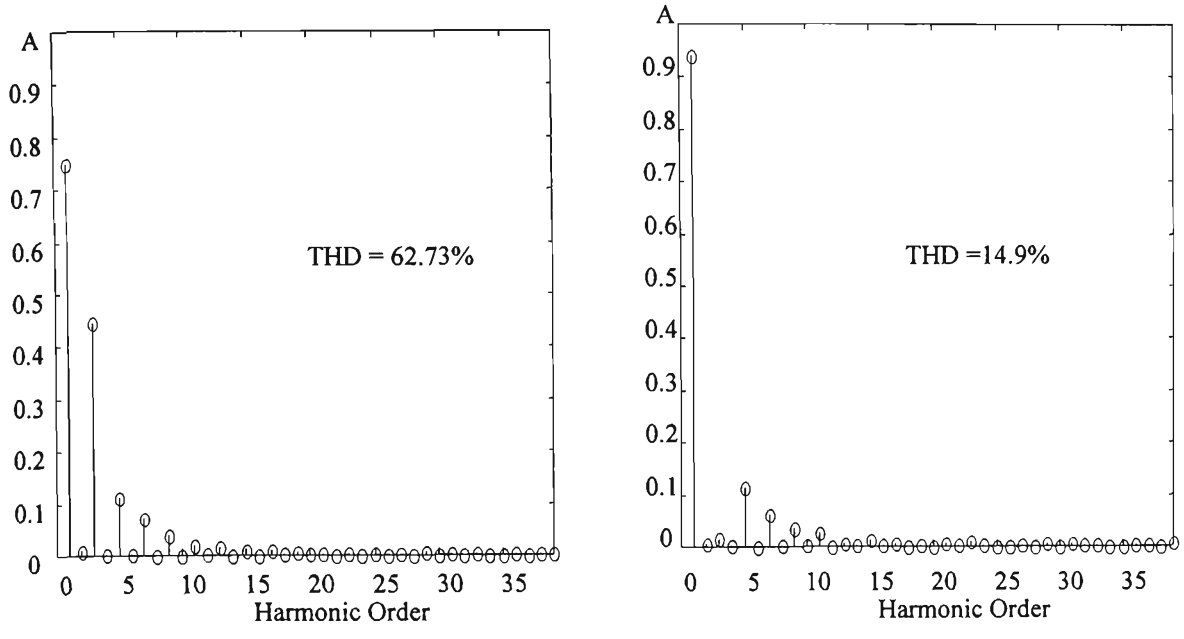


Figure 5.15: The frequency spectrum of source current for 3rd harmonic reduction (a) before and (b) after compensation.

5.4.2.2 5th harmonic cancellation

Figure 5.16 shows the experimental results for 5th harmonic cancellation. The magnitude of the 5th harmonic current component is not significant compared to the 3rd harmonic. Therefore, no significant harmonic reduction can be seen on the source current waveform.

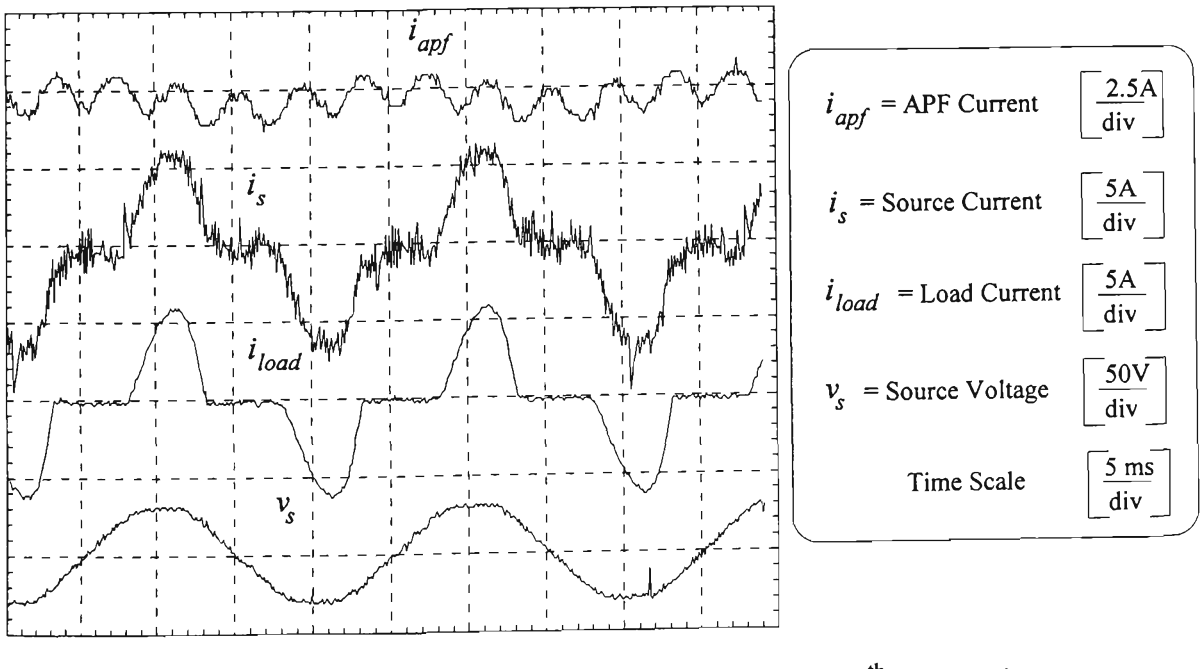
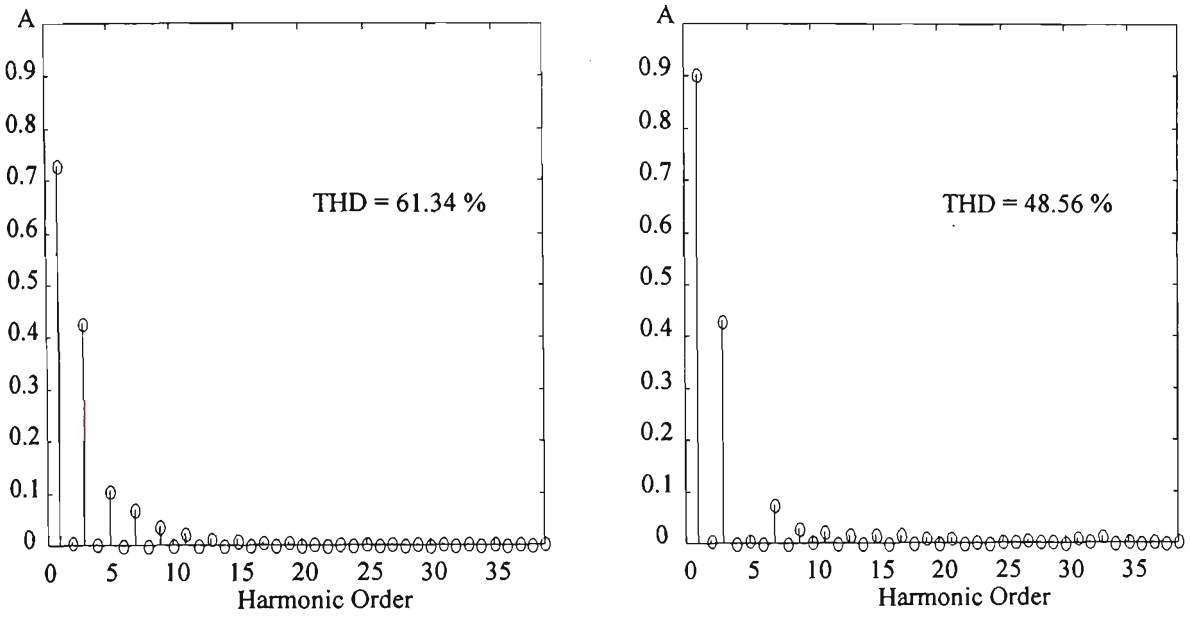


Figure 5.16: Selective harmonic compensation; 5th harmonic.

Figure 5.17 shows the harmonic spectrum of the source current before and after compensation. The 5th harmonic in the load current has decreased from 15% to about 1.3% and the THD reduced from 61% to 49% which seems unsatisfactory.



(a) (b)

Figure 5.17: The frequency spectrum of source current for 5th harmonic reduction (a) before and (b) after compensation.

5.4.2.3 3rd and 5th harmonic cancellation

Figure 5.18 shows the experimental results for combined 3rd and 5th harmonic reduction. The corresponding spectrum is given in Figure 5.19 which shows that THD has been reduced form 63% to 9%. As seen in Figures 5.18 and 5.19 except for the high frequency components due to switching, the fundamental is seen to be the significant component in the source current waveform.

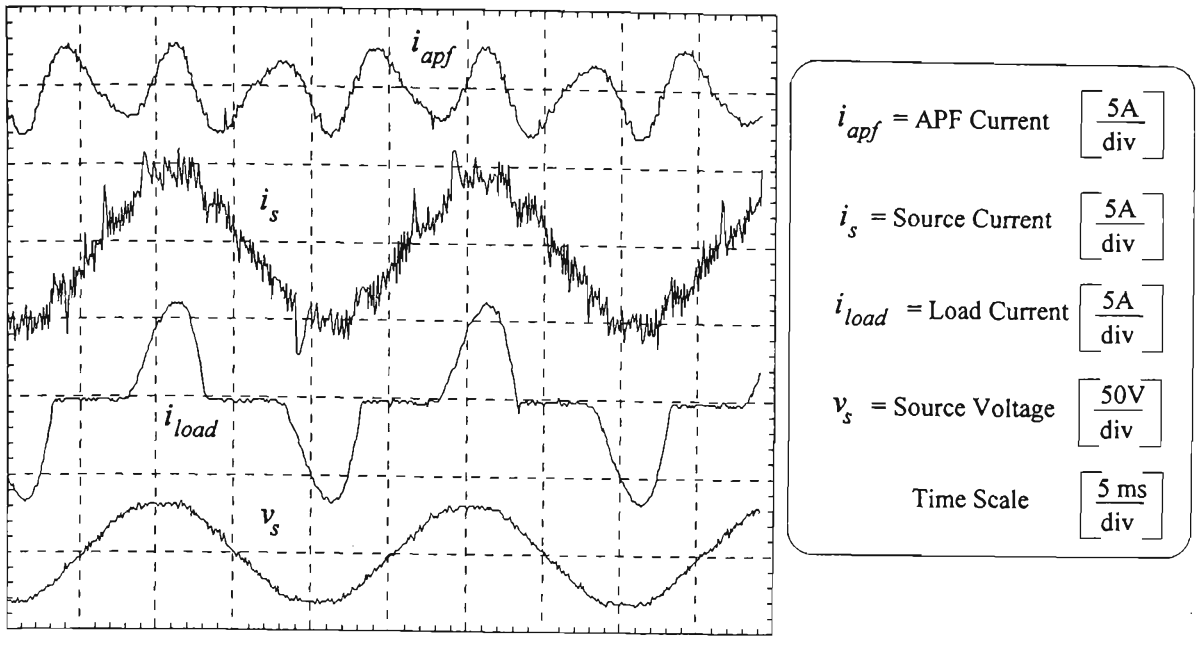
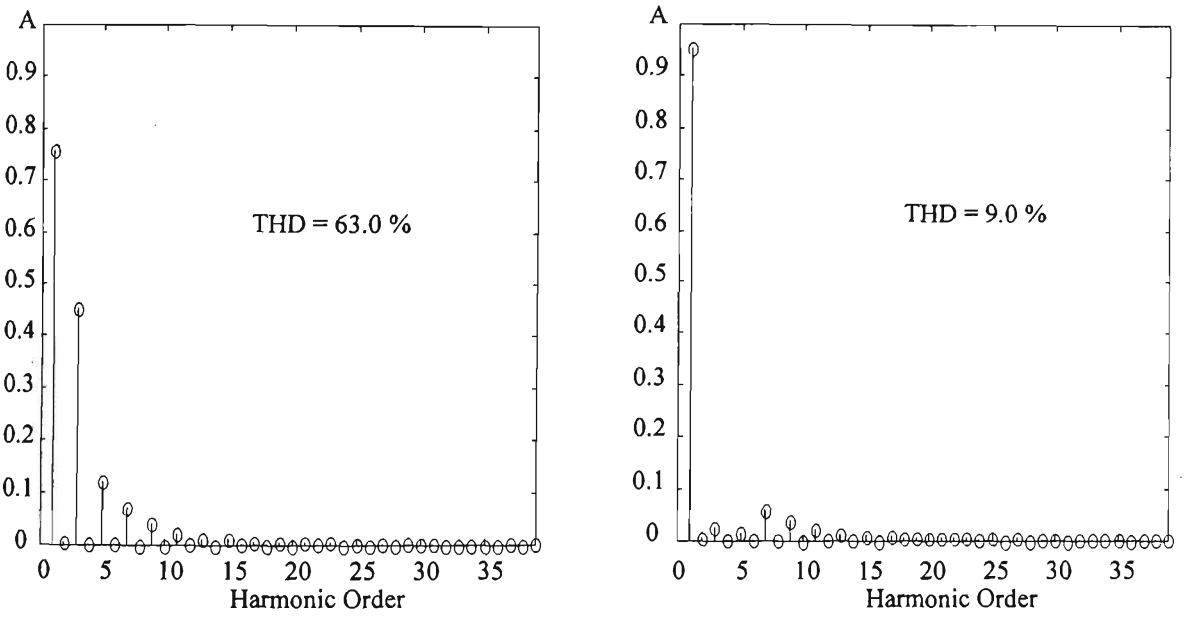


Figure 5.18: Selective harmonic compensation; 3rd + 5th harmonics.



(a) (b)

Figure 5.19: The frequency spectrum of source current for 3rd +5th harmonic reduction (a) before and (b) after compensation.

5.4.2.4 3rd + 5th +7th harmonic cancellation

The experimental results for combined compensation of 3rd, 5th and 7th harmonic components are presented in Figures 5.20 and 5.22 without and with reactive compensations respectively. The corresponding frequency spectra of the source and load current waveforms are shown in Figures 5.21 and 5.23.

Figure 5.20 shows the harmonic reduction without any power factor correction. The source current still shows the phase delay with respect to the supply voltage. Figure 5.21 shows the frequency spectrum of the source current before and after compensation. The THD level has been reduced from 62.7% to 8.0% which is very close the full-compensation scheme (Figure 5.13).

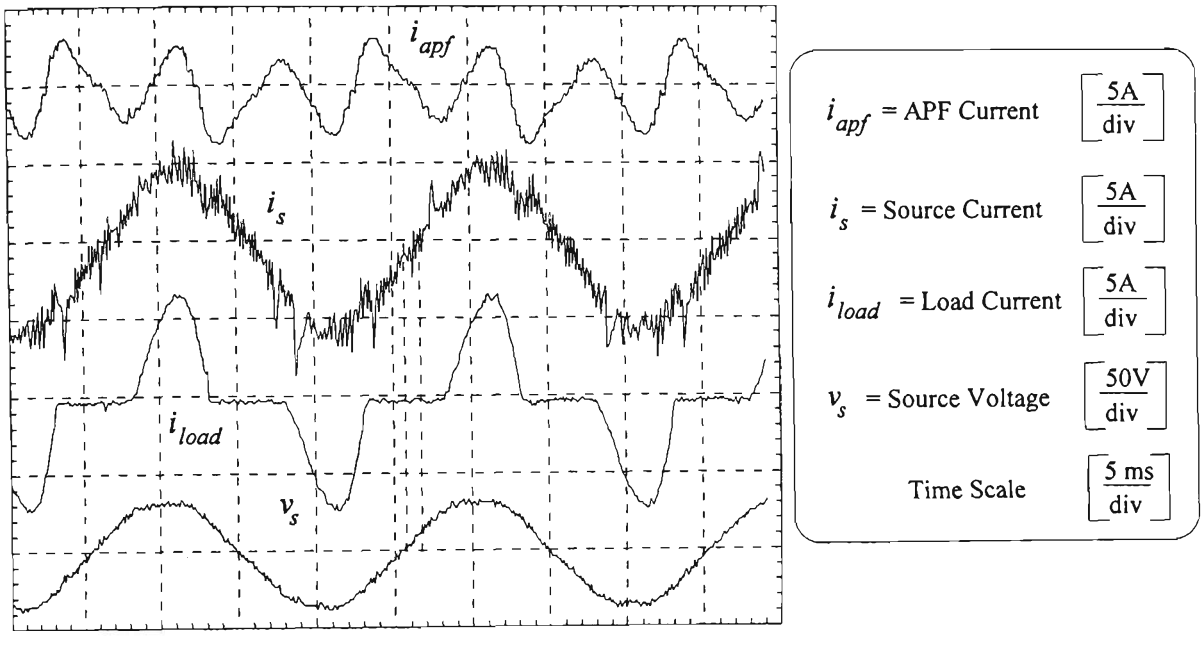


Figure 5.20: Selective harmonic compensation; 3rd +5th +7th harmonics.

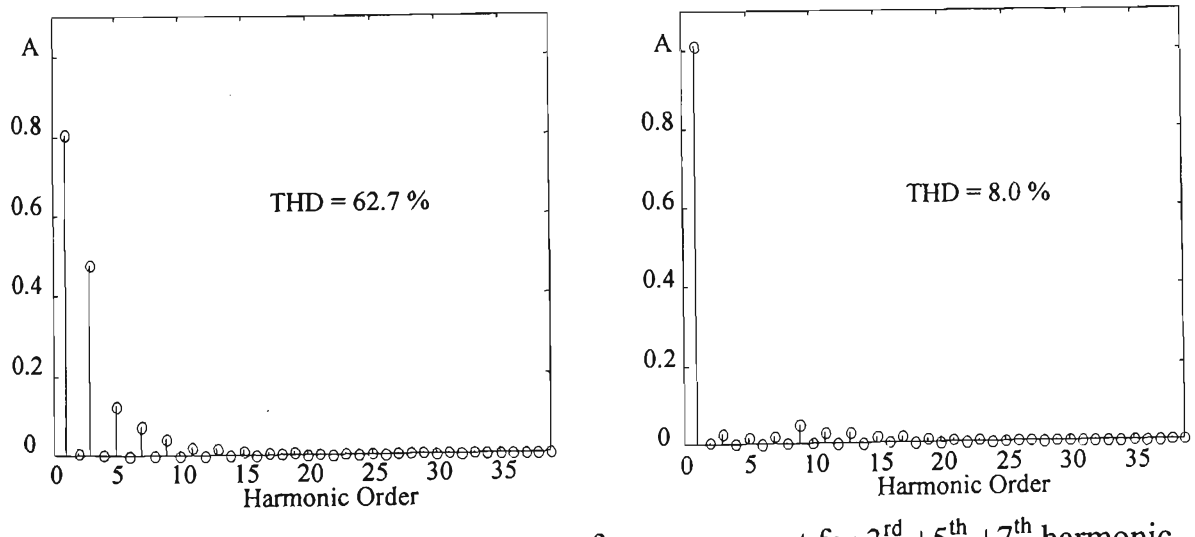


Figure 5.21: The frequency spectrum of source current for 3rd +5th +7th harmonic reduction (a) before and (b) after compensation.

Figure 5.22 shows the experimental results for the same scheme but with fundamental reactive power compensation. The phase difference of the source current waveform with respect to the supply voltage has been reduced from 27° in Figure 5.20 to 9° in Figure 5.22 (ie. $cos(\phi)$ from 89% to 98%). The THD of the source current is decreased from 62% to 10% as shown in Figure 5.23. The reason for an increase in THD in the second case (harmonic reduction and reactive power compensation) is the reduction of the source fundamental current obtained by power factor correction (Note: $THD \propto 1/I_1$).

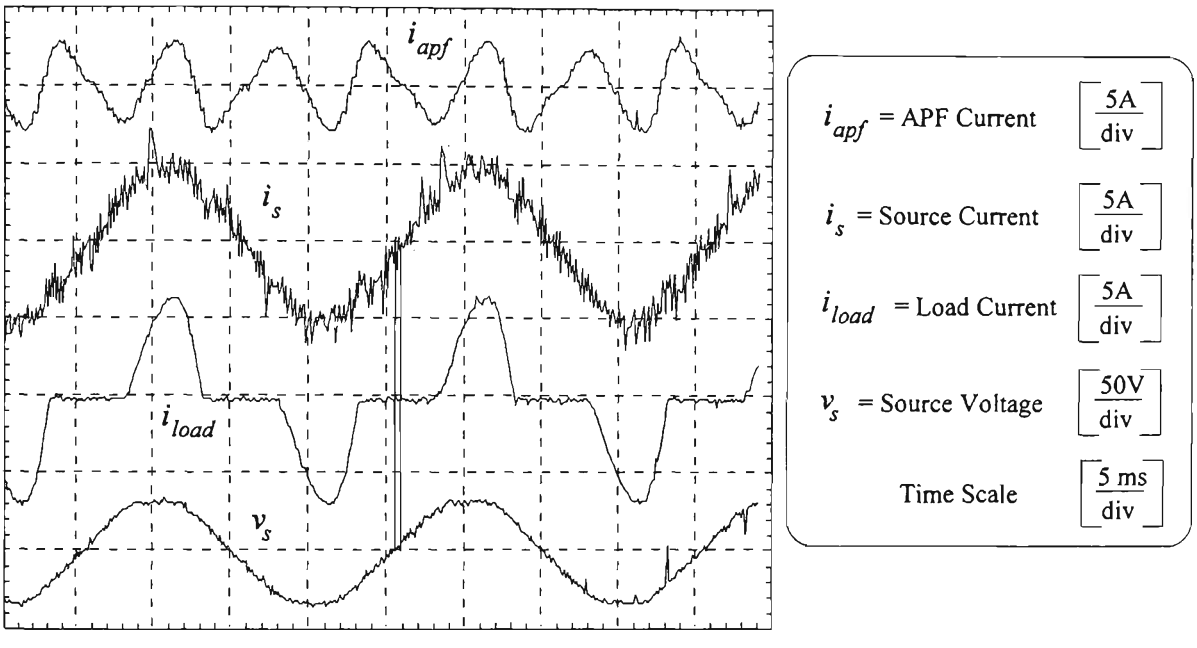


Figure 5.22: Selective harmonic compensation; 3rd +5th +7th harmonics and reactive power compensation.

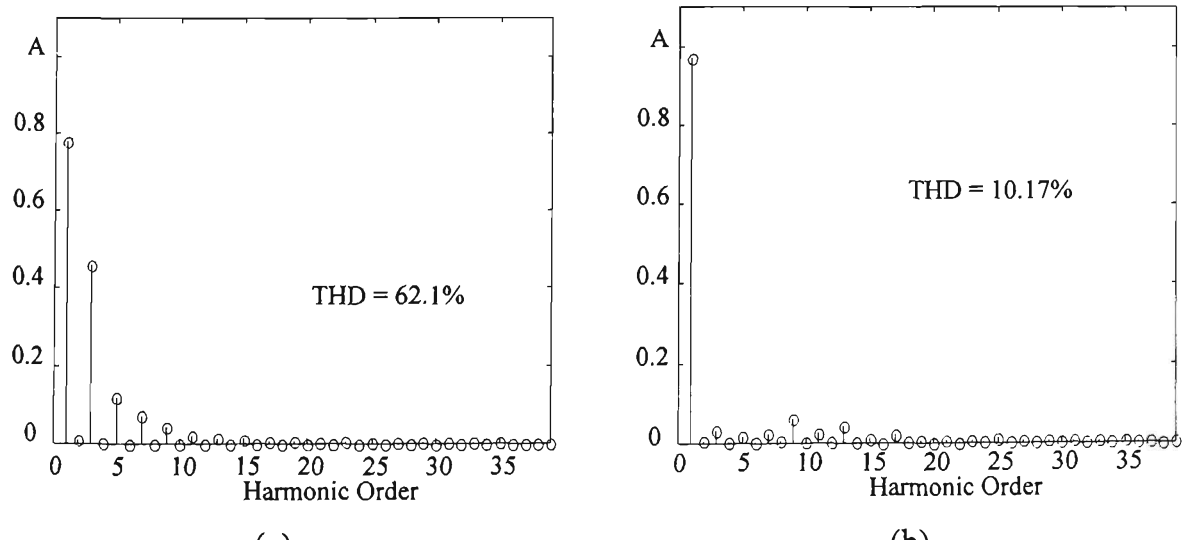


Figure 5.23: The frequency spectrum of source current for 3rd +5th +7th harmonic reduction (a) before and (b) after compensation with reactive power.

5.4.3 Compensation Based Harmonic Standards

In the proposed harmonic compensation schemes based on harmonic standards, the individual harmonic voltage ratio, K_h^{std}, and the total harmonic distortion of voltage (THDV) due to non-linear load current at the point of common coupling (PCC) should be kept below the levels recommended by harmonic standards. These harmonic voltage limits can be converted to harmonic current distortion limits that are more appropriate for the application of the proposed schemes. In Chapter 4 the guidelines for calculation of K_h^{std} and conversion of the recommended harmonic voltage limits to the harmonic current limits were given [4].

The value for K_h^{std} is determined based on several parameters including the load power, supply system impedances and short circuit current at PCC. In order to verify the proposed concept for partial harmonic standard based compensation K_h^{std} has been chosen to be a constant for all harmonic orders. Three values of K_h^{std}=5%, 10% and 15% are chosen which are equal and less than the typical values given in Table 4.1 [4]. The experimental results for these schemes are presented in Figures 5.24-5.30. The harmonic magnitudes are reduced in these schemes up to the K_h^{std} % of the fundamental load current.

5.4.3.1 $K_h^{std} = 5\%$

Figures 5.24 and 5.25 show the experimental results for APF, load and source current waveforms and frequency spectrums respectively. In this scheme all source current harmonic magnitudes should be kept below 5% of the fundamental current. As shown in Figure 5.25-d, the 3rd, 5th and 7th harmonic components exceed 5% of the fundamental. Therefore, the APF current contains the 3rd, 5th and 7th harmonics. The total harmonic distortion in the source current is reduced from nearly 51% to 12%. The performance of the APF in this scheme is similar to the selective 3rd harmonic reduction scheme.

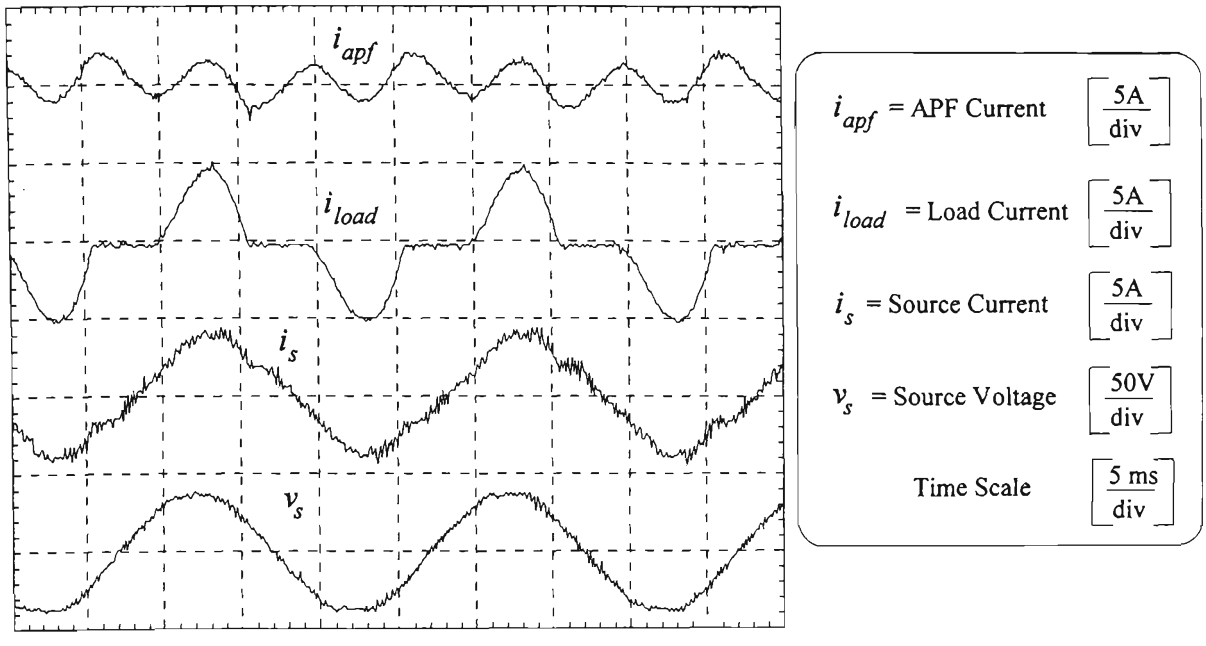
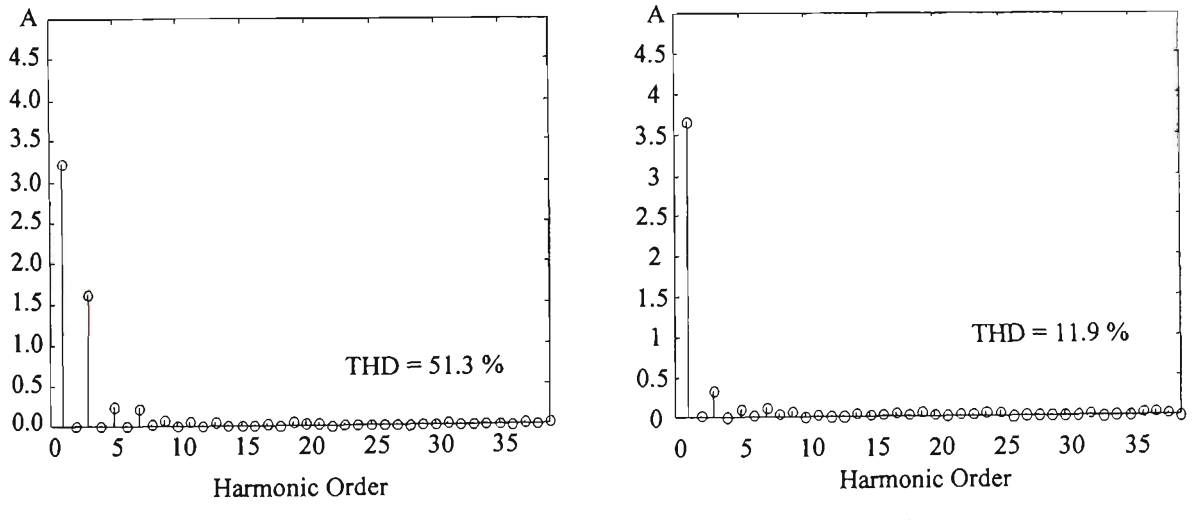


Figure 5.24: The 5% harmonic compensation scheme.



(a) (b)

Figure 5.25: The frequency spectrum of source current for 5% compensation scheme: (a) before and (b) after compensation.

5.4.3.2 $K_h^{std} = 10\%$

The experimental results for APF, load and source current waveforms and frequency spectrums respectively are shown in Figures 5.26 and 5.27. The source harmonic current magnitudes are reduced to 10% of the fundamental load current. As shown in Figure 5.27-d the third harmonic is nearly 50% of the fundamental and the other harmonic components are below the 10% threshold. The APF should reduce the 3rd

harmonic component to a level below 10% of the fundamental. Therefore the APF reference waveform consists of the third harmonic (80% of 3rd) and a small fraction of the fundamental to compensate the switching losses.

The total harmonic distortion in source current is reduced from nearly 51% to 15% which is mostly due to 3rd harmonic reduction. The performance of APF in this scheme is similar to the selective 3rd harmonic compensation scheme.

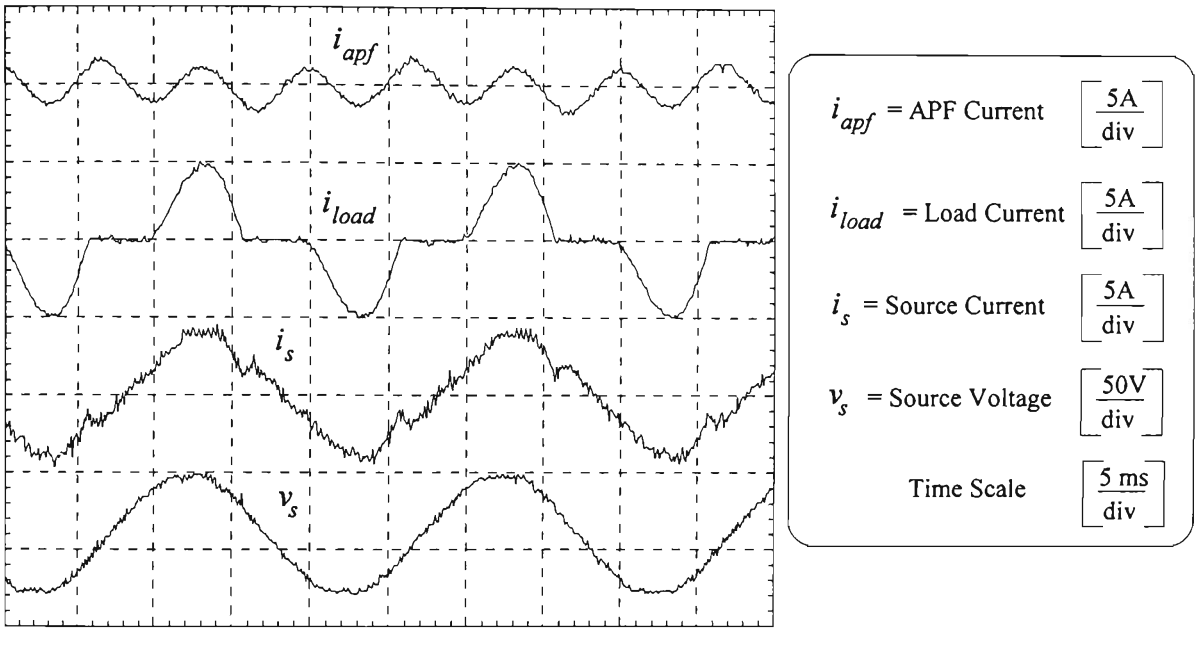
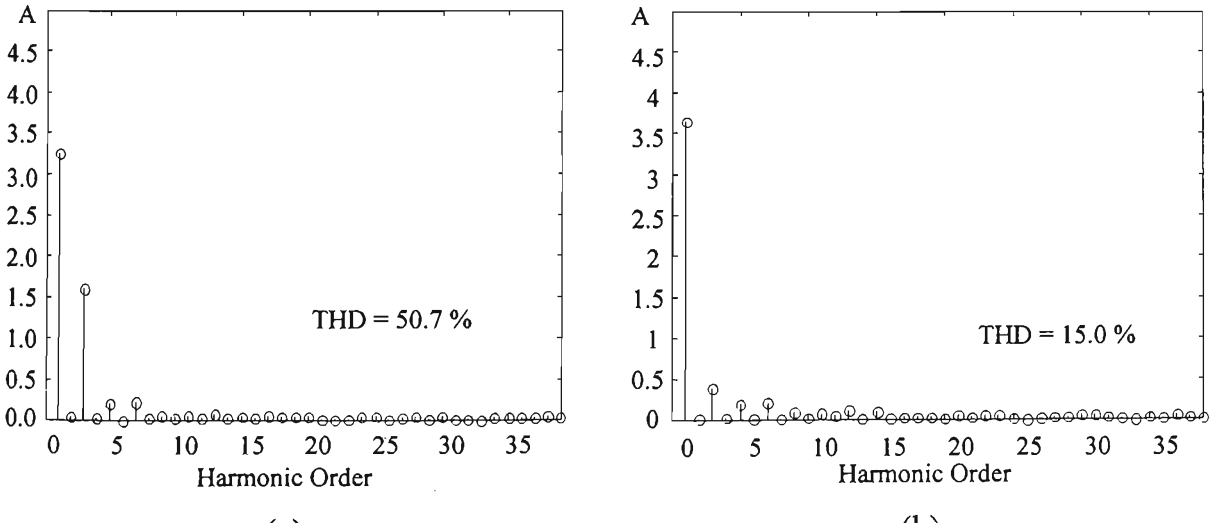


Figure 5.26: The 10% harmonic compensation scheme.



(a) (b)

Figure 5.27: The frequency spectrum of source current for 10% compensation scheme: (a) before and (b) after compensation.

5.4.3.3 $K_h^{std} = 15\%$

Figures 5.28 and 5.29 show the experimental results for APF, load and source current waveforms and frequency spectrums. In this experiment all load current harmonic magnitudes are reduced to 15% of the fundamental load current. Similar to 10% compensation scheme, only the third harmonic component does not exceed the 15% threshold. As shown in Figure 5.29-b, the level of compensation (3rd harmonic) is much lower than in the previous experiment. The source current THD is reduced from nearly 50% to 22%.

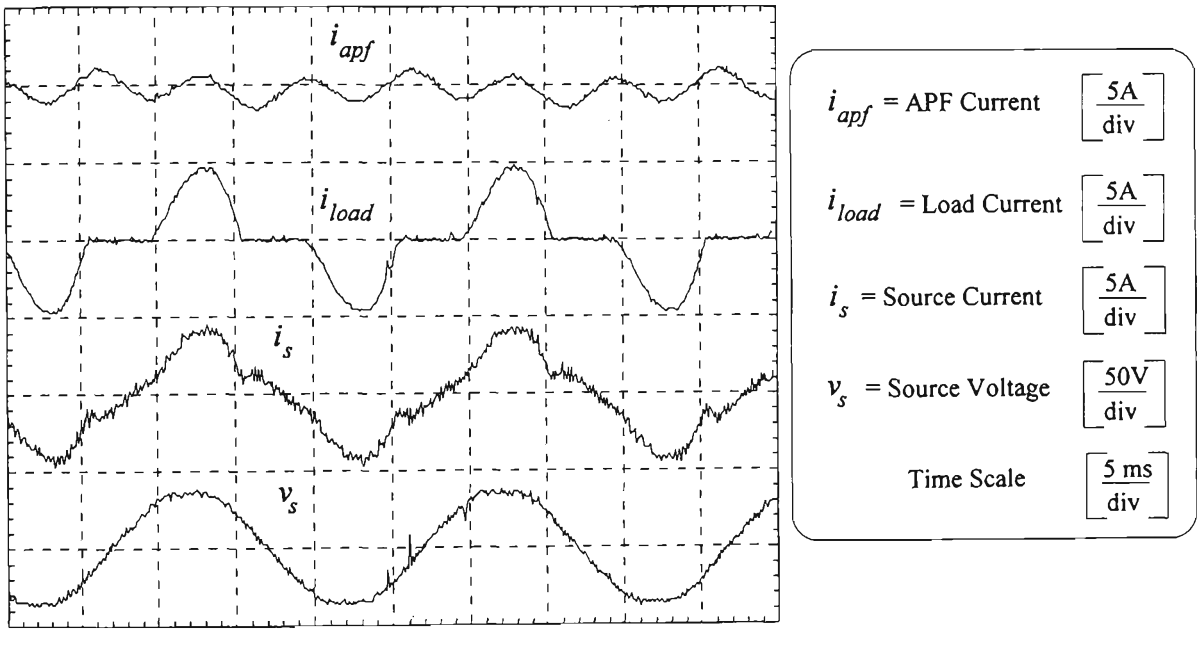


Figure 5.28: The 15% harmonic compensation scheme.

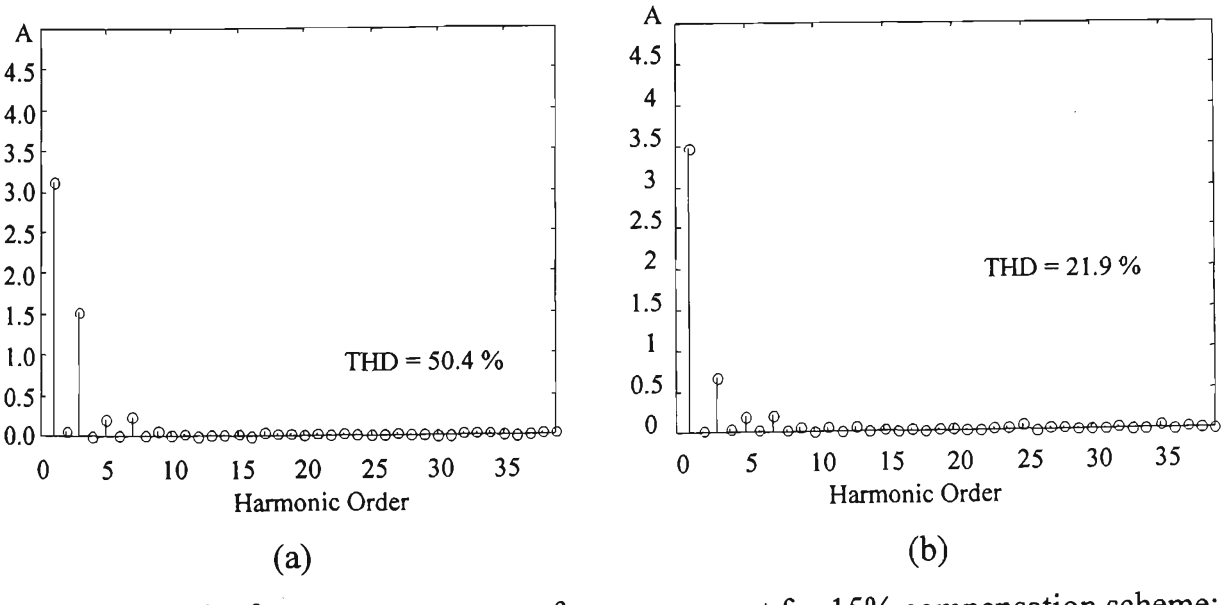


Figure 5.29: The frequency spectrum of source current for 15% compensation scheme: (a) before and (b) after compensation.

5.4.3.4 $K_h^{std} = 20\%$

The experimental results for APF, load and source current waveforms and frequency spectrums are shown in Figures 5.30 and 5.31. The load harmonic current magnitudes are reduced to 20% of the fundamental load current. The magnitude of the third harmonic in this experiment is more than 50% of the fundamental. Other harmonic components are below 20% threshold. The source current THD is reduced from 51% to 26%. The reduction in APF current reduces the switching losses therefore the magnitude of the fundamental current in APF is also reduced.

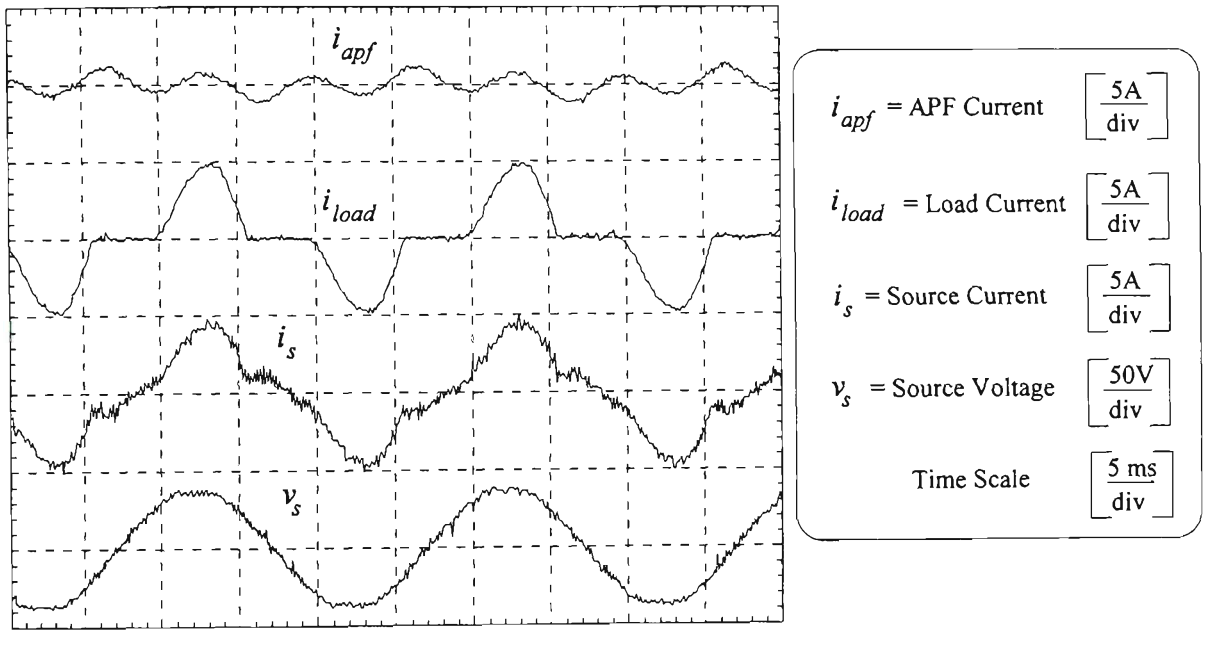


Figure 5.30: The 20% harmonic compensation scheme.

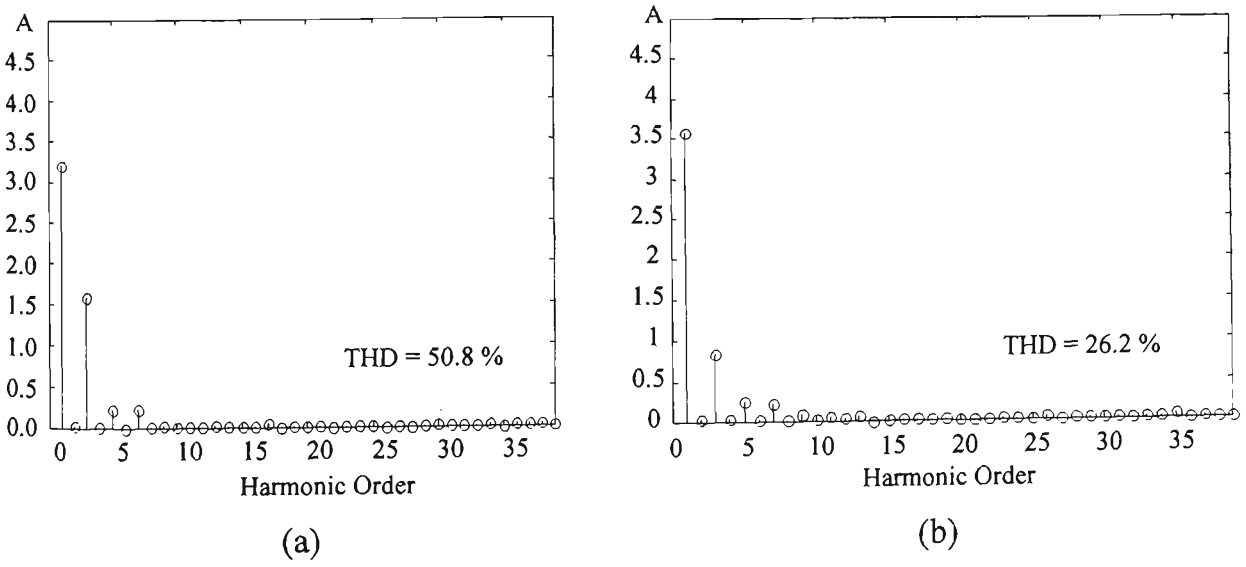


Figure 5.31: The frequency spectrum of source current for 20% compensation scheme: (a) before and (b) after compensation.

Table 5.3 shows the magnitude of the fundamental source current, i_{s1}, the maximum APF current, i_{apf}, the real power of the APF, p_{apf}, and the maximum apparent power of the APF, $p_{apf(max)}$, for the implemented schemes. As seen from Table 5.3, reduction of the level of harmonic compensation (increasing K_h^{std}) reduces the power of the active power filter. For example, the maximum apparent power of the APF is reduced from 113 VA in full compensation to 103 VA when the $K_h^{std} = 5\%$ scheme is applied; a reduction of almost 9% in the active power filter rating.

Table 5.3: The comparison of the selected schemes for harmonic reduction.

Standard levels K_h^{std}	i_{s1} **(A)**	$i_{apf(max)}$ **(A)**	p_{apf} **(W)**	$p_{apf(max)}$ **(VA)**	**THD** *before compensation*	**THD** *after compensation*
Full (0%)	2.6	2.6	3.8	113	51 %	4 %
5%	2.6	1.8	2.7	103	51 %	12 %
10%	2.6	1.6	1.9	105	51 %	15 %
15%	2.6	1.3	1.6	98	50 %	22 %
20%	2.5	1.2	1.1	72	51 %	26 %

5.4.4 Transient Performance

The transient performance of the active power filter subject to a step change in load current magnitude was tested. This transient operation is obtained by generating a step change in the load current magnitude up to twice the steady state load current. The case of this sudden change from full load to half load working conditions and vice versa are illustrated in Figures 5.32 and 5.33. As shown in Figures 5.32 and 5.33, line current reaches the steady state in almost three cycles after the step change had occurred. The delay associated with the time response of the system is due to the filter settling time in the harmonic estimation module. If we consider the trajectory for , V_{dc}, it is evident that

under transient conditions APF current increases to supply the increased load current demand by taking the energy instantaneously from the DC bus capacitor. The DC bus capacitor voltage is seen to recover within about three cycles from the effect of step change in the load current.

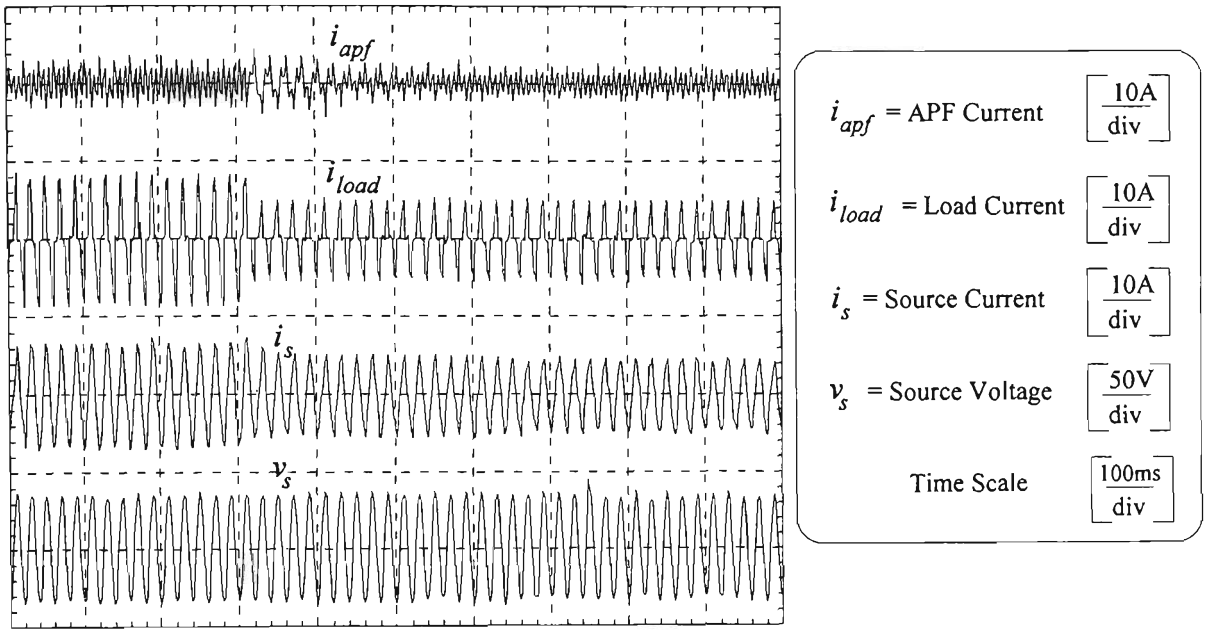


Figure 5.32: Transient Performance of APF with harmonic standard (5%).

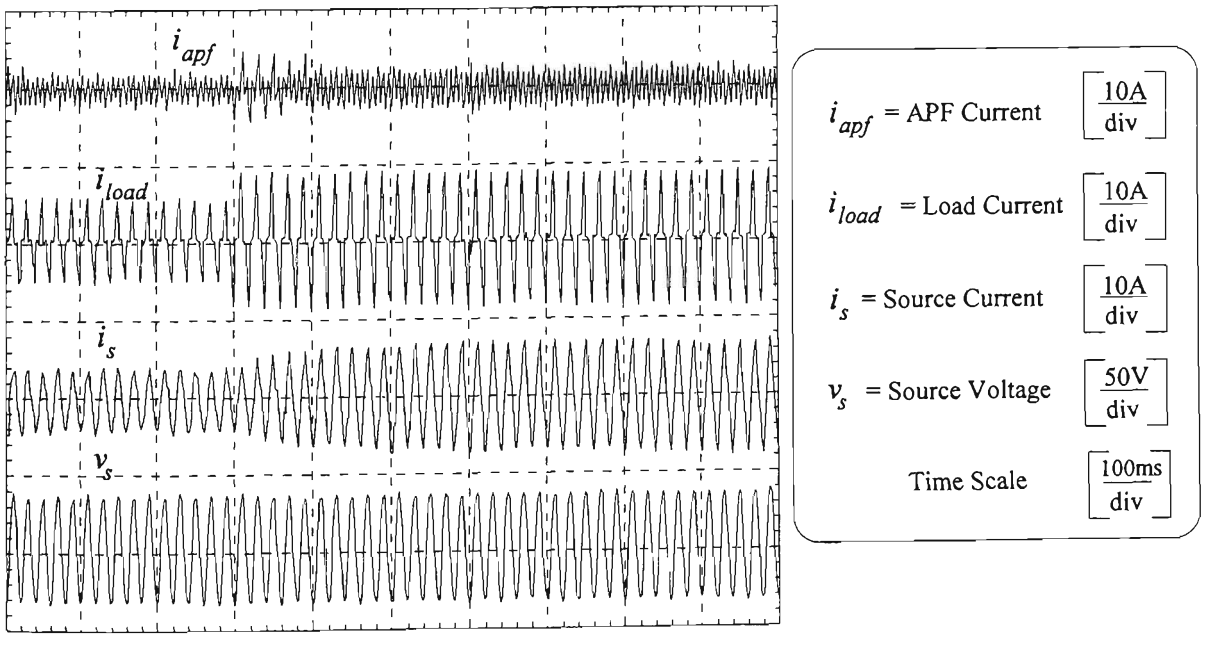


Figure 5.33: Transient Performance of APF with harmonic standard (5%).

5.5 CONCLUSION

In this Chapter the capabilities of the proposed DSP based control strategy for active power filtering have been demonstrated. The proposed control strategy for active power filtering was verified through measurements on a laboratory prototype active power filter. Furthermore, the experimental results for the proposed equal area based PWM (EAPWM) switching strategy were also presented.

The proposed EAPWM switching strategy was implemented on an inverter circuit of the prototype circuit. The experimental results validated the performance of EAPWM for the inverter based applications, in terms of reduced harmonic distortion factor (HDF) and increased fundamental voltage. The experimental results confirmed the validity of simulation results presented in Chapter 2.

The experimental results in relation to the performance evaluation of the FM demodulation based frequency tracking technique was illustrated. The time-varying frequency of the input signal was identified for slow varying and transient conditions. The estimated fundamental frequency was used to adjust the parameters of the filter bank.

The ability of the filter bank based harmonic estimator was demonstrated in harmonic retrieval for non-sinusoidal load current waveform. The capabilities of the proposed harmonic estimation and measurement techniques were employed for selective and partial harmonic reduction in active power filtering. The experimental results were presented for selective harmonic compensation schemes including the cancellation of the 3^{rd}, 5^{th}, 7^{th} and their combinations with and without reactive power compensation.

The recommendations of harmonic standards were incorporated for partial harmonic compensation. The proposed standard based schemes for harmonic reduction were implemented. These schemes include the partial reduction of source current harmonic components up to K_h^{std}=5%, 10% 15% and 20% of the fundamental current. The experimental results showed the effectiveness of the proposed control strategy in reducing the power rating of the APF while fulfilling the harmonic standard requirements.

CHAPTER 6.

CONCLUSION

The issue of power quality in general, and harmonic distortion in particular is an important issue for utilities and customers and leads most utilities to find economical solutions. It is now an obligation upon utilities and consumers to resolve the issues of the excessive harmonic distortion within a mutually acceptable framework or in accordance with existing harmonic standards [13, 16]. In this regard, this thesis dealt with the problem of harmonic reduction in power systems and inverter based PWM applications.

In recent years there has been considerable interest in the use of active power filters (APF) for reducing harmonic currents in power systems [21-24]. Active power filters inject equal-but-opposite distortion directly at the point of common coupling thereby cancelling the original distortion of the load current.

The control strategies used for active power filters can be either time or frequency domain based techniques [18, 19, 31]. In time domain approaches, the instantaneous error due to the deviation of the voltage or current from its reference waveform is used to control the PWM voltage or current source inverters for injection of equal-but-opposite distortion at the PCC. Frequency domain approaches such as fast Fourier transform (FFT) have only been considered for predetermined and selective compensation due to the high computational burden and the associated delays. The main

disadvantage of this method is its high computational requirements especially when it comes to online operation and non-integer components such as interharmonics.

Predetermined harmonic cancellation is another approach in the frequency domain category. This approach is similar to tuned passive filters in that a set of harmonics can be selected for compensation [18, 22]. The reference waveform is synthesised from the estimated harmonic components using a PWM switching strategy. It is possible to reduce a specific harmonic to a desired level of compensation while reducing the power rating of the active power filter. This approach has been used in inverter based applications such as adjustable speed drives to reduce the level of harmonics in the inverter output current [40, 41].

In this thesis a new control strategy for active power filtering was proposed. The proposed control strategy is a time-domain approach. On the other hand, it gives all the best features from the frequency domain approaches such as partial harmonic cancellation. Furthermore, a new PWM switching strategy for full-bridge inverter based applications has been proposed. The new switching strategy gives better performance in terms of minimum harmonic distortion and higher fundamental voltage when compared to conventional techniques [43].

6.1 EQUAL AREA BASED PWM TECHNIQUE (EAPWM)

The equal area based PWM technique (EAPWM) is essentially a non-uniform sampling technique with the centre of the PWM pulses aligned with the centre of integration of the corresponding areas of the reference waveform.

A performance evaluation of the EAPWM along with three conventional open-loop PWM switching strategies was presented. These three conventional PWM switching strategies are natural sampling, regular sampling and equal sampling techniques. The same conditions were used for all three techniques in order to perform a comparison.

The natural and regular sampling techniques were computationally least expensive out of the selected techniques when compared with the equal sampling technique. It was shown that EAPWM yields a significant improvement in terms of minimal harmonic distortion factor (HDF) while producing a higher fundamental voltage magnitude than the conventional techniques [42, 43]. The EAPWM switching strategy has considerable

practical use for variable-speed AC motor drive applications where harmonics in the output of the inverter pose serious problems to the drive performance.

6.2 HARMONIC REDUCTION

Harmonic compensation is a cost-sensitive issue for customers when the utilities start to enforce harmonic standards. Consequently, cost is still seen to be an obstacle for the wide spread deployment of active power filtering (APF). A reduction in active power filter ratings is desirable while satisfying the minimum requirements set in the harmonic standards. This can be achieved by reducing only those harmonics that exceed the acceptable levels recommended by the harmonic standards. This concept could be implemented by producing an on-line estimation of the load current harmonic components. Therefore, an adaptive filtering algorithm for active power filters was proposed in Chapter 3. The proposed algorithm estimates the phase and frequency of the fundamental and the harmonic components of the load current in both steady state and transient conditions.

6.2.1 Infinite Impulse Response (IIR) Filter Bank

In the proposed harmonic estimation technique a resonator based filter bank is used. The parallel structure of this filter enables the desired harmonic components to be retrieved using IIR resonator filters. The centre frequency of each IIR filter in the filter bank is aligned to the frequency of the load current harmonic or interharmonic components.

6.2.2 Frequency Tracking

To estimate the harmonic components of the load current waveform an accurate estimation of the fundamental frequency is required. Two methods were evaluated; namely adaptive IIR filtering and FM demodulation (FMD) techniques.

Adaptive IIR filter employs an IIR filter whose bandpass frequency is adaptively varied such that the mean square of the error signal at that frequency is minimised. The frequency of the input signal can be easily estimated from the filter parameter. Among the various adaptive algorithms which have been proposed for IIR filters, the gradient based algorithm was used in this project which is simple to implement due to its low complexity [72].

In contrast to the adaptive IIR filter where there is no priori knowledge on the frequency of the signal, in the frequency demodulation technique (FMD) the boundaries of the frequency of the signal are known. Using this information, the instantaneous phase and frequency of the power system fundamental voltage can be determined. It was shown through the simulation results that the FM demodulation gives improved performance in terms of the accuracy and the delay of tracking when compared to the adaptive IIR filtering technique.

6.2.3 Harmonic Estimation

When the frequency of the power system voltage waveform is identified it can be used for filter bank parameterisation. The bandwidth of the bandpass filters in filter bank is controlled by the feedback gain parameter. It was shown that the phase and gain of each bandpass filter at its centre frequency are exactly zero and unity, respectively.

Simulation results showed that the proposed structure provides accurate estimation of harmonic components of the load current. Once initialised, the proposed structure can provide on-line estimation of the fundamental and harmonic components. The simulation results for the estimation of the load current harmonic components up to the largest harmonic order were presented and compared with short-term Fourier transform simulation results. The results show that the proposed technique is capable of estimating the signal in a time-varying situation.

6.2.4 Harmonic Magnitude Calculation

Once the harmonic components of the load current waveform are retrieved, the magnitude and phase of each component can be calculated using a sliding algorithm. Simulation results for the magnitude calculation of the harmonic components of a non-sinusoidal load current were presented. The harmonic magnitudes were estimated accurately when the transient in the output of the filters had elapsed. The delay in the response of the technique in the transient situation was found to be a function of the IIR filter time response.

A harmonic phase error correction due to the delay in the data acquisition and processing was introduced in Chapter 4. This was incorporated into the harmonic estimation module.

6.3 ACTIVE POWER FILTER

Using the ideas of the adaptive harmonic estimation technique proposed in Chapter 3, several harmonic reduction schemes for active power filter control strategies were discussed. These included full compensation, selective and harmonic standard based compensation schemes.

In Chapter 4 a detailed discussion on the implementation of the proposed control strategy for active power filtering using a digital signal processor (DSP) and an IGBT based inverter was presented. A working prototype of a shunt APF was designed and built around the TMS320C32 DSP and the IGBT inverter modules.

6.4 EXPERIMENTAL RESULTS

6.4.1 Equal Area Based PWM Technique (EAPWM)

In Chapter 5, the experimental results for the proposed EAPWM PWM technique and the control strategy for active power filtering were presented. The proposed EAPWM technique was implemented on the DSP and with some changes in the configuration of the active power filter circuit such as providing a dc supply for inverter, the circuit was used to verify the proposed method. The experimental results for two selected switching frequency ratios and a wide range of modulation indices were presented. In these experiments, the EAPWM method was used to synthesise a sinusoidal waveform with different frequency ratios and modulation indices. The experimental results validated the simulation results given in Chapter 2 and indicate that lower HDF is achieved by using EAPWM technique.

6.4.2 Frequency and Harmonic Estimation

The experimental results for FM demodulation based frequency tracking in both steady state and transient situations were presented. The estimated fundamental frequency was used to adapt the filter parameters in the filter bank. This technique further provides on-

line estimation of the phase of the fundamental current with respect to voltage for reactive power compensation purposes.

The experimental results for the retrieval of the significant harmonic waveforms were presented. The on-line calculation of load current harmonic magnitudes was implemented to determine the level of compensation in the proposed harmonic reduction schemes. The harmonic waveforms of interest were adjusted to a percentage of the fundamental magnitude which is set by harmonic standards. The modified waveforms were then added together to form the active power filter reference waveform.

A priori knowledge about the harmonic content of the load current waveforms can be used to reduce the number of filters in the filter bank structure which further reduces the computational burden.

6.4.3 Harmonic Reduction

The proposed harmonic reduction schemes for active power filtering, described in Chapter 4, were implemented and described in Chapter 5. These include selective and partial compensation schemes. The experimental results were presented for selective low order harmonic compensation including the cancellation of the 3^{rd}, 5^{th}, 7^{th} and their combinations with and without reactive power compensation. Four partial harmonic reduction schemes were implemented. The experimental results showed the effectiveness of the proposed control strategy in reducing the required power rating of the active power filter while fulfilling the particular requirements of a harmonic standard.

The proposed control strategy for harmonic compensation gives flexibility in terms of selective and partial harmonic and reactive power compensations. The performance of the proposed control strategy was presented through the experimental results. It has been shown that by employing partial harmonic reduction schemes the load harmonic current components can be reduced up to recommended values set by standards while a reduction in APF power rating can be achieved.

6.5 FUTURE RESEARCH ISSUES

Further research is required on both power electronic circuits and control strategies to improve the performance of the active power filters [25]. A continued effort in the field of power electronics and signal processing research will enable the power industry to have improved harmonic control of power systems in the future. The following are the issues that require further research:

1. In this project a single frequency estimator was used to track the fundamental frequency. It was assumed that all frequency components of the load current are integer multiples of frequency of the fundamental. However, in some applications the load current waveforms contain interharmonics and sub-harmonics. For example, in cyclo-convertors, the magnitude and the frequency of the interharmonic components are time-varying in nature. A frequency tracking technique for online tracking of the fundamental frequency and other frequency components of a non-linear loads such as cyclo-converters would be useful. In these cases fast and high resolution frequency estimation enables effective harmonic compensation.

2. Research on harmonic estimation has only considered the estimation of slow time-varying signals. Although the resulting estimation accuracy of these techniques was found to be adequate for most situations in power systems, it is expected that for some applications such as arc-furnaces and cyclo-convertors, where the magnitude and frequency of harmonics (and interharmonics) are changing very quickly, these methods may not provide an effective solution especially during the transient period.

3. The performance of the active power filter control strategy during transient periods should be further investigated. A technique for detecting and identifying transient situations can prevent any malfunctioning in the active power control strategy.

4. Stability of the proposed system in response to time-varying situations such as start and stop periods should be examined in detail. The initial conditions, time response, and convergence rate of the system should be studied.

5. A practical model of the power system should be considered in the analysis of the performance of the active power filters. This modelling enables the utilities and the customers to determine the harmonic voltage distortion at various buses due to the harmonic compensation using the proposed control strategies.

6. The digital simulations can be improved by taking into account the operation of the inverter and power system dynamic characteristics. Software packages such as Electro-Magnetic Transient Program (EMTP) can be used to this end. These packages allow the simulation of the power system and active power filters in transient and steady state conditions.

7. The online application of the proposed EAPWM switching strategy in active power filters may provide a reduction switching losses. The possibility of employing a parallel processor for EAPWM PWM signal generation can be investigated. This would provide extra processing capabilities for active power filter control system which allow the implementation of more advanced and complex algorithms.

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APPENDIX

A.

DSP PROGRAMS

A.1 ACTIVE POWER FILTER

A.1.1 Main Module

```
#include "stdio.h"
#include "periph.h"
#include "math.h"
#include "dsp.h"


/*   Defined Values */
#define INTERRUPT   2                          /* interrupt for adc 1 */
#define FIR_ORDER    75                        /* FIR Filter order */
#define FIR_BUF_SIZE FIR_ORDER + 1     /* ADC circular sample buffer size */
#define No_Harmonics      32     /* Cycle resolution or FFT resolution */

/* Prototypes       */

inline void hyst_pwm(void);       /* PWM generation module Natural Sampling */
void init_apf(void);              /* Initialise the whole variables */
void freq_est(void);              /* Frequency estimation module*/
void filt_bnk(void);              /* Filter bank filtering module */
void wave_ref(void);              /* Reference Waveform genration */


struct Resonator{
     double X;
     double W2;
     double WP;
     double A;
     double Y;
     double Yest;
     double Yold;
     double Std;                       /* Standard values*/
     double Gain;          /* Gain for Compensation (STD or partial)*/
     double Phase;         /* Phase Computation */
     double Mag;                       /* Magnitude of each Harmonics */
     double CCos;          /* Cos(2*Pi*50*m*dt) for Harm Estimation */
     double SSin;          /* Sin(2*Pi*50*m*dt) for Harm Estimation */
     double SinTable[64]; /* Sin Table for ache Harm and 64 Samples*/
     double CosTable[64]; /* Cos Table */
};
```

```
struct Resonator Harm[No_Harmonics];

double     PI = 3.14159265358979323846; /* PI number  */
double     c1,d1,C1,D1;                 /* Fourier values for Magnitude and
Phase */
double     Fundamental= 50;             /* Fundamental Frequency =50*/
double     Err=0, PErr, Ko = 0.00125;     /* IIR Erro Filter bank, Feedback
Gain*/
double     THD=0;          /* THD for Load Current   */

int        Sample11, Sample12;    /* Input from ADC1 Pin2 9,11*/
int        Sample21, Sample22;    /* Input from ADC2 Pins 5,7 */
int        Channel[8];                 /* ADC sample array */
floatLoadCurrent;                 /* Input Load Current pin 11 */
floatSupplyVoltage;       /* Input Supply Voltage pin 09 */
floatAPFCurrent;                  /* Inverter Current pin 07 */
floatCompensatedCurr;             /* Compensated Current */

double     Omega;        /* Frequency of carrier signal 2*PI*50/3200 */
double     OmegaTi;     /* Updated Frequency of carrier signal 2*PI*50/3200 */
int        N, NN=1;                    /* N: number of pulse per cycle  */
int        i=0,m=0,j=0;                      /* temporary variable */
int        time_0=0,time_e;             /* time before the main loop inside
loop*/

int        Sampling_Frequency;         /* Sampling Frequency */
float      Sampling_Period;            /* Sampling Period */
int        Loop_Period;                /* Loop Period in MicroSecond */

double     Yk_1R=0, Yk_1I=0,
double     Yk_2R=0, Yk_2I=0;     /* temp buffer for DF, Y_R and Y_I     */
double     DF, Phase,PHI=0;
double     Yk_C, Ireactive;            /* Frequency Deviation and Phase */
double     Phase_Offset;               /* Phase to Frequency in freq_est  */

double     STD_BASE=1;


int  cariertime=0,tic = 0;       /* sample pointer in time domain */
int  FIR_Pointer;                /* sample buffer tail,  head pointers */
int  LUT_Pointer=0;              /* Pointer to Sin or Cos  lookup Table */

double     dummy1,dummy2;        /* dummy variables */

float      FIR_Coeff[FIR_ORDER + 1];    /* fir low-pass filter */
float      IIR_Coeff[FIR_ORDER + 1];    /* low-pass filter */

volatile float* FIR_Sample_Real = (volatile float*)0x907000;
volatile float* FIR_Sample_Imag = (volatile float*)0x907200;
volatile float* FIR_Sample_Curr = (volatile float*)0x907400;
void main()
{
     MHZ = 60;
     enable_clock();                  /* Enables timebase interrupt */
     enable_cache();
     enable_monitor();
     enable_interrupts();

     init_apf();                 /* Initialise the all variables */

     clrscr();
     bold();
     printf("\n Active Power Filter Programs\n\n");
     normal();
     cursor(OFF);

     timer(0,100000);            /* set timer to drive sample interrupt */

     set_mux(2,0);               /*  set the channel two to mux 0 */
     set_gain(2,0);
     set_mux(3,0);               /*  set the channel three to mux 0 */
```

```
    set_gain(3,0);
    set_mux(4,0);                /*  set the channel four to mux 0 */
    set_gain(4,0);
    set_mux(5,0);                /*  set the channel five to mux 0 */
    set_gain(5,0);

    *DIO_CONFIG =0x01;                /* Set I/O to Output */
    *ADC0; *ADC1; *ADC2; *ADC3;       /* release all analog interrupts */
    *DAC0 = 0;

    *(INT_MASK) = 0x0f;          /* enable ADC2 interrupt only */
    trigger(0,1);                /* ADC1 triggered using timer 0 */
    trigger(0,2);                /* ADC2 triggered using timer 0 */
    trigger(0,3);                /* ADC3 triggered using timer 0 */
    trigger(0,4);                /* DAC0 triggered using timer 0 */

    Loop_Period= 31245;          /* Loop_Period= 312.5 microsecond (x 100) */
    time_0=uclock();

    printf("\n Program is running, press any key to stop it.\n");

    *DIO=0x0000;

    while (1)
    {
         time_e= (int) (100*uclock());       /* (x 100) */

         while ( ( time_e - time_0) > Loop_Period)
         {
            time_0=time_0+Loop_Period;
            freq_est();          /* Call freq_est every 4 samples 40 usec */
            filt_bnk();          /* Filter Bank filtering module 80 usec */
            wave_ref();          /* Reference Waveform generation module */
            hyst_pwm();          /* Hysteresis PWM */
            cariertime++;
         }
         *DAC0= (int) (-CompensatedCurr);
         *DAC1= (int) (-Ireactive);
    }

    *DIO=0x0000;
    *DAC0=0; *DAC1=0;
    ms(5);
    monitor();
}
```

A.1.2 Hysteresis PWM Module

```
inline void hyst_pwm(void)
{
     Sample11 = *ADC1;  Sample11 = *ADC1;
     APFCurrent = -(float) (Sample11>> 16);   /*Inverter Current pin 9 */

     if ( APFCurrent > 1.01 * CompensatedCurr ) *DIO= 65;
     if ( APFCurrent < 0.99 * CompensatedCurr ) *DIO= 20;
}
```

A.1.3 Frequency Estimation Module

```
/*
*    Frequency Estimation Program using FM Demodulation technique
*    interrupt handler for analog
*/
void freq_est(void)          /*  frequency estimation module */
{
     double Yk_R, Yk_I;
     double Uk_I, Uk_R;

     /* contains the analog inputs 4 & 5 */
     Sample21 = *ADC2;    Sample21 = *ADC2;
```

```
/* Input Supply Voltage pin 7 */
SupplyVoltage = -(float)( (Sample21 << 16) >> 16);

tic++;

if (tic == 1 )
{
     /* the multiplication of Cos Carrier with  Supply Voltage */
     FIR_Sample_Real[FIR_Pointer] = (float)( SupplyVoltage *
                                          (Omega*cariertime));

     /* the multiplication of Sin Carrier with Supply Voltage */
     FIR_Sample_Imag[FIR_Pointer] = (float)(-SupplyVoltage *
                                          sin(Omega*cariertime));

     /* get sample results, store to circular sample buffers */
     if(++FIR_Pointer == FIR_BUF_SIZE)
               FIR_Pointer = 0;

     /* call fir filter for removing the frequency component 20 Hz */
     Yk_R = fir(&FIR_Coeff[0], &FIR_Sample_Real[FIR_Pointer],
                          FIR_ORDER + 1);
     Yk_I = fir(&FIR_Coeff[0], &FIR_Sample_Imag[FIR_Pointer],
                          FIR_ORDER + 1);

     PHI = atan2(Yk_I,Yk_R);      /* Phase of Voltage to Cos wt */

     Uk_R =    ((Yk_R * Yk_2R) + (Yk_I * Yk_2I));
     Uk_I =    ((Yk_I * Yk_2R) - (Yk_R * Yk_2I));

     Yk_2R = Yk_1R;         /* buffer for last two values of Yk_R */
     Yk_2I = Yk_1I;         /* buffer for last two values of Yk_I */

     Yk_1R = Yk_R;          /* buffer for last value of Yk_R */
     Yk_1I = Yk_I;          /* buffer for last value of Yk_R */

     Phase = atan2(Uk_I,Uk_R);    /* Phase of signal (frequency
     variation df)*/

     DF = Phase * Phase_Offset;   /* Phase of signal (frequency
        variation df)*/
}
```

A.1.4 Power Factor Calculation

```
/* Update the Centre Frequency of Filter Bank */
if (tic  == 2 )
{
     FIR_Sample_Curr[FIR_Pointer] = (float)(-Harm[0].Yest *
                                          sin(Omega*cariertime+PHI));
     Yk_C = fir(&FIR_Coeff[0], &FIR_Sample_Curr[FIR_Pointer],
                                          FIR_ORDER + 1);
}
```

A.1.5 Harmonic Magnitude and Phase Calculations

```
     /* this Function computes the Fourier coefficient of
        sinusoid using  sliding goertzel algorithm */
if (tic  == 3 )
{
     if(++LUT_Pointer == 64)              LUT_Pointer= 0;

     if(j > 32-NN)   j= 0;    /*update magnitude every half cycle */
     for (m=j; m<j+NN; m++)        /* NN = 16*/
     {
        C1=Harm[m].Y;
        D1=(-1/Harm[m].SinTable[0])*(Harm[m].Yold -
                                Harm[m].CosTable[1]*Harm[m].Y);
        c1=Harm[m].CosTable[LUT_Pointer] * C1 -
                                Harm[m].SinTable[LUT_Pointer] * D1;
        d1=Harm[m].SinTable[LUT_Pointer] * C1 +
```

```
                                        Harm[m].CosTable[LUT_Pointer] * D1;
            Harm[m].Phase=atan(-c1/d1);      /*Phase Computation*/
            Harm[m].Mag=sqrt(c1*c1+d1*d1);   /*Amplitude Computation*/
      }
      j=j+NN;
      }
```

A.1.6 Filter Bank Parameterisation

```
      /* Update the Centre Frequency of Filter Bank */
      if (tic  == 4 )
      {
            tic=0;
            OmegaTi=  ((Fundamental+DF) * Sampling_Period) * 2 *PI;
            for (m = 0; m < No_Harmonics; m++)
            {
               Harm[m].A=cos((m+1)*OmegaTi);
            }
      }
```

A.1.7 Checking the Harmonic Standard Recommended Values

```
      /* Update the Standard Application for Wave_gen module*/
      if (tic  == 4 )
      {
            tic=0;
            STD_BASE= Harm[0].Mag;
            for (m=1; m<No_Harmonics; m++)            /*No_Harmonics*/
            {
               dummy2 = Harm[m].Std * STD_BASE;
               if (Harm[m].Mag > dummy2)
                     Harm[m].Gain = 1 - (dummy2/ Harm[m].Mag);
               else
                     Harm[m].Gain = 0;
               THD+= (Harm[m].Mag * Harm[m].Mag);
            }
            THD= sqrt(THD)/STD_BASE;
      }
}
```

A.1.8 Initilasation

```
void init_apf(void)                    /*  initialise the whole variables */
{
      char filename[20];               /* Input File Name  */
      long infile;                     /* Input file handle */
      long outfile;                    /* Output file handle */
      char buff[4];                    /* IEEE Floating output */
      floatSum_Of_Coeff;               /* Sum of Coeff for Normalization */

      if ( (infile = fopen(".\\f800.bin", "r")) == 0)
      {
            printf("\nInput file open error - Program terminating!");
            monitor();
      }
      for (i = 0; i < FIR_ORDER + 1; i++)
      {
            fread(buff, 4, 1, infile);
            FIR_Coeff[i] = from_ieee(buff[0]); /* low-pass filter */
            Sum_Of_Coeff += FIR_Coeff[i];
      }
      fclose(infile);

      /* normalize filter coefficients */
      for (i = 0; i < FIR_ORDER + 1; i++)
      {
            FIR_Coeff[i] /= Sum_Of_Coeff;
      }
```

```
    Sampling_Frequency = 2 * No_Harmonics * Fundamental;
    Sampling_Period = 1 / ((float) (Sampling_Frequency));
    Loop_Period = 1000000 / ((float) (Sampling_Frequency));

    Phase_Offset =       Sampling_Frequency/(4*PI) /4;
    Omega = (2*PI*Fundamental)/Sampling_Frequency;

    /* Initialisation for filter bank module */
    for (m = 0; m < No_Harmonics; m++)
    {
        Harm[m].A=cos( Omega *(m+1)); /* Centre frequency of each filter*/
        Harm[m].Y=0;
        Err -= Harm[m].Y;      /* weighted error (input to all filters) */

        /* lokkup table for harmonic prediction*/
        Harm[m].SSin=sin(Omega * (m+1)) / Omega/(m+1);
        Harm[m].CCos=cos(Omega * (m+1));
    }

    PErr= 4* Ko * Err;

    for (m = 0;m < No_Harmonics; m++)
    {
        Harm[m].W2= PErr * Harm[m].A + 2 * Harm[m].A * Harm[m].Y;
        Harm[m].WP= -PErr - Harm[m].Y;
        Harm[m].Y= Harm[m].W2;
    }

    printf("\nBuilding Sine and Cosine table for Magnitude Measurement.");
    for ( m = 0; m < No_Harmonics; m++ )
    {
        for ( i = 0; i < 64; i++ )/* fill sin table for each harmonic */
        {
           Harm[m].SinTable[i]=sin(Omega*(m+1) * (i+1));
           Harm[m].CosTable[i]=cos(Omega*(m+1) * (i+1));
        }
    }
    if ( (infile = fopen(".\\Standard.bin", "r")) == 0)
    {
           printf("\nInput file open error - Program terminating!");
    }
    for (m = 0; m <  No_Harmonics; m++)
    {
        fread(buff, 4, 1, infile);
        Harm[m].Std= from_ieee(buff[0]);    /* Harmonic Standard*/
    }
    fclose(infile);

    printf("\n Initialization Finished...");

}
```

A.1.9 Harmonic Estimation Module

```
void filt_bnk(void) /*  filter bank filtering module */
{
    Sample22 = *ADC2;    Sample22 = *ADC2;
    LoadCurrent  = -(float)(Sample22 >> 16);
    Err= LoadCurrent;                  /* normalise input voltage 3276.7 */
    for (m=0; m < No_Harmonics; m++)         /* No_Harmonics =32 */
    {
        Err = Err - Harm[m].Y; /* weighted error (input to all filters) */
    }

    PErr = 4* Ko * Err;

    for (m=0; m<No_Harmonics; m++)
    {
        Harm[m].W2 = Harm[m].A * PErr + 2 * Harm[m].A * Harm[m].Y +
                                                        Harm[m].WP;
        Harm[m].WP = -PErr - Harm[m].Y;
        Harm[m].Yest = Harm[m].W2 * Harm[m].CCos + Harm[m].SSin *
```

```
                                                    (Harm[m].W2 - Harm[m].Y);
            Harm[m].Yold = Harm[m].Y;
            Harm[m].Y= Harm[m].W2;
      }
}
```

A.1.10 Reference Waveform Generation Module

```
void wave_ref(void)
{
      CompensatedCurr =Err;        /*[put the reduce of filter bank output */
      for (m=1; m<No_Harmonics; m++)          /*No_Harmonics*/
            CompensatedCurr +=  Harm[m].Y * Harm[m].Gain; /* weighted error */
            Ireactive = 2 * Yk_C * sin(Omega*cariertime +PHI);
      CompensatedCurr = CompensatedCurr - Ireactive ;
}
```

A.2 EQUAL AREA PWM TECHNIQUE

```
/* Equal Area PWM DSP module program EAPWM.C
* Generate a sine wave on DAC channels 0 and 1 */

#include "stdio.h"
#include "periph.h"
#include "math.h"

#define INTERRUPT 2                 /* interrupt bit# for analog interrupt */
#define RESOLUTION 200              /* Defines # points in waveform */
#define DAC_CHANNELS 2              /* number of DAC channels */
#define ADC_DEVICES_MAX 8           /* max number of ADC channels 8 */

/* Prototypes */

void sinbuild(float M, int N);
void sinbuild2(int N);

void c_int02();
int sign(float a);

volatile float frequency;
volatile float Module;

int pwmwave[RESOLUTION];  /* Switching pattern for first leg */
int prev = 0,jj=0;
int S11=0,S12=0,S21=0,S22=0,SS=0;

main()
{
      int N,previous;
      float step,Max_Freq;
      MHZ = 60;

      enable_interrupts();

      printf("  WAVE - generate sine waveforms on DAC 0 and 1\n\n");
      printf("\n   Enter The No. of Pulses per Cycle (N is evev):  ");
      scanf("%d", &N);
      Max_Freq = 100000. / RESOLUTION;
      printf("\n   Enter sine wave frequency 10-%3.1f: ",Max_Freq);
      scanf("%f", &frequency);

      if(frequency < 10.0)          frequency = 10.0;
      if(frequency > Max_Freq)      frequency = Max_Freq;

      printf("\n   Enter the Modulation Index 0-1: ");
      scanf("%f", &Module);

      if(Module < 0.0) Module= 0.1;
      if(Module > 1.0) Module= 1.1;
```

```
    sinbuild(Module, N);

    cursor(OFF);
    timer(0,0);
    install_int_vector(c_int02, INTERRUPT + 1);

    *DIO_CONFIG =0x01;                  /* Set I/O to Output */

    /* release all analog interrupts */
    *ADC0; *ADC1; *ADC2; *ADC3;
    *DAC0 = 0;  *DAC1 = 0;
    *DIO=0x00;

    *(INT_MASK) = 0x02;  /* enable ADC2 interrupt only */

    /* connect DAC conversion trigger to channel 0 timer */
    trigger(0,1);
    trigger(0,2);
    trigger(0,4);

    /* initialize hardware timer to DAC sample frequency */
    timer(0, (int)(RESOLUTION * frequency));
    /* install and enable DAC interrupt */
    install_int_vector(c_int02, INTERRUPT+1);
    enable_interrupt(INTERRUPT);

    printf("\n\n   Wave Outputs are on DAC0 and DAC1\n");
    printf("\n   Press any key to stop programs. \n");

    while(!kbd_hit());
    getchar();

    printf("\n\n End of Active Power Filter Program 1...");
    disable_interrupt(INTERRUPT);

    while(!kbd_hit());

    *DIO=0x00;
    *DAC0=0; *DAC1=0;
    getchar();
    monitor();
}
```

A.2.1 Look up Table

```
/* This routine makes a Equal Area look up tables for Inverter Input:
    frequency:     Frequency of PWM Waveform
    Module:        Modulation index
    N:      Number of pulse per cycle
*/
void sinbuild(float Module, int N)
{
    float pi = 4. * atan(1.0);
    long double xx,xx0=0.;
    long double teta1=0, teta2=0;
    float step,Max_Freq;
    float xsin;

    int i,ii,j,k1,k2,signx;
    long double area, half_area;

    /* build sine waveform data table */

    for (i=1;i <= N; i++)
    {
        teta2= (float) i * 2. * pi / N;     /*   */
        area = (float) cos(teta1) + cos(teta2);   /*   */

        xx =  acos(area/ 2.);               /*   */
        if (xx < teta1) xx = 2*pi -xx;
        xsin=sin(xx);
        signx =  sign( xsin);
```

```
            area = (float) cos(teta1) - cos(teta2);   /*    */
            half_area = fabs(area) * Module / 2;
            teta1=teta2;

            k1 = (int)(RESOLUTION * (xx - half_area) /pi /2);      /*    */
            k2 = (int)(RESOLUTION * (xx + half_area) /pi /2);      /*    */

            for (j = k1; j < k2; j++)                  /*    */
            {
               pwmwave[j] = 32000 * signx;
            };
      }
}
```

A.2.2 Switching Sequences

```
/* DAC interrupt routine
*  Each time the timer expires, prev is incremented, rolling
*  over at the value of resolution.   prev  is used as an index into
*  the waveform array.  The current waveform voltage  waveform[prev]
*  is output to the DACs.*/

void c_int02()
{
      int tt;
      if (++prev == RESOLUTION)
      {
            prev = 0;
      }
      S11 = (pwmwave[prev] > 0);          /* pin 24 */
      S12 = (pwmwave[prev] < 0);          /* pin 23 */

      S21 = (S21 | S12 ) & (~ S11);       /* pin 26 */
      S22 = (S22 | S11 ) & (~ S12);       /* pin 25 */
      S22= (~ S21);

      tt =  S11 + 4 * S12 +  16 * S21 +  64 * S22;
      *DIO=( 0x55 & tt );

      *DAC0 = (int) (pwmwave[prev]);
      *DAC1 = (int) (tt*400);

}
```

A.2.3 Sign Function

```
/* Sign */
int sign(float inpval)
{
      if (inpval == 0.)  return 0;
      if (inpval > 0.)  return 1;
      return -1;
}
```

APPENDIX

B.

MICRO-CONTROLLER PROGRAMS

B.1 FILTER BANK

```
PROGRAM FB.UCP;
{ Filter Bank Program }

{ 1.0 Free-running loop. Check ability to read time into simulation }
{ 2.0 Added interrupt processing routine as test                    }
{ 3.0 Single phase hysteresis current controller. Control executed  }
{       at external interrupt. Reference is 15A pk 50Hz sinewave.   }
{       No deadtime between transistor switchings.                  }

VAR
    time1, time2, start_time, enable: REAL;
    v_err, v_err0, Pgain, Igain, Dgain: REAL;
    Icntrl, Pcntrl, Dcntrl, Control: REAL;
    I_Load: REAL;
    V_dc2:  REAL;
    V_s:    REAL;
    VS:     REAL;
    I_Loss: REAL;
    I_Coef: REAL;
    I_Comp: REAL;
    Err:    REAL;
    PErr:   REAL;
    Ko:     REAL;
    Omega;  REAL;
    SL;     REAL;
    dummy;  REAL;
    m:      INTEGER;
    W2:     ARRAY[11] of REAL;
    WP:     ARRAY[11] of REAL;
    Y:      ARRAY[11] of REAL;
    Yest:   ARRAY[11] of REAL;
    Std:    ARRAY[11] of REAL;
    CCos:   ARRAY[11] of REAL;
    SSin:   ARRAY[11] of REAL;
    A:      ARRAY[11] of REAL;
{-------------------------------------------------------------}
PROCEDURE Interrupt;
    { Executed once every interrupt cycle }
BEGIN

    IF(enable<>0) THEN
        BEGIN
```

```
            I_Load:= vin[2];  { Get load current }
            Err:=  vin[2];    { store load current in residue }
            V_s:= vin[6];      {Get Source volatge }

            V_dc2:= vin[4];   { Get DC link volatge }
            v_err:=VS -V_dc2;
            Pcntrl:= v_err *Pgain;
            Icntrl:= Icntrl + v_err *Igain;
            Dcntrl:= (v_err - v_err0) *Dgain;
            Control:= Pcntrl + Icntrl +Dcntrl;
{           IF (Control <= 0) THEN Control:=0;}
            v_err0:=v_err;
            I_Loss:= Control * I_Coef * V_s;

            { Loss waveform synthesis; it is in phase with supply volatge}
            time2:= gettime;


            {Sending to output for monitoring }
            vout[3]:= I_Loss;

            IF(time2> 0.5) THEN
               BEGIN
                  SL:= 1;      {Step Change in load  after t=0.25}
               END;
            ELSE
               BEGIN
                  SL:= -1;
               END;
            vout[2]:= SL;

            { Harmonic estimation using filter bank }
            FOR m:=1 TO 11 DO Err:= Err - Y[m];

            PErr:=4*Ko*Err;

            FOR m:=1 TO 11 DO
                BEGIN
                    W2[m]:= A[m] * PErr + 2 * A[m] * Y[m] + WP[m];
                    WP[m]:= -PErr - Y[m];
                    Yest[m]:= W2[m]*CCos[m]+SSin[m]* (W2[m]-Y[m]);
                    Y[m]:=  W2[m];
                END;
            I_Comp:= Err;
            { Compensating current with harmonic prediction}
            FOR m:=2 TO 5 DO I_Comp:=I_Comp + Y[m] * Std[m];


            { send the refernce compensation current to next module }
            vout[1]:=I_Comp - I_Loss;
        END;
END;


{-----------------------------------------------------------------}


BEGIN
    { Initialise variables }
    time1:= 0;
    start_time:= .001;          { 100ms after simulation start }
    enable:= 0;                 { Enable interupt}
    I_Load:= 0.0;               { Load current }
    Omega:= (2*3.14*50)/3200;   { Frequency of carrier signal }

    VS:=114;              { squared reference source volatge value}
    v_err:=0;
    v_err0:=0;

    Pgain:=10;
```

```
    Dgain:=0;
    Igain:=0.01;
    I_Coef:=0.0047/VS;

    {IIR Erro Filter bank, Feedback Gain (0.4/No_Harmonics)}
    Ko:= 0.0125;                { Filter bank feedbank gain }
    vout[2]:=-1;


    { Filter notch frequency paramet}
    FOR m:=1 TO 11 DO A[m]:= cos(Omega*m);
    FOR m:=1 TO 11 DO Std[m]:= 1;
    FOR m:=1 TO 11 DO SSin[m]:=sin(Omega*m)/Omega/m;
    FOR m:=1 TO 11 DO CCos[m]:=cos(Omega*m);
    FOR m:=1 TO 11 DO Y[m]:=0;
    FOR m:=1 TO 11 DO Yest[m]:=0;
    FOR m:=1 TO 11 DO W2[m]:=0;
    FOR m:=1 TO 11 DO WP[m]:=0;
REPEAT  { Main program loop }
    time1:= gettime;
    IF(time1<start_time) THEN
        { Disable all outputs and actions before start_time }
        BEGIN
        enable:= 0;
        END;
    ELSE
        { Enable control functions after start_time }
        BEGIN
        enable:= 1;
        END;
UNTIL FALSE;  { end of main endless loop }
END.
```

B.2 HYSTERESIS PWM

```
PROGRAM Hyst.UCP;
{ Control program for PWM Inverter }

{ 1.0   Free-running loop. Check ability to read time into simulation }
{ 2.0   Added interrupt processing routine as test                    }
{ 3.0   Single phase hysteresis current controller. Control executed  }
{           at external interrupt. Reference is 15A pk 50Hz sinewave. }
{           No deadtime between transistor switchings.                }

VAR
    time1, start_time, enable: REAL;
    mains_period: REAL;
    I_Ref: REAL;
    I_APF:  REAL;
    I_hyst: REAL;
{-------------------------------------------------------------------}
PROCEDURE Interrupt;
    { Executed once every interrupt cycle }
BEGIN
    IF(enable<>0) THEN
    BEGIN
        { Get rectifier and load current }
        I_Ref:= vin[1];
        vout[1]:= I_Ref;

        { Get active power filter current  }
        I_APF:= vin[4];

        { Do hysteresis control of U phase }
        IF(I_APF>(I_Ref+I_hyst)) THEN
            { Switch on lower transistor }
            BEGIN
            vout[0]:= -1;
            vout[2]:= +1;
            vout[4]:= +1;
```

```
            vout[6]:= -1;
            END;
        IF(I_APF<(I_Ref-I_hyst)) THEN
            { Switch on upper transistor }
            BEGIN
            vout[0]:= +1;
            vout[2]:= -1;
            vout[4]:= -1;
            vout[6]:= +1;
            END;
    END;
END;


{--------------------------------------------------------------------}


BEGIN
    { Initialise variables }
    time1:= 0;
    start_time:= 0.001;           { 10ms after simulation start }
    enable:= 0;
    mains_period:= 0.02;        { 20ms for 50Hz }
    I_hyst:= 0.1;              { 1A }
    I_APF:= 0.000;
    vout[0]:= -1;        { Up transistor off }
    vout[2]:= -1;        { Up transistor off }
    vout[4]:= -1;        { Up transistor off }
    vout[6]:= -1;        { Up transistor off }


REPEAT  { Main program loop }

    time1:= gettime;
    IF(time1<start_time) THEN
        { Disable all outputs and actions before start_time }
        BEGIN
        enable:= 0;
        END;
    ELSE
        { Enable control functions after start_time }
        BEGIN
        enable:= 1;
        END;
;
UNTIL FALSE;  { end of main endless loop }
END.


{--------------------------------------------------------------------}
```

APPENDIX

C.

RECOMMENDATIONS OF HARMONIC STANDARDS

C.1 K_h^{std} CALCULATION

The following relationships are based on these assumptions:

$$L = \frac{\sqrt{3} * 100 * I_h * E}{K_h^{std}} \tag{C.1}$$

$$U_h = \frac{\sqrt{3} * h * 100 * I_h * E}{10 * F} \tag{C.2}$$

$$I_{h(\max)} = U_{h(\max)} * \frac{10 * F}{\sqrt{3} * h * E} \tag{C.3}$$

$$U = \frac{h * K_h^{std} * L}{1000 * F} \tag{C.4}$$

where

- L = convertor full load rating, in kilovolt amperes,
- $I_h = h^{th}$ harmonic current, in amperes,
- E = system line-to-line voltage, in kilovolts,
- $K_h^{std} = h^{th}$ harmonic current, as percentage of full load current

  (Table C.1 shows typical values for K_h^{std} [4]),

- h = order of harmonic,
- U_h = percentage h^{th} harmonic voltage drop, at point of common coupling,
- F = fault level at point of common coupling, in megavolt amperes.

Table C.1: Recommended values for current harmonic distortion [4].

Harmonic order (h)	**Maximum harmonic current ratio, K_h^{std} Effective number of pulses 6, 12, 24**		
3	6	12	24
5	17.5	2	2
7	11	1.5	1.5
11	4.5	4.5	1
13	3	3	0.75
17	1.5	0.2	0.2
19	1.25	0.15	0.15
23	0.75	0.75	0.75
25	0.75	0.75	0.75