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**Abstract**

Optical feedback Self-mixing Interferometry (OFSMI) can achieve a high-resolution displacement sensing and measurement by using advanced digital signal processing. However, most existing signal processing algorithms used for OFSMI signals are implemented on a PC by Matlab or other programming languages. In this case, the whole structure of OFSMI sensing system is incompact and the measurement is in low speed. The design trends in sensing systems are towarding to small size, high integration and fast real time processing. These trends require us to improve the existing OFSMI design. It is a good solution to apply Field-programmable gate arrays (FPGAs) technique onto OFSMI sensing systems. In this work, we designed a FPGA based signal processing unit for an OFSMI displacement sensing system. The OFSMI sensing signals observed from an OFSMI system is connected to a FPGA development board (Spartan-3E) for high speed signal processing. The FPGA processing unit retrieves the displacement information carried in the OFSMI signals. The FPGA design includes noise reduction, signal peak detection and impulse magnitude tracking. As the magnitude of the sensing signal is time-varying, for adapting the variation, a dynamic updating algorithm is introduced in the magnitude tracking unit. Both simulation and hardware co-simulation show that the OFSMI system with a FPGA based signal processing unit can achieve fast and reliable displacement sensing.

**Keywords**

processing, signal, optical, fpga, mixing, self, feedback, interferometry, system

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# FPGA-based Signal Processing in an Optical feedback Self-mixing Interferometry System

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## ABSTRACT

Optical feedback Self-mixing Interferometry (OFSMI) can achieve a high-resolution displacement sensing and measurement by using advanced digital signal processing. However, most existing signal processing algorithms used for OFSMI signals are implemented on a PC by Matlab or other programming languages. In this case, the whole structure of OFSMI sensing system is incompact and the measurement is in low speed. The design trends in sensing systems are towarding to small size, high integration and fast real time processing. These trends require us to improve the existing OFSMI design. It is a good solution to apply Field-programmable gate arrays (FPGAs) technique onto OFSMI sensing systems. In this work, we designed a FPGA based signal processing unit for an OFSMI displacement sensing system. The OFSMI sensing signals observed from an OFSMI system is connected to a FPGA development board (Spartan-3E) for high speed signal processing. The FPGA processing unit retrieves the displacement information carried in the OFSMI signals. The FPGA design includes noise reduction, signal peak detection and impulse magnitude tracking. As the magnitude of the sensing signal is time-varying, for adapting the variation, a dynamic updating algorithm is introduced in the magnitude tracking unit. Both simulation and hardware co-simulation show that the OFSMI system with a FPGA based signal processing unit can achieve fast and reliable displacement sensing.

**Keywords:** FPGA based signal processing, filter design, self-mixing interferometry, optical feedback self-mixing, displacement sensing, semiconductor laser sensing

## 1. INTRODUCTION

The optical feedback self-mixing interferometry (OFSMI) technique has been being an active research area in the last few decades [1, 2]. The OFSMI technique makes use of the self-mixing effect. The self-mixing effect occurs when part of the laser beam, which is emitted by a semiconductor laser (SL), back-reflected from a moving target and is added with the standing wave inside the active cavity of the laser diode (LD), resulting in the modulation of both the amplitude and the frequency of the lasing field. Compare with the other conventional interferometric techniques, OFSMI is much simplicity in system structure and low cost in implementation because many optical elements such as beam splitter, reference mirror and external photodetector are not required, according to which OFSMI has attracted extensive research activities and have been designed for a variety of applications such as dimensional control, vibration measurements, blood flow measurement, sound reproduction, angle measurements etc[3, 4]. The system consists of a LD packaged with photodetector (PD), a focusing lens, and a signal processing unit. When the OFSMI effect occurs, variations of the output power, referred to as the OFSMI signal, are detected by the PD and sent to the signal processing unit where the signal is analyzed in order to extract useful information. The self-mixing interference was used to measure the displacement with an accuracy of half-wavelength ($\lambda/2$) by counting the OFSMI signal peaks. In order to do the real time digital signal processing, some kinds of real time signal processing system has been implemented. A pure hardware system was implemented to do the real time signal pre-processing by using some discrete electronic components, and a PC was used to reconstruct the displacement and display[5]. Then an improved signal processing system with better accuracy has been implemented with a phase-looked loop (PLL) based on the former system[6]. After that, another pure hardware signal processing system was suggested by using a high-pass filter to pre-process the OFSMI signal, which will effectively reduce the noise, and also use a hardware up-down counter with a 5-digit display instead of PC[7]. For the sensing application, a compact sensor with a PC interface by using OFSMI technique has been described[8]. The sensor will output the signal after pre-processing in the alignment phase, and then send the signal to the PC to use the software to do the displacement reconstruction.

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As for the industrial sensing applications, a compact system with high performance in real time signal processing and portability is essential. In another word, the sensing system should have the features with small size, high integration and high efficient. Recent years, Field-programmable gate arrays (FPGAs) has been widely used in real time signal processing due to its high integration, high speed performance such as it can offers a viable alternative for speeding up the real-time signal processing without sacrificing accuracy or incurring excessive communication latency[9]. In order to use the features of the FPGA into the OFSMI technique, it is good solution to combine the FPGA technology and the OFSMI sensing system design together.

This paper presents the use of a FPGA-based displacement sensing by using OFSMI technique. The sensing signal from the OFSMI system is feed into a FPGA development system for high speed processing, from which the displacement information can be obtained. The design of the FPGA unit includes noise reduction, signal peak detection and impulse magnitude tracking. By investigating the features for both the sensing signal and the noise involved, we decide to use a median filters for removing sparkle like noise while a Bandpass FIR filter for reducing the high frequency noise and the slow time-varying fluctuation. As the magnitude of the sensing signal is time-varying, for adapting such variation, a dynamic updating threshold is specially considered in the design for guarantee the measurement accuracy of the tracking unit. The preliminaries on FPGA-based signal processing for an OFSMI system are described in Section II. Section III presents the implementation details and the results, where the real-time simulation results by using the hardware co-simulation method are compared with the Matlab offline simulation results. Conclusions are given in Section IV.

## 2. FPGA-BASED SIGNAL PROCESSING FOR OFSMI SIGNALS

### 2.1 The displacement sensing principle using OFSMI

There are two alternative and equivalent methods for describing self-mixing optical feedback interferometric effects: the Long and Kobayashi equations based approach[7] and the three-mirror cavity based approach[10]. Both approaches yield the same description about the behavior of a single-mode SL with optical feedback, and take the form as following equations:

$$\phi_F(n) = \phi_0(n) - C \cdot \sin\left[\phi_F(n) + \arctan(\alpha)\right] \tag{1}$$

$$P\left(\phi_F(n)\right) = P_0\left[1 + mF\left(\phi_F(n)\right)\right] \tag{2}$$

$$F\left(\phi_F(n)\right) = \cos\left(\phi_F(n)\right) \tag{3}$$

Eq. (1) describes the phase relationship between the feedback phase $\phi_F(n)$ and the light phase $\phi_0(n)$. $n$ is the discrete time index. $C$ is the optical feedback level factor and $\alpha$ is the linewidth enhancement factor. While Eq. (2) accounts for the laser power fluctuations as result of the interferometric phase variations with $P\left(\phi_F(n)\right)$ and $P_0$ denote the laser power with and without feedback respectively. $F\left(\phi_F(n)\right)$ is called the interferometric function which gives the effect of the external cavity length to the emitted power by the SL, and $m$ is called modulation index (typically $m \approx 10^{-3}$). $F\left(\phi_F(n)\right)$ is defined by Eq.(3) and is a periodic function of period $2\pi$, it is also called normalized OFSMI signal. Some simulation waveforms are shown in Fig. 1. In order to obtain the simulation OFSMI signal $E(n)$, some important parameters values are set as below. $C = 3$, $\alpha = 3$, the vibration amplitude is $5\pi$, the frequency of the OFSMI signal is $100Hz$, and the sample frequency is $102.4kHz$. $E(n)$ is the normalized OFSMI signal. $D(n)$ is the pulse train which can be obtained from $E(n)$. $C(n)$ is the reconstructed displacement. The displacement is obtained by counting the pulse train signal. The displacement is increased by $\lambda / 2$ for a positive pulse and decreased by $\lambda / 2$ for a negative pulse.

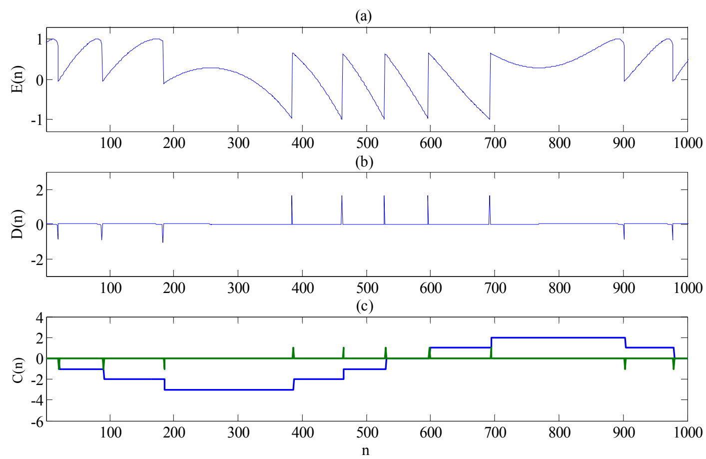


Figure 1. (a) Normalized OFSMI signal $E(n)$, (b) pulse train $D(n)$ obtained from $F(n)$, (c) reconstructed displacement $C(n)$.

### 2.2 FPGA design for displacement reconstruction

The FPGA-based OFSMI displacement sensing system is shown in Fig. 2. It contains a sensor head and a FPGA development board. The sensor head is built using a basic OFSMI structure[11]. OFSMI signals displacement of the target can be generated by the sensor head. The FPGA part is used to do pre-processing OFSMI signals and displacement reconstruction.

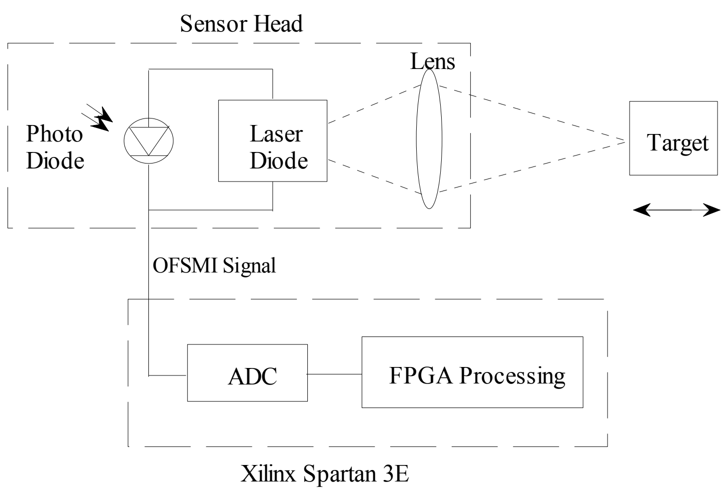


Figure 2. Structure of the FPGA processing system.

We use a Xilinx Spartan 3E development board for the FPGA design. One push button (BTN_SOUTH: K17) is used to reset the whole system. An OFSMI signal is connected to an amplifier (LTC6912-1) provided by the Spartan 3E board. The amplified signal then converted by analogue to digital converter (ADC), LTC 1407A-1. The discrete OFSMI signal is then processed by FPGA, from which, the displacement information carried in the OFSMI signal can be retrieved. The obtained displacement to be displayed on the oscilloscope is sent to a digital to analog converter (DAC), LTC 2624, for further display using oscilloscope.

The FPGA processing part consists of the following four subsystems. These subsystems are shown in Fig. 3, including Noise reduction unit, Signal peak detection unit, Impulse magnitude tracking unit and Reconstruction unit. Fig.3 shows the structure of the FPGA-based OFSMI signal processing. The reconstruction unit will transform the waveform from the pulses count numbers to the displacement of the target. The details about the functions and configuration of other subsystems are described in the next few sections.

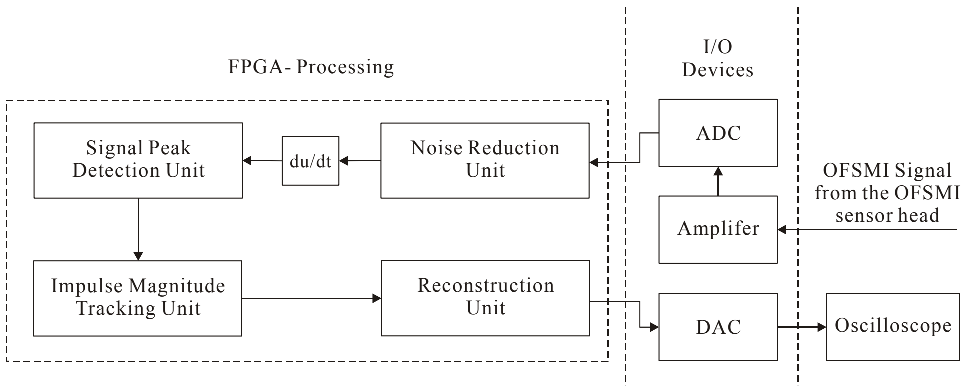


Figure 3. The structure of the FPGA-based OFSMI signal processing.

## 2.3 Noise Reduction

The noise reduction unit consists of a band-pass filter and an adaptive median filter. OFSMI signal contains the sparkle-like noise and slow-time envelope fluctuation[12]. The band-pass filter is designed to reduce the slow-time envelope fluctuation. A median filter which is shown in Fig. 4 is used to remove the sparkle-like noise. The median filter is a nonlinear filter and is proven to be a efficient tool for combating impulsive noises.

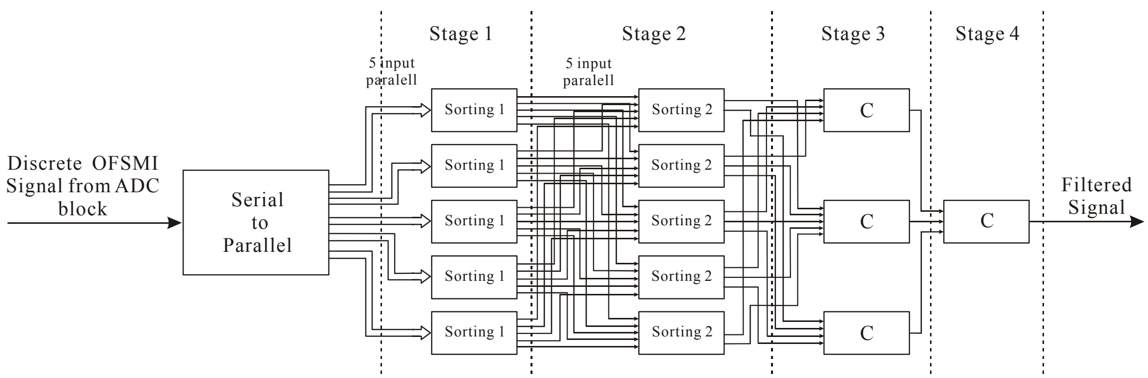


Figure 4. The structure of the 25 points median filter.

The Bandpass filter is generated by the Xilinx system generator by using FDA tools. As the span of a sparkle-like impulse is less than 20 points in most cases in our OFSMI system, we use a 25 points median filter to remove the sparkle parts. The median filter design makes fully use of the parallel architecture of the FPGA. Firstly, sequential input (OFSMI) data are collected and converted into five groups in parallel output at block “serial to parallel”. Each group goes to its corresponding block named “sorting”. Each sorting block sorts its 5 input data in descending order and then sends them to next 5 “sorting” blocks respectively. The sorting blocks in stage 2 still sort the input data in descending order, however, the output is different. The first and second sorting blocks in stage 2 output the first 2 and 3 data respectively, the third sorting block output the middle 3 data and the fourth and fifth sorting blocks output the last 3 and 2 data respectively. Stage 3 produces 3 data which are the first data of the first comparator output, the third data of the second comparator and the last data of the third comparator. Stage 4 finally finds the middle value among the 25 input data.

## 2.4 Pulse peak detection

After OFSMI signal preprocessing, we use a differential unit to get a pulse train signal. The signal can be used for displacement reconstruction. However, the pulse train has different magnitude. Thus, an adaptive threshold is used to adaptive the varying magnitude of pulse train.

After derivate, the signal value is compared with the former value and hold the bigger one as the maximum. The maximum value will update continuously and compare with a pre-set positive threshold until it is bigger than the preset positive threshold. Meanwhile, the latest maximum value is hold as a new positive threshold and maximum value will be reset to the initial value. The signal will derivate OFSMI signal will stop from comparing with the pre-set threshold. Meanwhile, the signal data is comparing with the positive threshold. If the signal data is bigger than the threshold, then the comparator will output '1', otherwise, the comparator will output '0'. The comparison is pipelining. When sequence 1-1-0 comes out as a result of comparison with the threshold, the latest maximum value will be treated as the positive impulse value and set as the new positive threshold. When the sequence 0-0-1 comes out, the internal positive counter is incremented. The new threshold is always set at 70% of the signal impulse value of previous period. Fig. 6 shows the block-frame of the algorithm, only for the positive count; as the negative one is the same.

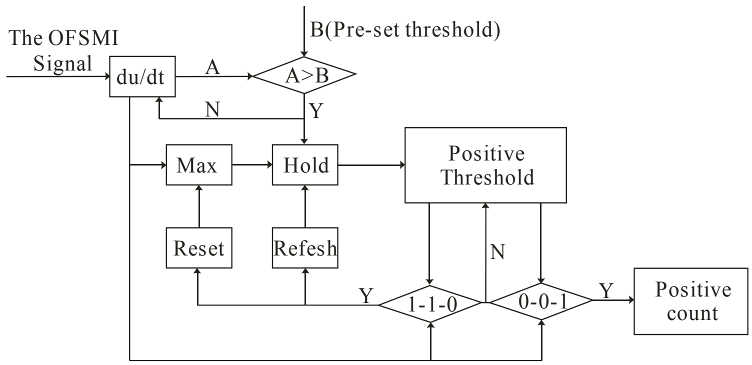


Figure 6. Block-frame of the adaptive threshold in FPGA.

## 3. CO-SIMULATION OF THE DESIGN

The FPGA-based signal processing unit was implemented on a Xilinx ® Spartan-3E FPGA (XC3S500E-4FG320C) Development Board. The FPGA used on this board has the following features: 10478 logic elements (LEs); 128 Mbit Parallel Flash, 16 Mbits of SPI serial Flash, 20 multiplier and 232 maximum user I/O pins, 4-output SPI-based Digital-to-Analog Converter (DAC), 2-input SPI-based Analog-to-Digital Converter (ADC) with programmable-gain pre-amplifier[13]. The internal clock is from the 50-MHz oscillator on the development board.

The FPGA design described in section 2 is converted in a VHDL code by using the Xilinx system generator. The code is downloaded into the SRAM on the FPGA development board through the USB-based JTAG interface. The hardware co-simulation is used to test our design.

The experimental OFSMI signal waveform is shown in Fig. 8(a). The discrete signal of the experimental OFSMI signal is shown in Fig. 8(b). Without preprocessing the signal, the noise will highly affect the detection accuracy. In order to solve this problem, the bandpass filter and the median filter are introduced. The waveform in Fig. 8(c) shows the output of the noise reduction unit. Fig. 8(d) shows the discrete signal after the derivate unit and the peak values of the pulses which have been detected by the signal peak detection unit. Due to the pre-set threshold, the updating and optimize of the adaptive threshold in the first few loops of the calculation will not affect the count result of the positive and negative impulse. All the pulses will be counted correctly. The reconstructed displacement of the experiment OFSMI signal is shown in Fig. 8(e), which is also the output of the reconstruction unit. As the accuracy of the sensing displacement is half-wavelength ($\lambda/2$) by counting the signal peaks, the efforts will be deployed to develop more accuracy method to reconstruct the real displacement.

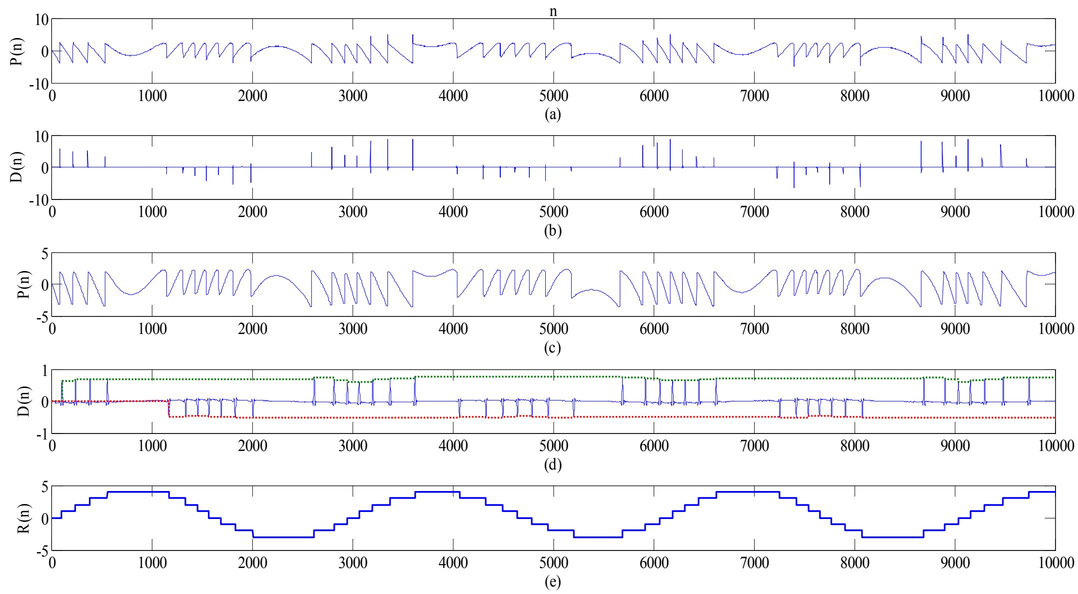


Figure 8. (a) The Experimental OFSMI signal, (b) derivative of experimental signal, (c) the median filtered signal waveform, (d) derivative of experimental signal after filtered and the peak value detection,(e) the displacement reconstruction.

## 4. CONCLUSION

The paper presents a FPGA-based signal processing for an OFSMI displacement sensing system. The FPGA design includes signal preprocessing and displacement reconstruction. With the bandpass filter and the median filter, the slow time-varying fluctuation and the sparkle-like noise can be effectively reduced. By introducing an adaptive threshold method, the peak detection block can achieve accurate fringe counting. Both simulation and hardware co-simulation show that the OFSMI system with a FPGA based signal processing unit can achieve fast and reliable displacement sensing.

## ACKNOWLEDGMENT

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